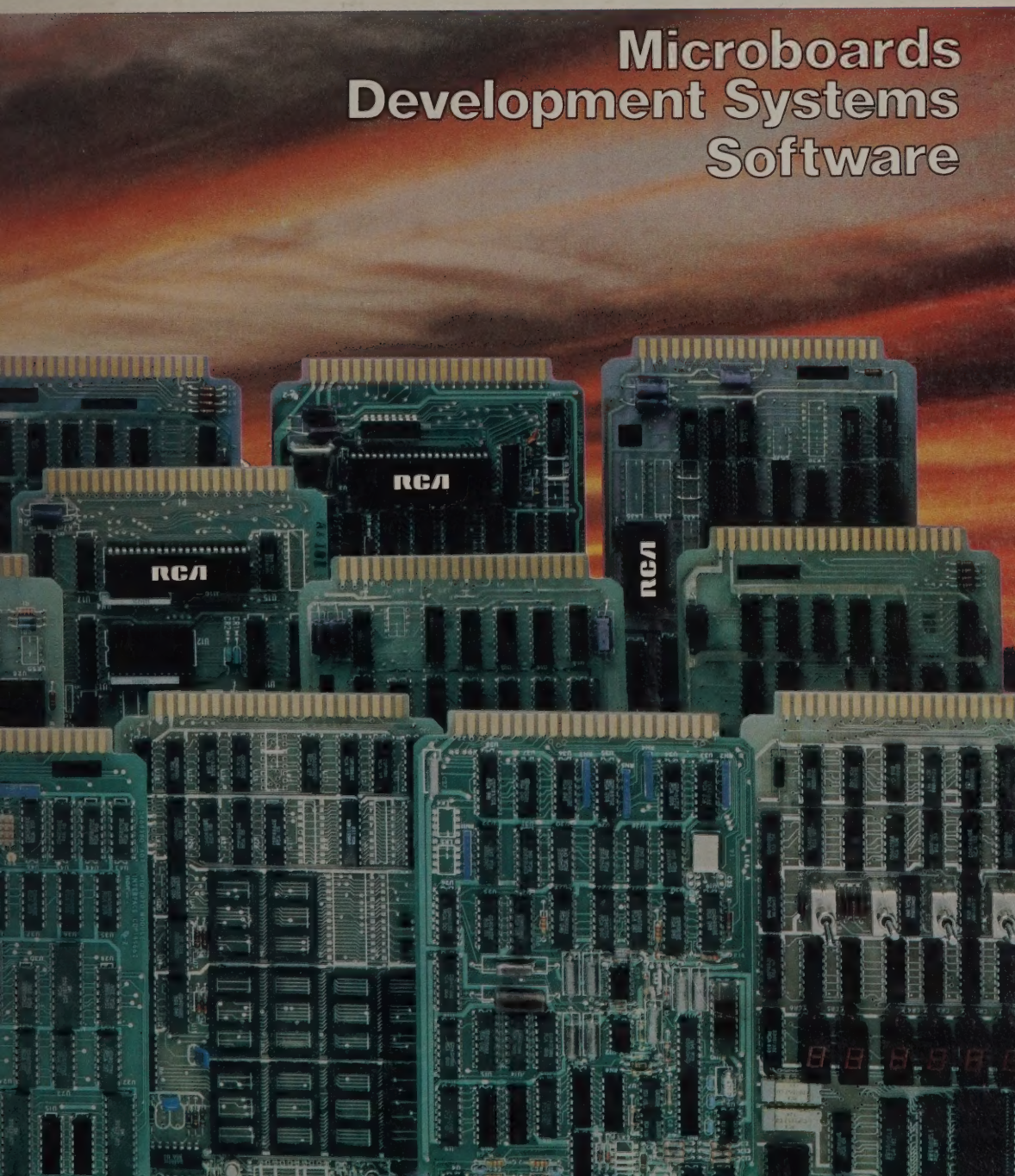
RCA Solid State

MICROSYSTEMS

Microboards
Development Systems
Software



RCA Microsystems

This DATABOOK contains complete technical information on the full line of Microboard computer systems and microprocessor development systems available from RCA Solid State Division. An Index to Products provides a complete listing of types.

The Index to Products is followed by a Product Classification Chart that groups systems according to product type and intended function.

Three separate data sections provide definitive ratings, performance specifications, and user information for (1) the CDP18S600 series of Microboard computer systems, (2) the CDP18S series of microprocessor development systems, and (3) software. Generally within each data section, the data pages for individual systems are grouped in alphanumerical sequence of type numbers. Because some devices are grouped together to show similarity of function, individual type numbers may be out of sequence. If you don't find the data on a specific type where you expect it to be, check the Index to Products.

The DATABOOK also contains selected application briefs and abstracts from application notes on RCA development systems.

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The data shown for some types are indicated as advance. **Advance data** are intended for engineering evaluation of types in the initial stages of design. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change of future manufacture of these devices. For current information on the status of advance programs, please contact your local RCA sales office.

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CDP18S622	Microboard 8K RAM, Battery-backup	181	MB-622
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CDP18S625	Microboard 8/16/32K ROM/PROM	195	MB-625
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CDP18S640A	Microboard Control and Display Module	252	MB-640A
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CDP18S659	Microboard Breadboard	429	MB-659
CDP18S660	Microboard Comb. Memory and I/O Module	361	MB-660
CDP18S661B	Microboard Video-Audio-Keyboard Interface (NTSC)	371	MB-661B
CDP18S661V3	Microboard Video-Audio-Keyboard Interface (PAL)	385	MB-661V3
CDP18S662	PIO Opto 22 Module Interface	394	MB-662
CDP18S663	Optically Isolated DC Interface	401	—
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CDP18S675	Microboard 5-Card Chassis	439	MB-675
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CDP18S694	Microboard Computer Development System (MCDS)	456	PD13

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CDP18S831	Micromonitor Operating System (MOPS)	507	PD31
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Industrial Chassis Series:			
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Product Classification Chart

Microboard Computers

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CDP18S604B	**1K RAM, 1/2/4K ROM/PROM**	**56**	**CDP18S609**	**1K RAM, 1/2/4K ROM/PROM**	**136**
CDP18S605	**2K RAM, 2/4K ROM/PROM**	**75**	**CDP18S610**	**2K RAM, 2/4K ROM/PROM**	**155**

Microboard Computer	Clock Frequency (MHz)	RAM (btyes)	ROM (bytes)	Serial I/O Port	I/O Lines	Ctr. Timer	Power* V	Power* (mA)	Temperature Range (°C)
CDP18S601 CPU: CDP1802	2	4K	4K (CDP1834) 4K (2708) 4K (2758) 8K (2716)	Software-driven; Q output; flag input	25: 20 programmable I/O (CDP1851); 4 flag inputs, 1 Q output	—	+5	10	−40 to +85
CDP18S602 CPU: CDP1802	Selectable: 2.4576, 1.2288, 0.6144, or 0.3072	2K	2K (CDP1834) 2K (2758) 4K (2716)	UART: 14 selectable baud rates from 50 to 19200 baud	21: 8 inputs (CDP1852), 8 outputs (CDP1852), 4 flag inputs, 1 Q output	—	+5	8	−40 to +85
CDP18S603 CPU: CDP1802	2	1K	4K (CDP1834) 4K (2708) 4K (2758) 8K (2716)	Software-driven; Q output; flag input	25: 20 programmable I/O (CDP1851); 4 flag inputs; 1 Q output	—	+5	7	−40 to +85
CDP18S604B CPU: CDP1802	2.097152	1K	1K (CDP1834) 1K (2758) 2K (2716) 4K (2732)	—	23: 8 inputs (CDP1852), 8 outputs (CDP1852), 4 flag inputs, 1 Q output 1 timer out 1 timer control	1	+5	4	−40 to +85
CDP18S605 CPU: CDP1802	Selectable: 2.4576, 1.2288, 0.6144, or 0.3072	2K	2K (CDP1834) 2K (2758) 4K (2716)	UART: 14 selectable baud rates from 50 to 19200 baud	—	—	+5	8	−40 to +85
CDP18S606 CPU: CDP1805	2	4K	4K (CDP1834) 4K (2708) 4K (2758) 8K (2716)	Software-driven; Q output; flag input	25: 20 programmable I/O (CDP1851); 4 flag inputs, 1 Q output	1	+5	10	−40 to +85
CDP18S607 CPU: CDP1805	Selectable: 2.4576, 1.2288, 0.6144, or 0.3072	2K	2K (CDP1834) 2K (2758) 4K (2716)	UART: 14 selectable baud rates from 50 to 19200 baud	21: 8 inputs (CDP1852) 8 outputs (CDP1852) 4 flag inputs, 1 Q output	1	+5	8	−40 to +85
CDP18S608 CPU: CDP1805	2	1K	4K (CDP1834) 4K (2708) 4K (2758) 8K (2716)	Software-driven; Q output; flag input	25: 20 programmable I/O (CDP1851); 4 flag inputs, 1 Q output	1	+5	7	−40 to +85
CDP18S609 CPU: CDP1805	2.097152	1K	1K (CDP1834) 1K (2758) 2K (2716) 4K (2732)	—	23: 8 inputs (CDP1852), 8 outputs (CDP1852), 4 flag inputs, 1 Q output 1 timer out 1 timer control	2	+5	4	−40 to +85
CDP18S610 CPU: CDP1805	Selectable: 2.4576, 1.2288, 0.6144, or 0.3072	2K	2K (CDP1834) 2K (2758) 4K (2716)	UART: 14 selectable baud rates from 50 to 19200 baud	—	1	+5	8	−40 to +85

*Typical values; running RS232C interface and no EPROM's. RS232C interface requires +12 to +15 V at 6 mA and −5 to −15V at 3 mA. Loop interface draws an additional 20 mA from the +5 V supply. **CDP18S604B and CDP18S609 do not have RS232C or 20-mA interface.**

Product Classification Chart

Microboard Memories

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CDP18S621	Microboard 16-Kilobyte RAM	176
CDP18S622	Microboard 8-Kilobyte Battery-Backup RAM	181
CDP18S623A	Microboard 8-Kilobyte RAM	190
CDP18S625	Microboard 8/16/32-Kilobyte ROM/PROM	195
CDP18S626	Microboard 32/64-Kilobyte EPROM/ROM/RAM	207
CDP18S627	Microboard 4-Kilobyte EPROM	229
CDP18S629	Microboard 32-Kilobyte RAM	237

Microboard	Memory Type	Memory Bytes	Data Rentention	Power* (V)	Power* (mA)	Temperature Range (°C)
CDP18S620	Static CMOS RAM	4 K	—	5	4	-40 to 85
CDP18S621	Static CMOS RAM	16 K	—	5	6	-40 to 85
CDP18S622	Static CMOS RAM	8 K	96 h	5	13[1]	-40 to 70
CDP18S623A	Static CMOS RAM	8 K	—	5	6	-40 to 85
CDP18S625	ROM/PROM	8/16/32 K	Permanent	5	10[2]	-40 to 85
CDP18S626	ROM/EPROM, RAM	32/64 K	Permanent (ROM's)	5	100[3]	-40 to 70[6]
CDP18S627	CMOS EPROM	4 K	Permanent	5	8[4]	-40 to 85
CDP18S629	Static CMOS RAM	32 K	—	5	27[5]	-40 to 85

*Typical
[1]Operating current with batteries on trickle charge
[2]Populated with eight CDP1834 CMOS ROM's
[3]Populated with sixteen 2716 EPROM's
[4]Populated with sixteen CDP18U42 CMOS EPROM's
[5]Populated with sixteen 6116 CMOS RAM's
[6]For operation at full temperature range the user should select ROM's or RAM's having suitable temperature specifications

Microboard Expansion Modules

		Page
CDP18S661B	Microboard Video-Audio-Keyboard Interface (NTSC)	371
CDP18S661V3	Microboard Video-Audio-Keyboard Interface (PAL)	385

Microboard	Video Signal	Dot Matrix	Page Memory Capacity	Page Memory Address	Character Memory Capacity	Character Memory Address	I/O Addressing	Power (V)	Power (mA)
CDP18S661B	NTSC	6 x 8	1 K	F800 through FBFF	1 K	F400 through F7FF	Two-level group select: 80-F0, link selectable	5	27[1]
CDP18S661V3	PAL	6 x 9	1 K	F800 through FBFF	1 K	F400 through F7FF	Two-level group select: 80-F0 link selectable	5	10[1]

[1]Typical; not including audio output

Product Classification Chart

Digital I/O Expansion Modules

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CDP18S640A	Microboard Control and Display Module (256-byte RAM; 4 control switches; 6-digit hex displays; 6 LED indicators; Utility runs software UART)	252
CDP18S640A1	Microboard Control and Display Module (256-byte RAM; 4 control switches; 6-digit hex displays; 6 LED indicators UART terminal interface; Utility runs hardware UART)	261
CDP18S641	Microboard UART Interface	270
CDP18S646	Microboard Parallel I/O Module	308
CDP18S650	Microboard Counter/Timer	342
CDP18S651	Microboard Floppy Disk Interface	343
CDP18S652	Microboard Memory and Tape I/O	345
CDP18S653V1, V2	Direct-Connect Auto Modems (Bell Compatible)	346
CDP18S653V3, V4	Direct-Connect Auto Modems (CCITT Compatible)	353
CDP18S660	Microboard Combination Memory and I/O Module	361
CDP18S662	PIO Opto 22 Module Interface	394
CDP18S663	Opto-Isolated PIO Module	401

Microboard	Serial I/O Port	I/O Lines	Memory RAM (bytes)	Memory ROM (bytes)	Power* (V)	Power* (mA)	Temperature Range (°C)
CDP18S640A	—	20 Lines Interface for Microterminal CDP18S021	256	1K UT60	5	350	0 to 70
CDP18S640A1	—	20 Lines Interface for Microterminal CDP18S021	256	1K UT61	5	350	0 to 70
CDP18S641	UART: switch selectable 110, 300, 1200, 4800, 9600, 19200 baud	—	—	—	5	2.01[1]	-40 to 85
CDP18S646	—	Three 8-bit output ports; one 8-bit input port	—	—	5	3[2]	-40 to 85
CDP18S650	—	8 Counter-Timer Modules; I/O lines on 36-pin header	—	—	5	10	-40 to 85
CDP18S651	—	Handles most floppy disk drives; Shugart Interface	—	—	+5 -5	250 3	0 to 70
CDP18S652	2-cassette tape I/O ports	—	1 K	24 K	5	10	0 to 70
CDP18S653V1, V3 CDP18S653V2, V4	300-baud modem 1200-baud modem	—	—	—	5,12	12,34	-40 to 85
CDP18S660	—	40 programmable I/O (2 CDP1851's) input, output, or bidirectional	2 K	8 K	5	8	-40 to 85
CDP18S662	—	24 bidirectional parallel Opto 22 interface	—	—	5	10	-40 to 85
CDP18S663	—	8 input, 8 output optically isolated DC lines	—	—	5	85	-40 to 85

*Typical
[1]Plus additional power required by data terminal
[2]Disk drive and printer connected and reset.

Product Classification Chart

Microboard A/D and D/A Converters

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CDP18S643A	Microboard A/D Converter	283	CDP18S654	Microboard A/D and D/A Converter (8-bit unipolar)	293
CDP18S644	Microboard A/D and D/A Converter (8-bit bipolar)	293	CDP18S657	Microboard D/A Converter (8-bit unipolar)	319
CDP18S647	Microboard D/A Converter (8-bit bipolar)	319	CDP18S658	Microboard A/D Converter (8-bit unipolar)	330

Microboard	Version	Resolution (bits)	No. of Channels	I/O Voltage Ranges (V)	Accuracy at 25°C[5] (least significant bits) Linearity	Gain	Offset	Settling (S) or Conversion (C) Time (μs)	Power[6] (V)	(mA)	Temperature Range (°C)
CDP18S642	D/A[2]	12/8	2	±2.5, ±5, or ± 10 0 to 2.5, 5, 10	±½	±½	±½	5 (S)	+5 +15 −15	26 50 50	−25 to 85
CDP18S643A	A/D[1]	12/8	8/16	±2.5, ±5, or ±10 0 to 2.5, 5, 10	±½	±½	±½	105/275 (C)	+5 +15 −15	85 50 50	−25 to 85
CDP18S644	A/D[1] D/A[2]	8 8	8/16 2	±2.5, or 0 to 2.5 ±2.5, or 0 to 2.5	±¾ ±½	±¾ ±½	±¾ ±½	215 (C) 15 (S)	+5	50	−40 to 85
CDP18S647	D/A[2]	8	2	±2.5, or 0 to 2.5	±½	±½	±½	15 (S)	+5	22	−40 to 85
CDP18S648	A/D[1]	8	8/16	±2.5, or 0 to 2.5	±¾	±¾	±¾	215 (C)	+5	40	−40 to 85
CDP18S654	A/D[3] D/A[4]	8 8	8/16 2	0 to 2.5 0 to 2.5	±¾ ±½	±¾ ±½	±¾ ±½	215 (C) 15 (S)	+5	15	−40 to 85
CDP18S657	D/A[4]	8	2	0 to 2.5	±½	±½	±½	15 (S)	+5	9	−40 to 85
CDP18S658	A/D[3]	8	8/16	0 to 2.5	±¾	±¾	±¾	215 (C)	+5	13	−40 to 85

[6]Typical [1]Binary or unipolar input [2]Binary or unipolar out [3]Unipolar input [4]Unipolar output
[5]Microboards provide offset and gain adjustments permitting the user to null total system error

Product Classification Chart

Microboard Industrial Chassis and Accessories

		Page
Chassis		
MSI 8000 series	Backplane with connectors	402
MSI 800 series	Standard industrial chassis	402
MSI 8800 series	Deluxe industrial chassis	402
Accessories		
MSIA 0100 series	Solid top and bottom covers	402
MSIA 0200 series	Perforated top and bottom covers	402
MSIA 0300 series	Solid rear panels	402
MSIA 0400 series	Front panel guards	402
MSIA 06	Mounting angle brackets	402
MSIA 07	End bezels (handles)	402
MSIA 08	Four-card front panel	402
MSIA 10	Cable conduit	402
MSIA 11	Card extractor	402
Modules		
MSIM 20	Microboard I/O module card (mounts up to 8 industry standard optically isolated power modules)	414
MSIM 40, E MSIM 41, E	Industrial microboard power supplies (includes power cord, circuit breaker, switch, and power-on light)	426
MSIM 50	Micro floppy disk drive module (contains 2 disk drives having storage capacity of 315 kilobytes each)	427

No. of Slots	Standard Industrial Chassis	Deluxe Industrial Chassis	Backplanes With Connector
4	MSI 804	MSI 8804	MSI 8004
8	MSI 808	MSI 8808	MSI 8008
12	MSI 812	MSI 8812	MSI 8012
16	MSI 816	MSI 8816	MSI 8016
20	MSI 820	MSI 8820	MSI 8020
24	MSI 824	MSI 8824	MSI 8024
25	MSI 825	MSI 8825	MSI 8025
Features Include:	• Rugged steel and aluminum chassis • 44-pin, 0.156-inch pitch card connectors mounted on 6-inch centers • Full-length card guides • Card extractor rail • Stick-on rubber feet • Power-supply connector	• All features of standard chassis plus — • Slide-in solid top and bottom covers • Screw-fastened front and rear panels • Standoff mounted see-through front panel guard • Two carrying handle/end bezels • Two mounting angle brackets	• Bare microboard backplane/connector assembly from Standard chassis with power-supply connector

Product Classification Chart

Other Chassis, Accessories, and Prototyping Systems

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CDP18S023	Power Converter (110 V ac, 60 Hz to 5 V dc 600 mA, reg.)	428
CDP18S023V3	Power Converter (220 V ac, 50 Hz to 5 V dc 600 mA, reg.)	428
CDP18S659	Microboard Breadboard	429
CDP18S670	Microboard 25-Card Chassis with Case and Power Supply	431
CDP18S675	Microboard 5-Card Chassis	439
CDP18S676	Microboard 5-Card Chassis with Case	439
CDP18S691	Microboard Prototyping System (CDP18S601, CDP18S640, CDP18S659, Chassis, Cables, Utility Program)	442
CDP18S692	Microboard Prototyping System (CDP18S602, CDP18S640A1, CDP18S659, Chassis, Cables, Utility Program)	448

Microboard Computer Development Systems (MCDS)

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CDP18S693	MCDS with Floating-Point BASIC3	456
CDP18S694	MCDS with Floating-Point BASIC3 Resident Assembler/Editor, PROM Programmer	456
CDP18S695	MCDS with Floating-Point BASIC3 Resident Assembler/Editor, PROM Programmer, Color Enhanced	464

MCDS Systems	CDP18S 693	694	695
System Includes:			
• CDP18S601 Computer	X	X	X
• CDP18S652 Memory and Tape I/O	X	X	X
• CDP18S661 Video/Audio Keyboard Interface			X
• Five-Card Chassis and Case	X	X	X
• ROM Monitor Program (2K)	X	X	X
• ROM-based BASIC3 Interpreter (12K) — development version	X	X	X
• Cassette I/O Unit for Memory Storage	X		
• Dual Cassette I/O Unit for Memory Storage		X	X
• Resident ROM-based (6K) ASSEMBLER/EDITOR program		X	X
• CDP18S480 PROM Programmer Module		X	X
• VP601 Keyboard			X
• 12-inch Color Monitor			X
System Features:			
• Low Cost	X	X	X
• Resident ROM-based ASSEMBLER/EDITOR program		X	X
• Line editing	X	X	X
• Powerful 1802 I/O constructs in BASIC	X	X	X
• Full BASIC3 with floating point	X	X	X
• Cold/warm start	X	X	X
• 6656 Multiple character variables (256x26)	X	X	X
• Resident ROM Monitor program	X	X	X
• Economical memory storage through audio tapes	X	X	X
• Terminal interface: 20-mA or RS232C serial with baud rates to 1200	X	X	X
• Expandable by use of Microboard modules	X	X	X
• PROM programmer software on cassette		X	X
• Color video display			X

Power Requirements:

CDP18S693V1 — 110 V, 60 Hz
CDP18S694V1 — 110 V, 60 Hz
CDP18S695V1 — 110 V, 60 Hz
CDP18S693V3 — 220 V, 50 Hz
CDP18S694V3 — 220 V, 50 Hz

Product Classification Chart

1800 Development Systems

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CDP18S005	Development System CDS II	469
CDP18S007V1	DOS Development System 110 V, 60 Hz (Includes Floppy Disk System)	469
CDP18S007V3	DOS Development System 220 V, 50 Hz (Includes Floppy Disk System)	469
CDP18S008V1	Development System CDS IV 110 V, 60 Hz with Integral CRT Display, Keyboard, Central Processor, Full-Screen Editing	472
CDP18S008V3	Development System CDS IV, 220 V, 50 Hz with Integral CRT Display, Keyboard, Central Processor, Full-Screen Editing	472
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Features and Functional Classifications

The RCA CDP18S600 Series offers a line of single-board computers plus a variety of expansion memory and I/O boards and accessory hardware. These boards may be combined to provide customized microcomputer systems for specific applications. RCA offers designers low-power CMOS computer boards engineered and tested to reduce the time required for the user to develop the over-all system. These ready-to-use microboard modules provide the following significant advantages.

- **Simple to Use**—Simply select the 4.5 x 7.5-inch Microboard modules your system needs, plug them on to the Microboard 5- or 25-card chassis with COSMAC Microboard Universal Backplane, and add a milliwatt power supply. You are ready to begin the development of the software for your application. No hand-wired breadboards, no hardware headaches, no design delays.

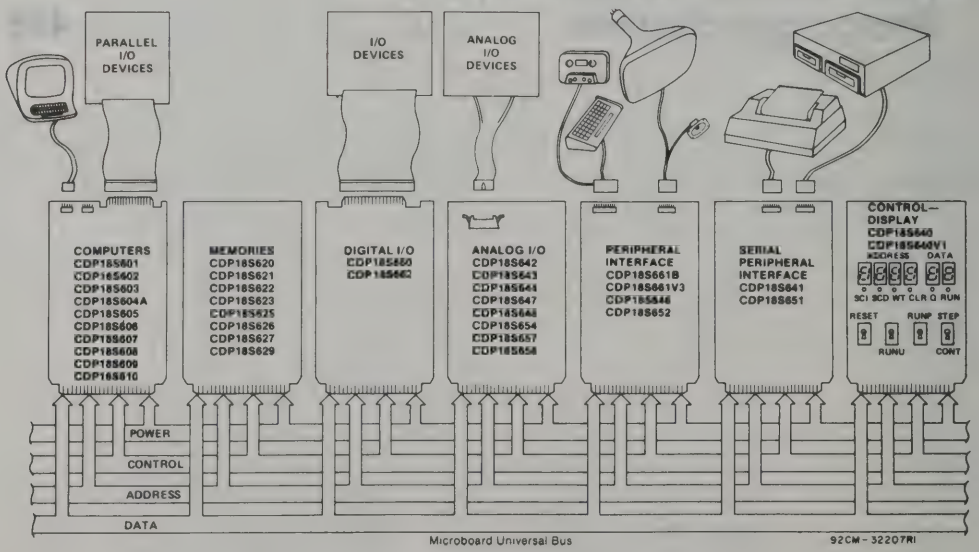
- **Low-Power Operation**—Utilizing all CMOS components, your RCA COSMAC Microboard system can be powered from a small supply, a wall supply, or even a battery. The integral battery option of the Microboard 8K RAM can be used to power the entire system.

- **Low-Cost Power Supply**—The low power requirements of the Microboard modules coupled with their wide operating-range capabilities allow use of low-cost power supplies having extended regulation limits. No longer does the power supply have to be bigger, bulkier, and heavier than the entire system. And you eliminate cooling fans along with associated reliability hazards.

- **Easy to Modify**—With the COSMAC Microboard Universal Backplane, any Microboard module works in any location. Use the broad selection of readily interchangeable Microboard modules. Simply exchange or add modules to match your changing design requirements. Lots of flexibility without hardware design headaches.

- **Excellent Noise Immunity**—CMOS technology provides reliable operation in high-noise process-control, automotive, and production-monitoring environments. No ground plane or extra decoupling capacitors needed.

- **Development System Compatibility**—All Microboard modules are designed to plug directly into the COSMAC Development Systems to facilitate rapid hardware and software development. The RCA COSMAC DOS Development System provides Editor, Assembler (Level I, II, and MACRO), Disk Operating System, Utility, and many other useful programs for the neophyte-to-expert software designer. And RCA provides ample technical literature and field engineering support.



Block diagram illustrating interconnection of Microboard modules.

CDP18S601

RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP18S601 is a versatile computer system on a single 4.5×7.5 inch card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S601 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and special requirements of his specific application. The CDP18S601 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC CDOS Development System CDP18S007 facilitating prototype design and the debugging of both hardware and software.

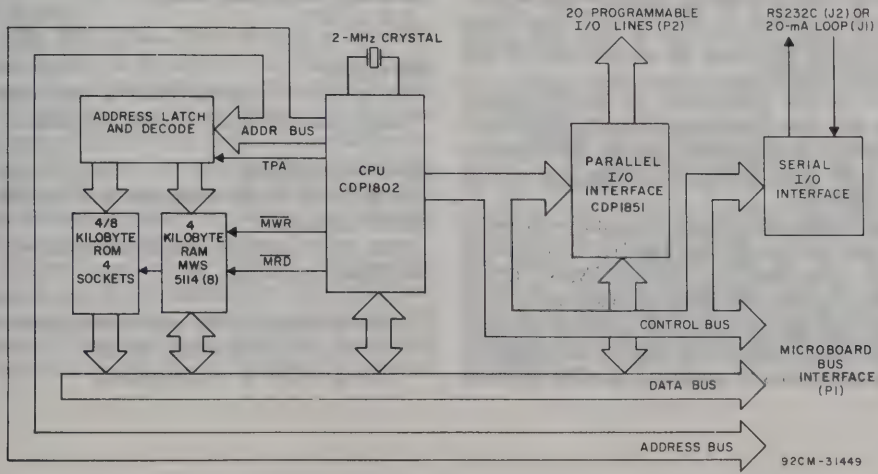
Component Features

Central Processing Unit. The central processor for the CDP18S601 Microboard Computer is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Inter-

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Current required—10 mA (typ.)†
- High noise immunity
- 2-MHz crystal clock
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 4 kilobytes of read/write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Flexible memory and I/O expansion
- 20 programmable parallel I/O lines
- 4 flag inputs
- Q serial data output
- RS232C or 20-mA serial I/O
- 65,536-byte memory space
- 44-pin system interface
- Temperature range −0°C to 70°C
- Small board size—4.5×7.5 inches

†With CMOS ROM and RS232C serial interface.



Block diagram of RCA COSMAC Microboard Computer CDP18S601.

CDP18S601

rupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. By means of eight MWS5114 RAM's, the CDP18S601 provides 4 kilobytes of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S601 provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

Application

The COSMAC Microboard Computer CDP18S601 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board. It may also be operated in conjunction with other Microboard System components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S601 Microboard Computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC CDOS Development System CDP18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

Specifications

Memory Capacity

On-board RAM: 4 kilobytes

On-board ROM/EPROM: 4 sockets for up to 8 kilobytes.

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map

On-board RAM: Any even 4-kilobyte block.

On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity

Parallel: 20 lines each programmable as input, output, or bidirectional.

Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.

Operating Temperature Range

0 °C to 70 °C.

Dimensions

4.5 inches × 7.5 inches (114.3 × 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

With CMOS ROM's, with RS232C: +5 V at 10 mA, typical operating

With CMOS ROM's and 20-mA loop: +5 V at 30 mA, typical operating

Optional voltages used only for RS232C interface:

+12 to +15 V at 8 mA, typical

−5 to −15 V at 8 mA, typical

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pin.

Clock

CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard Computer CDP18S601 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

DB7 through DB0—Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2—Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high, $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$—Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S601 uses EF1 and EF2, conditioned by the secondary I/O address, to test the READY state of I/O ports A and B. The serial data interface input is presented directly on EF4 or EF3 chosen by link LK36. I/O devices using the INT line may make use of the EF lines to identify the device. They may also be used to indicate priority or status.

INT—Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

$\overline{DMAI}$, $\overline{DMAO}$—Taken directly to the CPU pins and not utilized by the CDP18S601, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0—State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB—Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0—Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S601 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

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$\overline{\text{MWR}}$—A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$—A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q—A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. The CDP18S601 may use Q as a serial data output to the RS232C and 20-mA data terminal drivers. It is also available for other uses through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT—A 2-MHz square-wave clock provided for general use. It is derived from the crystal-controlled oscillator in the CPU.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$—Two control inputs to the CPU which determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA IN requests then load memory starting from location zero for as many bytes as there are DMA IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to $\overline{\text{CLEAR}}$.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU—Run Utility Software. A signal supplied to the CDP18S601 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The RAM on the CDP18S601 is 4 kilobytes of contiguous memory. The high-order four bits of memory address are latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy any even 4-kilobyte block in the memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

Table I—4-Kilobyte Link Connections

4-Kilobyte Address Space	Link LK10, LK11, or LK22 Pin Connections
0000 - 0FFF	1:16, 5:12
1000 - 1FFF	1:16, 6:11
2000 - 2FFF	1:16, 7:10
3000 - 3FFF	1:16, 8:9
4000 - 4FFF	2:15, 5:12
5000 - 5FFF	2:15, 6:11
6000 - 6FFF	2:15, 7:10
7000 - 7FFF	2:15, 8:9
8000 - 8FFF	3:14, 5:12
9000 - 9FFF	3:14, 6:11
A000 - AFFF	3:14, 7:10
B000 - BFFF	3:14, 8:9
C000 - CFFF	4:13, 5:12
D000 - DFFF	4:13, 6:11
E000 - EFFF	4:13, 7:10
F000 - FFFF	4:13, 8:9

LINK 11 is associated with the 4-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.

ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

Two types of links are provided and must be made up by the user to suit the particular ROM configuration selected. The first link type is for accommodating the type of ROM selected (CDP1834, 2708, 2758, or 2716. The second link type is for selecting the memory address space to be occupied by the ROM.

Link LK4 is an 18-pin dual-in-line arrangement with preprinted links to accommodate the 2716 ROM's.Table II gives the connections required for each ROM type.

Links LK10 and LK22 are 16-pin dual-in-line arrangements with no preprinted links. A DIP switch may be installed if frequent address changes are expected. Link LK10 provides the high-order four address bits decoded so that two links or jumpers place sockets XU24 and XU25 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK22 does the same for sockets XU26 and XU27. See Table I for address map and link connections.

To avoid having floating inputs to the gates, both links LK10 and LK22 should always have two jumpers. For example, if sockets XU26 and XU27 are unused, LK22 may be jumpered the same as LK10. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

In instances where no ROM sockets are used, it may be desirable to jumper links LK10, LK11,and LK12 identically so that the unused ROM space overlays the RAM space. In this way, no memory space is taken from the system's 64-kilobyte space for the unused ROM sockets.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK10 and LK22 should be jumpered identically in accordance with Table I. Then, the ROM's should be installed in sockets XU25, XU27, XU24, and XU26, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK10 and LK22 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then, socket XU25 is the low 2 kilobytes and socket XU24 is the high 2 kilobytes of the 4-kilobyte block as set in LK10. Similarly, socket XU27 is the low 2 kilobytes and socket XU26 is the high 2 kilobytes of the 4-kilobyte block set in LK22.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with two-kilobyte ROM's type 2716. If all links are set up for the 2-kilobyte ROM's as shown in Table II for LK4, and LK10 and LK22 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU25 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in

Table II - ROM Type Selection Links

Link LK4 Pins	ROM Type CDP1834	2708	2758	2716*
1:18	X	OPEN	SHORTED	SHORTED
2:17	X	SHORTED	OPEN	OPEN
3:16	SHORTED	SHORTED	SHORTED	OPEN
4:15	OPEN	OPEN	OPEN	SHORTED
5:14	OPEN	OPEN	OPEN	SHORTED
6:13	SHORTED	SHORTED	SHORTED	OPEN
7:12	X	SHORTED	OPEN	OPEN
8:11	X	OPEN	OPEN	SHORTED
9:10	X	OPEN	SHORTED	OPEN

*X = don't care; Link LK4 is prewired to accept 2716.

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socket XU24, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU24 or socket XU25 while the other is occupied by a 1-kilobyte ROM. Socket XU27 (low 2 kilobytes) and socket XU26 (high 2 kilobytes) may be used in the same manner.

I/O Operation

Serial I/O Interface. Serial data output is generated by the Q line from the CPU. Thus, software using the SET Q and RESET Q instructions generates data rate and format. Serial data input is presented to either EF3 or EF4, selectable by links as shown in Table III. The software uses the test branch instructions to decode incoming data.

Table III—Link Table for Serial Data In

Link LK36	Function
7:10	Data to EF3
8:9	Data to EF4

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2 respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire in the C5 holes. RS232C data terminals require that +12 volts be available on pin 20 of the backplane and -5 volts be available on pin 11.

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S601 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The CDP18S601 uses bit three as the group select; that is, the group number $(08)_{16}$ or $(0000\ 1000)_2$ is transmitted by the 61 output instruction to select the programmable I/O on board.

In general, although Interrupt is not gated by group select, External Flags are gated by the appropriate group select. The serial interface on the CDP18S601, however, uses either EF3 or EF4 with no gating by group number. Therefore, when the serial interface is wired for use, EF3 or EF4, whichever was chosen, is not generally available for other devices.

Parallel I/O Interface. The parallel I/O interface consists of 20 lines provided on connector P2. These 20 lines are generated by the CDP1851 Programmable I/O Interface and may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides the Q line, EF1 through EF4, CLEAR, three different voltages, and a logic ground.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device.

The CDP1851 is assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data = 08 is required before read, write, or control I/O may be performed.

Signal ARDY conditioned by the group select generates EF1; BRDY and group select generates EF2. Link LK41, pins A and B may be jumpered if interrupt-driven software is to be used. Then, INTA or INTB generates INT unconditionally.

Once the group select is accomplished, N1 and N2 are used to address the CDP1851. The following read and write instructions are used to access data, status, and command registers.

62—Write to control register
64—Write to Port A data register (if A is an output)
66—Write to Port B data register (if B is an output)
6A—Read status register
6C—Read Port A data register (if A is an input)
6E—Read Port B data register (if B is an input)

Using the READY Lines for Data Synchronization. The Port A and Port B RDY lines are presented to the CPU EF1 and EF2 lines when the group select is set. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU. Note that there is a logic reversal: when RDY is true, the EF is false. Because of the logic reversal and because the event of interest is RDY going false, the EF true test is used. A test for ARDY might use the B1 instruction (34) which would take the branch if ARDY were false.

When a port designated as an **output** port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true), and load the next output byte. When a port is designated as an **input** port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and then reads the input byte. **In this case, a dummy read after reset is necessary to raise the first RDY.**

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the INTERRUPT Line for Data Synchronization. If link LK41, A:B is jumpered, INTA or INTB generates INT to the CPU. INT is not conditioned by the group select.INT is set by the remote device sending STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table IV summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the group select 08, and then, either testing the RDY lines or reading the status byte. The low-order two bits of the status byte are: bit 0 = INTB; bit 1 = INTA.

Bidirectional Mode. Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, ARDY and ASTB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and BSTB becomes A OUTPUT STB. Each of the eight lines AD0—AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that output data is gated into AD0—AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode. Both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write

Table IV—READY and INTERRUPT Actions for Input and Output Modes.

		Output Port	Input Port
READY	Set By	Loading Data	Reading Data
	Reset by	STB leading edge	STB leading edge
INTERRUPT	Set by	STB trailing edge	STB trailing edge
	Reset by	Loading Data	Reading Data

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control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development Systems CDP18S005 or CDP18S007

Replacement of the CDS CPU Module CDP18S102 with the RCA COSMAC Microboard Computer CDP18S601 requires some link changes on the CDP18S601 and wiring changes on the CDS backplane. These changes are:

LK 43—Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D. See Table V.

Table V-Changes on Link LK43 for Installation of CDP18S601 in COSMAC Development System CDP18S005.

LK43	A:B	C:D	A:D	B:C
Microboard	*Closed	*Closed	Open	Open
CDS	Open	Open	Closed	Closed

*Preprinted links

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK 36—Serial Data In to external flag lines. In the CDS II, if the Terminal Interface Module CDP18S507 is not retained, connect pins 8:9 for EF4 to make the CDP18S601 the operator's terminal interface. If the CDP18S507 is retained, EF3 may be used for another serial interface purpose by connecting pins 7:10. In the CDS III, the UART module in location 14 is the operator's terminal interface and pins 7:10 and 8:9 may be left open.

LK 36—RNU to start ROM's at address 8000. Cut the wire jumper in pins 5:12. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed. This wire should be removed when the CPU Module CDP18S102 is re-installed. See Table VI.

Table VI-Changes on Link LK36 for Installation of CDP18S601 in COSMAC Development System CDP18S005.

LK36	RNU 5:12	RNU 6:11	EF3 7:10	EF4 8:9
Microboard	¢Closed	Open	Open	¢Closed
CDS	Open	Closed	Open	Closed@

¢Wire jumpers installed
@ Assumes the CDP18S601 serial interface is to be the operator terminal interface.

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LK 10, 11, and 22—Set up as previously described for the memory address desired, taking care that the CDS memories are not assigned to overlap the assignment of the CDP18S601 Microboard Computer.

Table VII summarizes the required CDS backplane wiring changes.

Table VII–Summary of Backplane Wiring Additions Needed When the CDP18S601 is Installed in the COSMAC Development System CDP18S005.

From		To		
Slot	**Pin**	**Slot**	**Pin**	**Function**
12	X	13	20	-12 V
12	11	14	11	-5 V
12	12	10	D	RNU-P†

†This connection should be removed when the CDP18S102 is reinstalled.

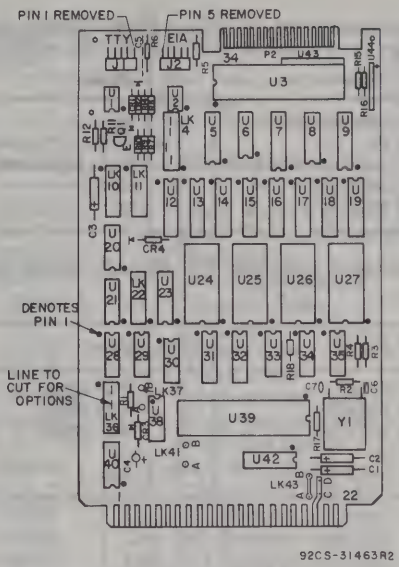
Parts List

C1, C2, C3 = 15 μF, 20 V
C4 = 1.5 μF, 35 V
C6=39 pF
C7=10 pF

CR1, CR2, CR3, CR4 = 1N270
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP86016-1, keying plug — AMP 87077-1, or equivalent)

P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalents

Q1 = 2N5139
R1 = 100 kΩ, ¼ W, 5%
R2 = 22 MΩ, ¼ W, 5%
R3, R4 = 22 kΩ, ¼ W, 5%
R5 = 3 kΩ, ¼ W, 5%
R6, R14 = 1 kΩ, ¼ W, 5%
R7 = 11 kΩ, ¼ W, 5%
R8 = 4.3 kΩ, ¼ W, 5%
R9 = 130 kΩ, ¼ W, 5%
R10 = 10 kΩ, ¼ W, 5%
R11 = 2.7 kΩ, ¼ W, 5%
R12 = 100 Ω, ¼ W, 5%
R15-R18 = 22 kΩ, ¼ W, 5%
U1 = CA3160
U2 = CA3140
U3 = CDP1851CE
U5, U8 = CDP1856CE
U6 = CD4069BE
U7 = CDP1867CE
U9 = CDP1866CE
U12–U19 = MWS5114
U20, U38 = resistor module, 22 kΩ, 14 pin
U21 = CD4001BE
U23 = CDP1858CE
U28, U29 = CD4012BE
U30 = CD4016BE
U31, U32 = CD4050BE
U33 = CD4025BE
U34 = CD4013BE
U35 = CD4023UBE
U39 = CDP1805CE
U40 = CD4093BE
U42 = resistor module, 22 kΩ, 16 pin
U43 = resistor module SIP, 22 kΩ, 10-pin
U44 = resistor, module SIP, 8-pin
XU3, XU39 = 40-pin socket
XU24-XU27 = 24-pin socket
Y1 = 2.00-MHz crystal



Layout diagram of RCA COSMAC Microboard Computer CDP18S601.

Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+5V
31	EF2-N	32	−5V/−15V
33	EF1-N	34	+12V/+15V

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Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

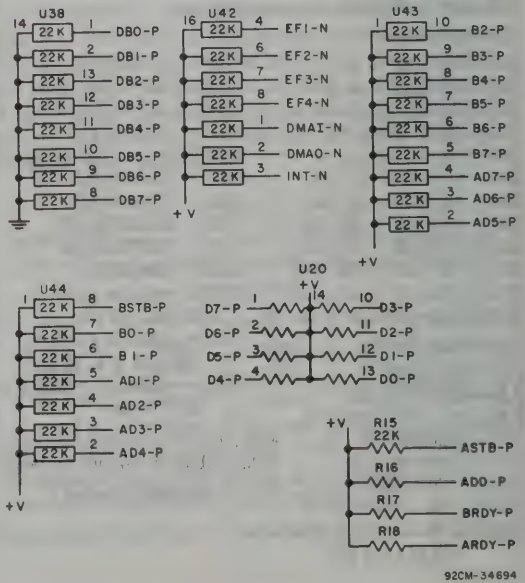
Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

Table VIII–List of Links and Their Functions

LK4	ROM Type Selection
*1:18	ROM Type 2758, 2716
2:17	ROM Type 2708
3:16	ROM Type 2758, 2708, or CDP1834
*4:15	ROM Type 2716
*5:14	ROM Type 2716
6:13	ROM Type 2758, 2708, or CDP1834
7:12	ROM Type 2708
*8:11	ROM Type 2716
9:10	ROM Type 2758
LK10	**ROM Decoding for XU24 and XU25**
*1:16	$\overline{A15}\cdot\overline{A14}$
2:15	$\overline{A15}\cdot A14$
3:14	$A15\cdot\overline{A14}$
4:13	$A15\cdot A14$
*5:12	$\overline{A13}\cdot\overline{A12}$
6:11	$\overline{A13}\cdot A12$
7:10	$A13\cdot\overline{A12}$
8:9	$A13\cdot A12$
LK11	**RAM Decoding**
1:16	$\overline{A15}\cdot\overline{A14}$
*2:15	$\overline{A15}\cdot A14$
3:14	$A15\cdot\overline{A14}$
4:13	$A15\cdot A14$
*5:12	$\overline{A13}\cdot\overline{A12}$
6:11	$\overline{A13}\cdot A12$
7:10	$A13\cdot\overline{A12}$
8:9	$A13\cdot A12$

LK22	ROM Decoding for XU26 and XU27
*1:16	$\overline{A15}\cdot\overline{A14}$
2:15	$\overline{A15}\cdot A14$
3:14	$A15\cdot\overline{A14}$
4:13	$A15\cdot A14$
5:12	$\overline{A13}\cdot\overline{A12}$
*6:11	$\overline{A13}\cdot A12$
7:10	$A13\cdot\overline{A12}$
8:9	$A13\cdot A12$
LK36	
1:16	Not applicable to CDP1802 or CDP1805
*2:15	CLEAR-N
3:14	Not applicable to CDP1802 or CDP1805
*4:13	WAIT-N
¢5:12	RNU-P from P1-3
6:11	RNU-P from P1-12 (CDS installation only)
7:10	EF3 for serial interface in
¢8:9	EF4 for serial interface in
LK37	
*A:B	+5 V V_{DD} to CDP1802
LK41	
A:B	Interrupt from PIO
LK43	
*A:B	Microboard system installation (EF4-N)
*C:D	Microboard system installation (+12 V)
A:D	CDS installation (+12 V)
B:C	CDS installation (EF4-N)

*Preprinted links
¢Wire jumpers installed



Pull-down and pull-up resistors.

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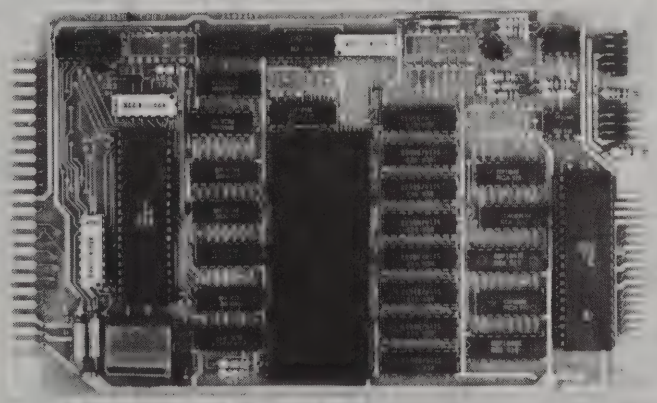
Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility
D	DB1-P	In/Out	Data Bus	4	INT-P	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Control
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Control
M	A0-P	Out	Multiplexed Address Bus	11	−5 V/−15 V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V	In	+5 volts dc	21	+5 V	In	+5 volts dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground



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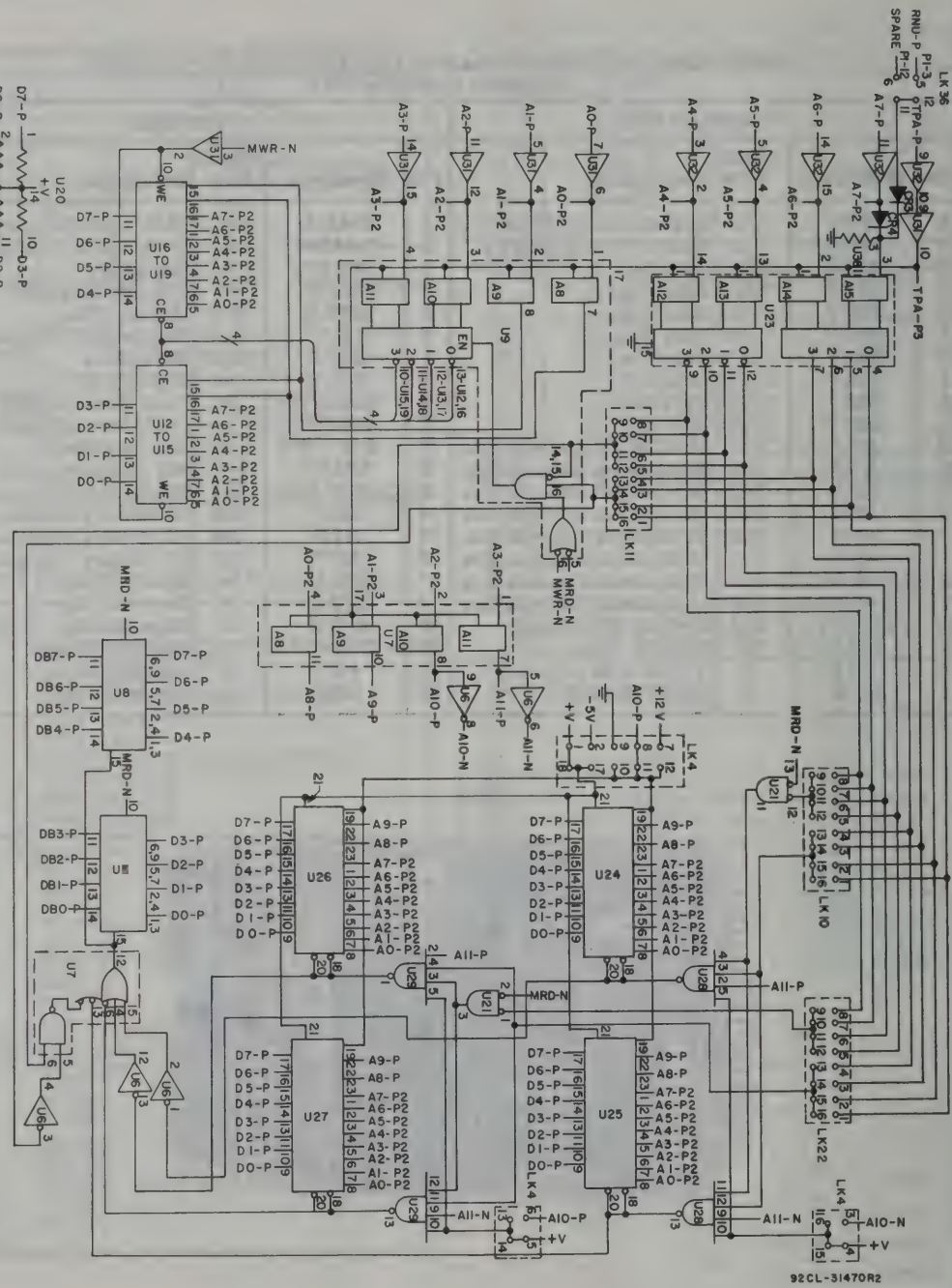

Logic diagram of Microboard Computer CDP18S601 - memory portions.

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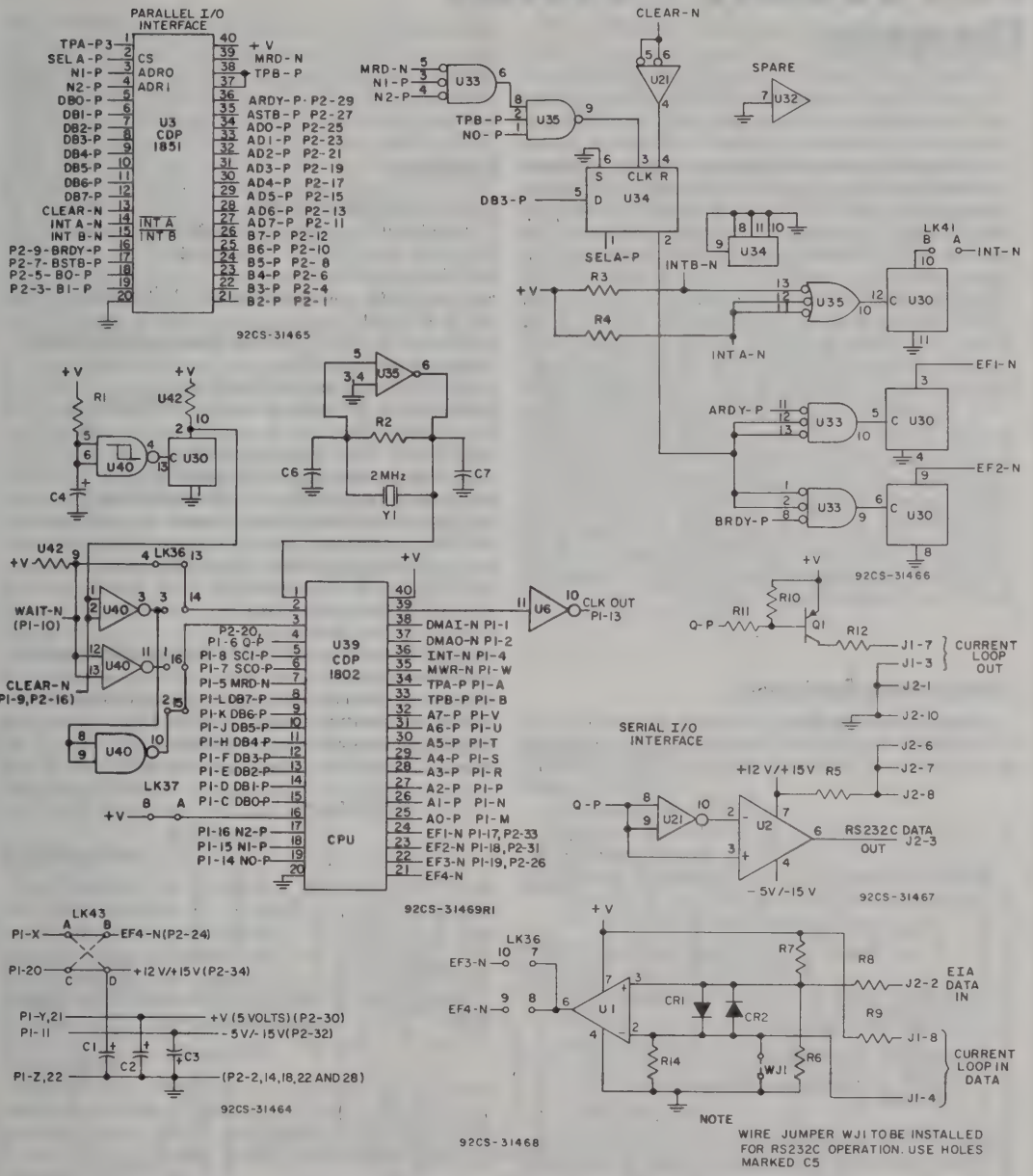

Logic diagram of Microboard Computer CDP18S601 - CPU and interface portions.

CDP18S602
RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP-18S602 is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a UART serial communications interface, power-on-reset, and expansion interface. Two on-board sockets are provided for read-only memory enabling the user to select 2 or 4 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of the CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S602 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and the special requirements of his specific applications. The CDP18S602 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC DOS Development System III CDP18S007, facilitating prototype design and the debugging of both hardware and software.

Component Features

Central Processing Unit. The central processor for the CDP18S602 Microboard Computer is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802.

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Current required: 8 to 28 mA (typ.)*
- High noise immunity
- Crystal clock — selectable rates: 2.4576, 1.2288, 0.6144, or 0.3072 MHz
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 2 kilobytes of read/write memory
- Sockets for 2/4 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Flexible memory and I/O expansion
- 8 parallel input and 8 parallel output lines
- 4 flag inputs; Q serial data output
- UART-driven serial I/O port
- 14 selectable baud rates: 50 to 19200 baud
- RS232C or 20-mA serial I/O
- 65,536-byte memory space
- 44-pin system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Powered through either expansion or I/O connector
- Wide temperature range: -40° C to 85° C
- Small board size: 4.5 x 7.5 inches

*Depending whether 20-mA serial interface is used.

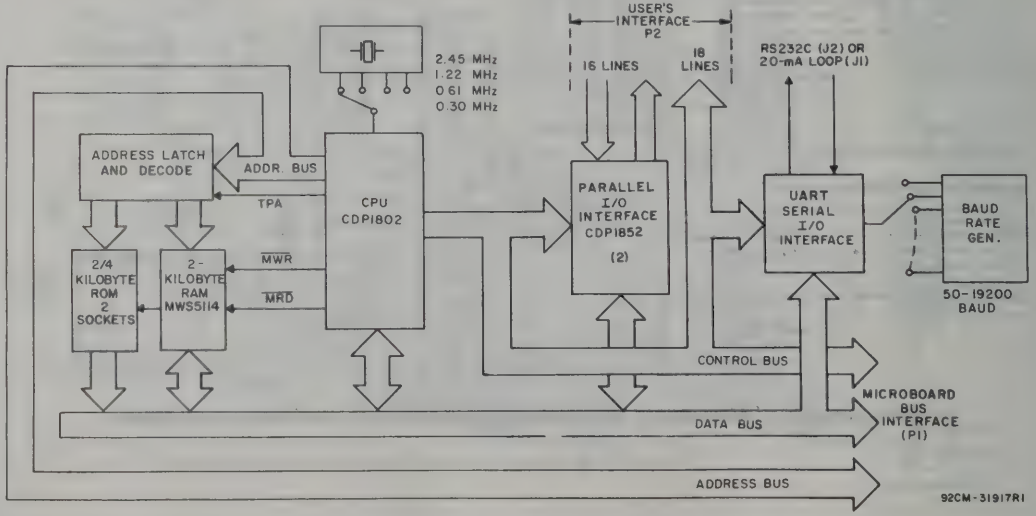

Fig. 1 — Block diagram of RCA COSMAC Microboard Computer CDP18S602.

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The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks and the like. One register each is designated for DMA and interrupt pointers. The CDP1802 provides a serial data-out connection, Q, and four external flag input pins, EF1 through EF4, whose logic levels may be tested with conditional branch instructions.

Memory. By means of four MWS5114 RAM's, the CDP18S602 provides 2 kilobytes of CMOS read-write memory. In addition, two sockets are provided for two or four kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM or 2758 or 2716-type EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on boundaries in accordance with the memory maps given in Tables I and II.

I/O. By means of two parallel I/O ports, type CDP1852, the CDP18S602 provides eight input and eight output lines. Each port has a handshaking line to indicate whether a byte has been written to or read from a port. A serial communications interface, having both a 20-milliampere loop and EIA RS232C capability, is driven by an on-board UART, the CDP1854A. Right-angle headers are provided for the serial communications interfaces.

The data format is determined by software. There are 14 baud rates available, from 50 to 19200 bauds, selectable by a four-rocket DIP switch. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. The user's edge connector provides, in addition to the two 8-line input and output ports, 18 other lines giving access to, among others, four flags, Q, interrupt, clock frequency, and three UART lines.

Application

The COSMAC Microboard Computer CDP18S602 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or through the I/O connector. The CDP18S602 may also be operated in conjunction with other Microboard Systems Components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 22-card Microboard Chassis (CPD18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S602 Microboard computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC DOS Development System III CPD18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When the CDP18S602 Microboard Computer is used with the Microboard Control and Display Module CDP18S640V1, some debugging capability is available even in such a two-card minimum system. By means of the control switches provided with the CDP18S640V1 (RESET, RUN PROGRAM, RUN UTILITY, AND STEP/CONT) and the six-digit hexadecimal display, the operator can observe the address and data sequences of both the fetch and execute cycles.

Specifications

Memory Capacity

On-board RAM: 2 kilobytes

On-board ROM/EPROM: 2 sockets for up to 4 kilobytes

Off-board Expansion: Any user-specified combination of RAM, ROM, and EPROM, up to a total of 65,536 bytes on-board and off-board

Memory Address Map

(See Tables I, II, and III)

On-board RAM: 2 kilobytes contiguous on any 2 kilobyte boundary: Links are preprinted for RAM at address 4000_{16}.

On-board ROM and EPROM: For CDP1834 and 2758, 2 kilobytes contiguous on any 2-kilobyte boundary.

For 2716, 4 kilobytes contiguous on any 4-kilobyte boundary. Links are preprinted for ROM types CDP1834 and 2758 and for address start at 0000.

CDP18S602

I/O Capacity
Parallel: 8 input lines and 8 output lines.
Serial: UART-controlled input and output lines. Choice of 20-mA loop or EIA RS232C interface. User-programmed data format. 15 selectable baud rates, 50 to 19200 baud. CTS and RTS control lines.

Operating Temperature Range
−40° C to 85° C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
With CMOS ROM's and RS232C: +5 V at 8 mA, typical operating
With CMOS ROM's and 20-mA loop: +5 V at 30 mA, typical operating
Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical

Connectors
System Interface: Edge fingers, 44 pins on 0.156-inch centers
Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers
Serial I/O: Two right-angle headers, 10 pins

Clock
CPU and Interface: crystal-controlled oscillator; selectable frequencies: 2.4576, 1.2288, 0.6144, and 0.3072 MHz. A preprinted link selects 2.4576 MHz as the CPU clock frequency.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard Computer CDP18S602 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802A (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor,** MPM-201.

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The service request line from the input port can be jumped via LK1 to either EF3 or EF4 flag lines to indicate status. A preprinted link connects the input port's SR (Service Request) line to EF3 and the SDI (Serial Data In) line to EF4, conditioned by the proper select signal.

$\overline{INT}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{INT}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter. The interrupt line from the UART or the service request line from input port can be presented directly to this input via link LK1.

$\overline{DMAI}$, $\overline{DMAO}$ — Taken directly to the CPU pins and not utilized by the CDP18S602, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S602 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. It is available for use through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A square-wave clock signal derived from an external crystal-controlled oscillator. One of four clock frequencies can be selected, 2.4576, 1.2288, 0.6144, or 0.3072 MHz. This signal is made available on connectors P1 and P2 by a preprinted link across pins 8 and 5 of link LK8. A preprinted link across pins 7 and 8 of link LK3 selects 2.4576 MHz as the CPU clock frequency.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ — Two control inputs to the CPU that determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA-IN requests then load memory starting from location zero for as many bytes as there are DMA-IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and O's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to CLEAR.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S602 to force the most significant address bit true. As a result, the program start is at memory location 8000 instead of 0000. When the CDP18S602 is used in a stand-alone mode and a utility program is included at 8000, an RNU-P signal must be supplied to connector P1-3, and pins 12:1 must be connected on link LK8. When the CDP18S602 is used with Control and Display Module CDP18S640V1, only pins 12:1 on link LK8 need be connected. Note: The board is supplied with a preprinted link — pins 12:1 on link LK8.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described in Tables I through IV. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

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RAM Address. The CDP18S602 Microboard Computer has two kilobytes of contiguous memory which can occupy any 2-kilobyte block in memory space on 2-kilobyte boundaries. The high-order byte of the memory address is latched and decoded. Bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two wire jumpers on link LK5. One jumper on link LK4 will enable the next level of decoding; selecting either A11 or A11 inverted enables the RAM decoder U21. If the latched bit A11 is not inverted, the low half of a 4-kilobyte block is enabled. Bit A10 will next select 1-kilobyte segments within the 2-kilobyte block.

To set up the RAM address, it is necessary to install two jumpers in link LK5 and one in link LK4 as given in the memory map of Table I. As an alternative, DIP switches may be installed if frequent link changes are anticipated.

To avoid having floating inputs to CMOS gates, links LK5 and LK4 must always have jumpers installed.

ROM Address. Two 24-pin sockets (XU9 and XU10) are provided for user-programmed ROM's. Three ROM types are suitable: CDP1834 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes). The address decoding technique prevents "wrap-around" in memory space for any memory type.

Table II shows the LK3 and LK4 link connections needed for the ROM selected. Tables III and IV give the additional link connections needed and the memory address information.

For testing or debugging, all ROM space can be inhibited by connecting A and B on link LK7.

When ROM's CDP1834 or 2758 are used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. One jumper on link LK4 enables the next level of decoding; selecting either A11 or A11 inverted enables ROM decoder U20.

Table I - Memory Map and Link Connections for RAM

LK5		LK4	RAM	Address
1:16	*5:12	*7:10	U16/U18 U15/U17	0000-03FF 0400-07FF
		8:9	U16/U18 U15/U17	0800-0BFF 0C00-0FFF
	6:11	*7:10	U16/U18 U15/U17	1000-13FF 1400-17FF
		8:9	U16/U18 U15/U17	1800-1BFF 1C00-1FFF
	7:10	*7:10	U16/U18 U15/U17	2000-23FF 2400-27FF
		8:9	U16/U18 U15/U17	2800-2BFF 2C00-2FFF
	8:9	*7:10	U16/U18 U15/U17	3000-33FF 3400-37FF
		8:9	U16/U18 U15/U17	3800-3BFF 3C00-3FFF
*2:15	*5:12	*7:10	U16/U18 U15/U17	4000-43FF 4400-47FF
		8:9	U16/Y18 U15/U17	4800-4BFF 4C00-4FFF
	6:11	*7:10	U16/U18 U15/U17	5000-53FF 5400-57FF
		8:9	U16/U18 U15/U17	5800-5BFF 5C00-5FFF
	7:10	*7:10	U16/U18 U15/U17	6000-63FF 6400-67FF
		8:9	U16/U18 U15/U17	6800-6BFF 6C00-6FFF
	8:9	*7:10	U16/U18 U15/U17	7000-73FF 7400-77FF
		8:9	U16/U18 U15/U17	7800-7BFF 7C00-7FFF
3:14	*5:12	*7:10	U16/U18 U15/U17	8000-83FF 8400-87FF
		8:9	U16/U18 U15/U17	8800-8BFF 8C00-8FFF
	6:11	*7:10	U16/U18 U15/U17	9000-93FF 9400-97FF
		8:9	U16/U18 U15/U17	9800-9BFF 9C00-9FFF
	7:10	*7:10	U16/U18 U15/U17	A000-A3FF A400-A7FF
		8:9	U16/U18 U15/U17	A800-ABFF AC00-AFFF
	8:9	*7:10	U16/U18 U15/U17	B000-B3FF B400-B7FF
		8:9	U16/U18 U15/U17	B800-BBFF BC00-BFFF
4:13	*5:12	*7:10	U16/U18 U15/U17	C000-C3FF C400-C7FF
		8:9	U16/Y18 U15/U17	C800-CBFF CC00-CFFF
	6:11	*7:10	U16/U18 U15/U17	D000-D3FF D400-D7FF
		8:9	U16/U18 U15/U17	D800-DBFF DC00-DFFF
	7:10	*7:10	U16/U18 U15/U17	E000-E3FF E400-E7FF
		8:9	U16/U18 U15/U17	E800-EBFF EC00-EFFF
	8:9	*7:10	U16/U18 U15/U17	F000-F3FF F400-F7FF
		8:9	U16/U18 U15/U17	F800-FBFF FC00-FFFF

*Preprinted link connections.

Table II — Connections for Link LK3 and LK4 for ROM

Link	CDP1834 or 2758	2716
LK4 1:16*	C	O
LK4 2:15	O	C
LK4 4:13	O	C
LK4 5:12*	X	O
LK4 6:11	X	O
LK3 1:14	O	C
LK3 2:13*	C	O

O = Open; C = Closed; *Preprinted link connections.
X = See Table III.

If bit A11 is not inverted, the low half of the 2-kilobyte block is selected. If bit A11 is inverted by U19, the high half of the block is enabled. Another jumper on link LK4 connects bit A10 to the decoder selecting one of the two 1-kilobyte blocks. For the CDP1834 and 2758, input pin 19 of the ROM is grounded. Note that to avoid floating inputs, links LK6 and LK4 must have jumpers installed.

When ROM 2716 is used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. With another jumper connecting pins 2:15 on link LK4, bit A11 now selects 2-kilobyte segments within a 4-kilobyte block. Link LK3 is used to connect address bit A10 to pin 19 of the 2716 ROM.

Table III — Additional Link Connections and Memory Addresses for ROM Types CDP1834 and 2758

LK6		LK4	ROM	Address
*1:16	*5:12	*5:12	U9	0000-03FF
			U10	0400-07FF
		6:11	U9	0800-0BFF
			U10	0C00-0FFF
	6:11	*5:12	U9	1000-13FF
			U10	1400-17FF
		6:11	U9	1800-1BFF
			U10	1C00-1FFF
	7:10	*5:12	U9	2000-23FF
			U10	2400-27FF
		6:11	U9	2800-2BFF
			U10	2C00-2FFF
	8:9	*5:12	U9	3000-33FF
			U10	3400-37FF
		6:11	U9	3800-3BFF
			U10	3C00-3FFF
2:15	*5:12	*5:12	U9	4000-43FF
			U10	4400-47FF
		6:11	U9	4800-4BFF
			U10	4C00-4FFF
	6:11	*5:12	U9	5000-53FF
			U10	5400-57FF
		6:11	U9	5800-5BFF
			U10	5C00-5FFF
	7:10	*5:12	U9	6000-63FF
			U10	6400-67FF
		6:11	U9	6800-6BFF
			U10	6C00-6FFF
	8:9	*5:12	U9	7000-73FF
			U10	7400-77FF
		6:11	U9	7800-7BFF
			U10	7C00-7FFF
3:14	*5:12	*5:12	U9	8000-83FF
			U10	8400-87FF
		6:11	U9	8800-8BFF
			U10	8C00-8FFF
	6:11	*5:12	U9	9000-93FF
			U10	9400-97FF
		6:11	U9	9800-9BFF
			U10	9C00-9FFF
	7:10	*5:12	U9	A000-A3FF
			U10	A400-A7FF
		6:11	U9	A800-ABFF
			U10	AC00-AFFF
	8:9	*5:12	U9	B000-B3FF
			U10	B400-B7FF
		6:11	U9	B800-BBFF
			U10	BC00-BFFF
4:13	*5:12	*5:12	U9	C000-C3FF
			U10	C400-C7FF
		6:11	U9	C800-CBFF
			U10	CC00-CFFF
	6:11	*5:12	U9	D000-D3FF
			U10	D400-D7FF
		6:11	U9	D800-DBFF
			U10	DC00-DFFF
	7:10	*5:12	U9	E000-E3FF
			U10	E400-E7FF
		6:11	U9	E800-EBFF
			U10	EC00-EFFF
	8:9	*5:12	U9	F000-F3FF
			U10	F400-F7FF
		6:11	U9	F800-FBFF
			U10	FC00-FFFF

*Preprinted link connections.

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Table IV - Additional Link Connections and Memory Addresses for ROM Type 2716

LK6		ROM	Address
*1:16	*5:12	U9 U10	0000-07FF 0800-0FFF
	6:11	U9 U10	1000-17FF 1800-1FFF
	7:10	U9 U10	2000-27FF 2800-2FFF
	8:9	U9 U10	3000-37FF 3800-3FFF
2:15	*5:12	U9 U10	4000-47FF 4800-4FFF
	6:11	U9 U10	5000-57FF 5800-5FFF
	7:10	U9 U10	6000-67FF 6800-6FFF
	8:9	U9 U10	7000-77FF 7800-7FFF
3:14	*5:12	U9 U10	8000-87FF 8800-8FFF
	6:11	U9 U10	9000-97FF 9800-9FFF
	7:10	U9 U10	A000-A7FF A800-AFFF
	8:9	U9 U10	B000-B7FF B800-BFFF
4:13	*5:12	U9 U10	C000-C7FF C800-CFFF
	6:11	U9 U10	D000-D7FF D800-DFFF
	7:10	U9 U10	E000-E7FF E800-EFFF
	8:9	U9 U10	F000-F7FF F800-FFFF

*Preprinted link connections.

Note that with type 2716 also, jumpers must always be present to avoid floating inputs to CMOS gates. Note that the CDP18S602 is initially configured for ROM types CDP1834 and 2758 at address 0000.

Input/Output Interfacing

Serial I/O Interfacing. Serial output data is generated by the UART. In Microboard systems including the Control and Display Module CDP18S640V1, the utility software UT61 sets the data format. This format is one start bit, eight data bits (no parity), and two stop bits. The utility also determines when to read data from the UART and when to write to it by reading its status word. The user, of course, has the option in a stand-alone system of writing his own UART routine.

The UART interrupt line is wired to link LK1 where the user may jumper it either to the CPU's interrupt input or to one of two flag lines (EF3 or EF4).

Three signals from the UART are available on the user connector P2. These signals, DA (data available), RTS (request to send), and CTS (clear to send), are useful for handshaking with modems. See the data sheet for UART CDP1854A (File No. 1193).

Because the SDI line is connected to EF4 by means of a preprinted link, a break condition may be conveniently detected.

Any one of the 14 baud rates available from the baud rate generator can be selected through a four-bit binary code determined by the setting of a four-rocker DIP switch. The switch settings are given in Table V.

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2, respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire between pins A and B on link LK2, and supplying +12 V and –5 V power.

Table V - Baud Rate Selection Chart

Switch S1				Output Rate Baud*
4	3	2	1	
C	C	C	C	19200
C	C	O	C	50
C	C	O	O	75
C	O	C	C	134.5
C	O	C	O	200
C	O	O	C	600
C	O	O	O	2400
O	C	C	C	9600
O	C	C	O	4800
O	C	O	C	1800
O	C	O	O	1200
O	O	C	C	2400
O	O	C	O	300
O	O	O	C	150
O	O	O	O	110

*Actual input to UART is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.
O = Open; C = Closed

Two-Level I/O Interfacing. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard System the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function. Any I/O function is assigned to a group number and only responds when its group number and its appropriate N register code are transmitted.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S602 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The user may place the UART in one of two I/O groups by the position of a jumper wire on link LK1. If data bit DB0 is used as a group select, the group number $(0000\ 0001)_2$ is transmitted by the 61 output instruction to select the UART. The CDP18S602 comes with the link preprinted for group 1. The user also has the option of using data bit DB1 or group number $(0000\ 0010)_2$ for selecting the UART. When the UART is selected, the I/O instructions 62, 63, 6A, and 6B are reserved for use in the utility programs UT61 for operating the UART. When the CDP18S602 is used with Microboard Control and Display Module CDP18S640V1, which contains the utility program UT61, the UART must be linked for group 1.

Other settings of links LK1 and LK10, as shown in Table VI, make it possible to monitor UART signals by connecting them to flag and interrupt lines.

Table VI - UART Linking Arrangements

UART Group Select
Group 1 (01_{16}): LK1 2:9 Closed; LK1 1:10 Open Group 2 (02_{16}): LK1 2:9 Open; LK1 1:10 Closed
SDI to EF4-N
LK1 6:5 Closed; LK10 2:3 Closed; LK10 1:4 Open
UART DA-N to EF4-N
LK1 6:5 Closed; LK10 2:3 Open; LK10 1:4 Closed
UART INT-N to CPU INT-N
LK1 3:8 Closed

Parallel I/O Interfacing. The parallel I/O interface consists of 20 lines provided on connector P2. Two CDP1852's provide one input and one output port. The input port sets a service request line (SR) when data is strobed into it. SR is initially linked to EF3. The output port provides a data available signal (DA) when a byte is written into it. For more details, see the data sheet for the CDP1852 (File No. 1166).

The two ports are assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data $=08_{16}$ is required before read or write may be performed. Then I/O instructions 62 and 6A select the output or input port, respectively.

Power-On Reset

An RC integrator (R2 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U23) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, UART, and the I/O group-select latches. After the CLEAR signal, the I/O group selects are reset, the output port and its DA are reset, and the input port goes to a high-impedance state with SR reset. The CPU initializes and starts processing at location 0000 provided the WAIT line is not asserted.

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development Systems CDP18S005 (II) and CDP18S007 (III)

Replacement of the CDS CPU Module CDP18S102 or CDP18S102V1 with the RCA COSMAC Microboard

CDP18S602

Computer CDP18S602 requires some link changes on the CDP18S602. These changes are:

LK9 — Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter), do not install A:D.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK8 — RNU to start ROM's at address 8000. If there is ROM at 8000 containing a utility program, connect a wire jumper between 11 and 2 on link LK8 and cut link between 12 and 1 on link LK8. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after the RESET RUN U switches are pressed.

Memory Address Links. The desired memory addresses should be set up according to the memory maps of Tables I through IV. Care should be taken that the CDS memories are not assigned to overlap the assignment of the CDP18S602 Microboard Computer.

Connector Matching Cables - Available Separately

CDP18S515 - TTY Terminal Interface Cable
Fits connector J1; 15 feet long; has Molex connector for 20-mA TTY terminal.

CDP18S516 - EIA Terminal Interface Cable
Fits connector J2; 15 feet long; has 25-pin delta and mating male connectors for EIA RS232C Terminal.

CDP18S517 - I/O Interface Cable
Fits connector P2; 36 inches long; 34-pin flat ribbon cable; output end unterminated.

Table VII - List of Links and Their Functions

LK1	
1:10	Select UART - Group 02_{16}
*2:9	Select UART - Group 01_{16}
3:8	UART Interrupt Line to CPU Interrupt
*4:7	Input Port Service Request to EF3
*5:6	Serial Data-In Line to EF4
LK2	
A:B	EIA Receiver Operation
LK3	
1:14	ROM 2716 Operation
*2:13	ROM CDP1834/2758 Operation
3:12	1.2288 MHz CPU Frequency
4:11	0.6144 MHz CPU Frequency
5:10	0.3072 MHz CPU Frequency
§6:9	4.9152 MHz CPU Frequency
*7:8	2.4576 MHz CPU Frequency
LK4	
*1:16	ROM Decoding
2:15	ROM Decoding
3:14	Permanent Connection
4:13	ROM Decoding
*5:12	ROM Decoding
6:11	ROM Decoding
*7:10	RAM Decoding
8:9	RAM Decoding

LK5		**LK6**	
1:16	RAM Decoding	*1:16	ROM Decoding
*2:15	RAM Decoding	2:15	ROM Decoding
3:14	RAM Decoding	3:14	ROM Decoding
4:13	RAM Decoding	4:13	ROM Decoding
*5:12	RAM Decoding	*5:12	ROM Decoding
6:11	RAM Decoding	6:11	ROM Decoding
7:10	RAM Decoding	7:10	ROM Decoding
8:9	RAM Decoding	8:9	ROM Decoding

LK7	
A:B	Inhibit ROM
LK8	
*1:12	RUN U
2:11	RUN U If Installed in CDP18S005 or CDP18S007
3:10	Not Used
4:9	Not Used
*5:8	Clock Frequency Out
*6:7	+5 V
LK9	
*A:B	$\overline{EF4}$ to Backplane
*C:D	+12 V/+15 V
LK10	
1:4	UART DA Line to $\overline{EF4}$
*2:3	Serial Data In to $\overline{EF4}$
LK11	
*1:5	$\overline{CLEAR}$
*2:3	$\overline{WAIT}$
5:6	Not Used
2:4	Not Used

*Preprinted links.
§Not applicable to CDP18S602.

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Table VIII — Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

Table IX - Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	DI2-P	2	GND
3	DI1-P	4	DI3-P
5	DI0-P	6	DI4-P
7	STROBE P	8	DI5-P
9	CLOCK OUT	10	DI6-P
11	DO7-P	12	DI7-P
13	DO6-P	14	CTS-N
15	DO5-P	16	CLEAR-N
17	DO4-P	18	GND
19	DO3-P	20	Q-P
21	DO2-P	22	DA-N
23	DO1-P	24	EF4-N
25	DO0-P	26	EF3-N
27	INT-N	28	RTS-N
29	DA-P	30	+5 V
31	EF2-N	32	−5 V/−15 V
33	EF1-N	34	+12 V/+15 V

Table X - Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Table XI - Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

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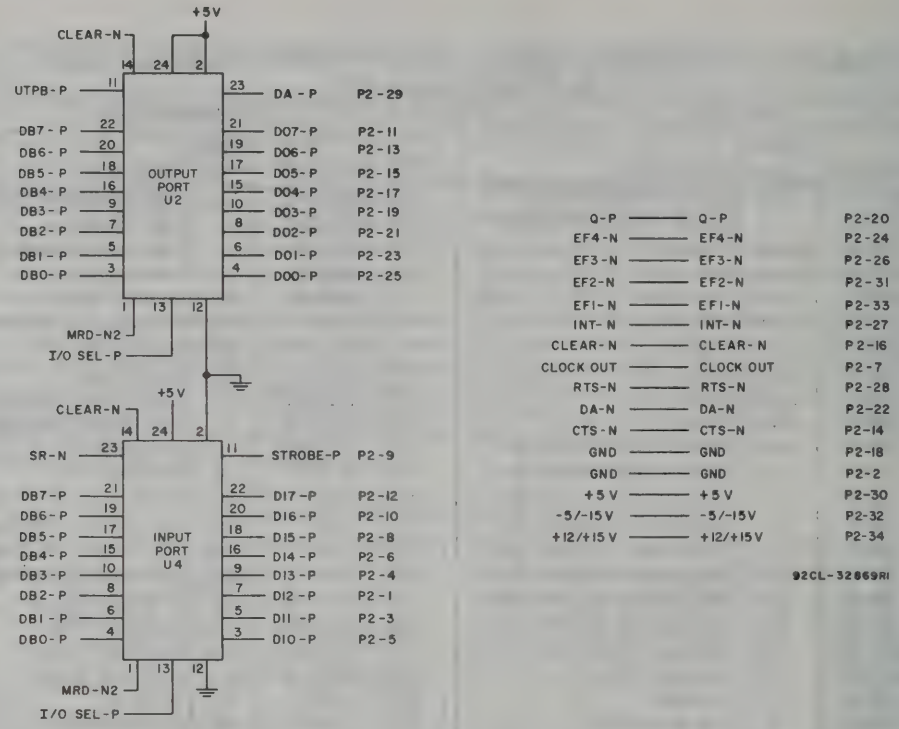
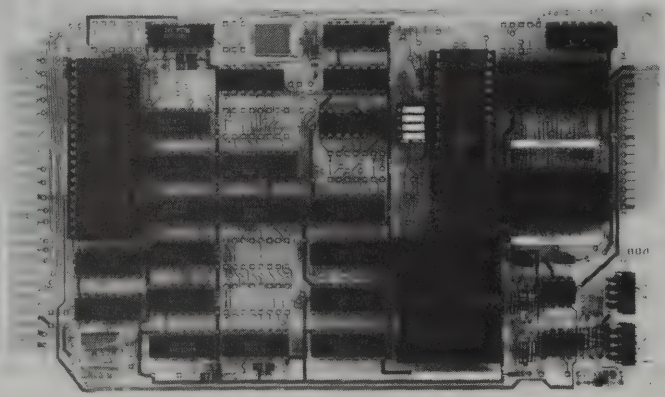


Fig. 2 — Logic Diagram of Microboard Computer CDP18S602 — Parallel I/O Interface Portion.



CDP18S602

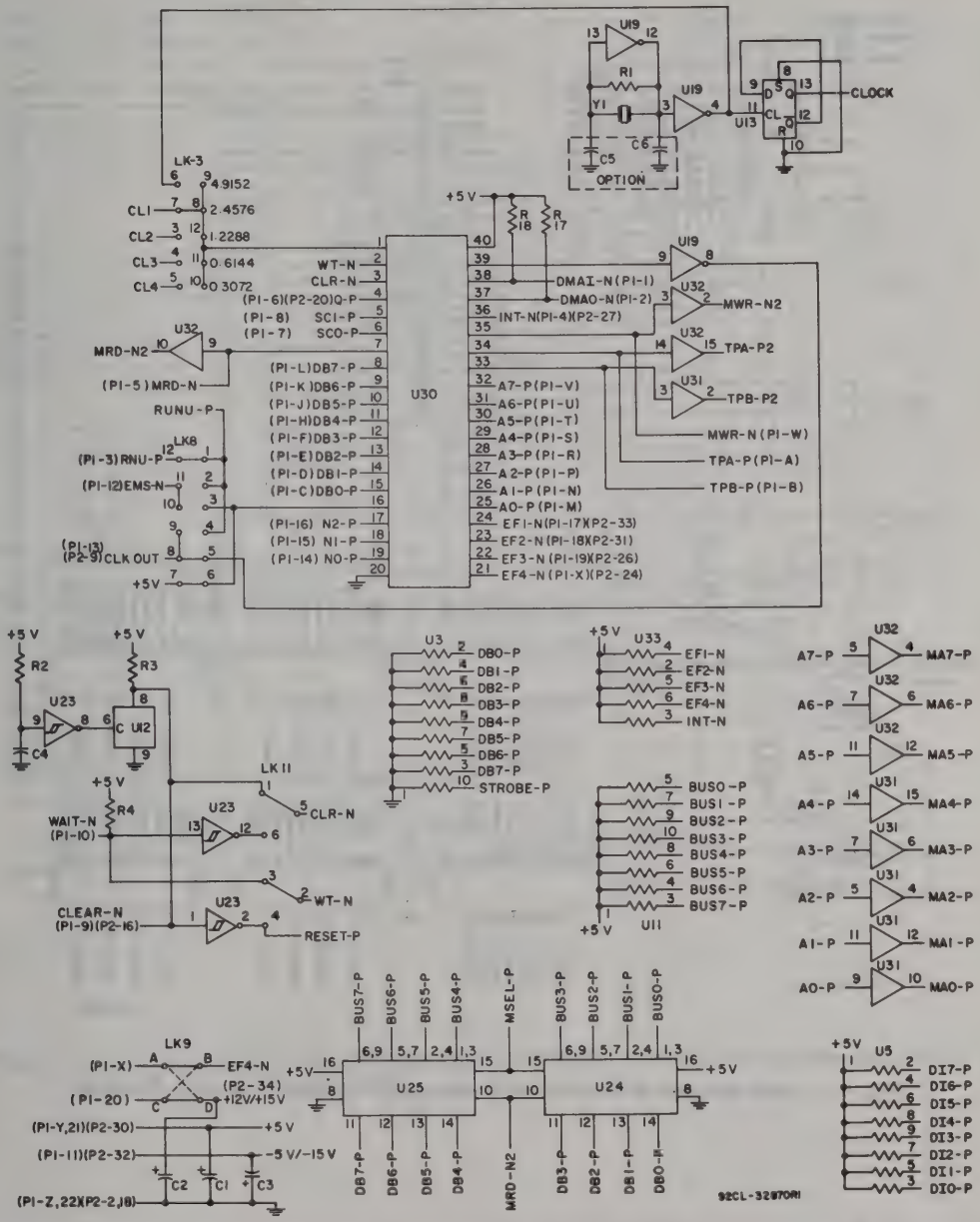


Fig. 3 — Logic diagram of Microboard Computer CDP18S602 - CPU, Oscillator, and Buffer portion.

CDP18S602

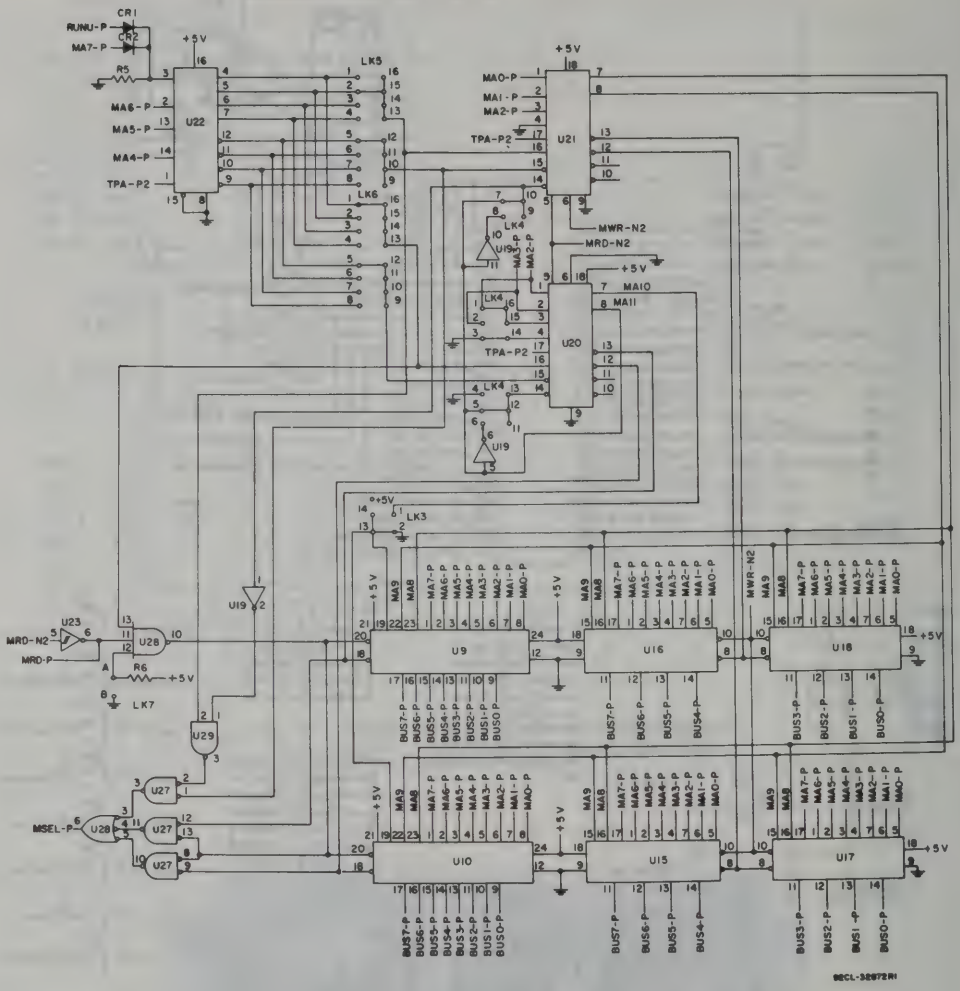


Fig. 4 — Logic diagram of Microboard Computer CDP18S602 - Memory Portions.

CDP18S602

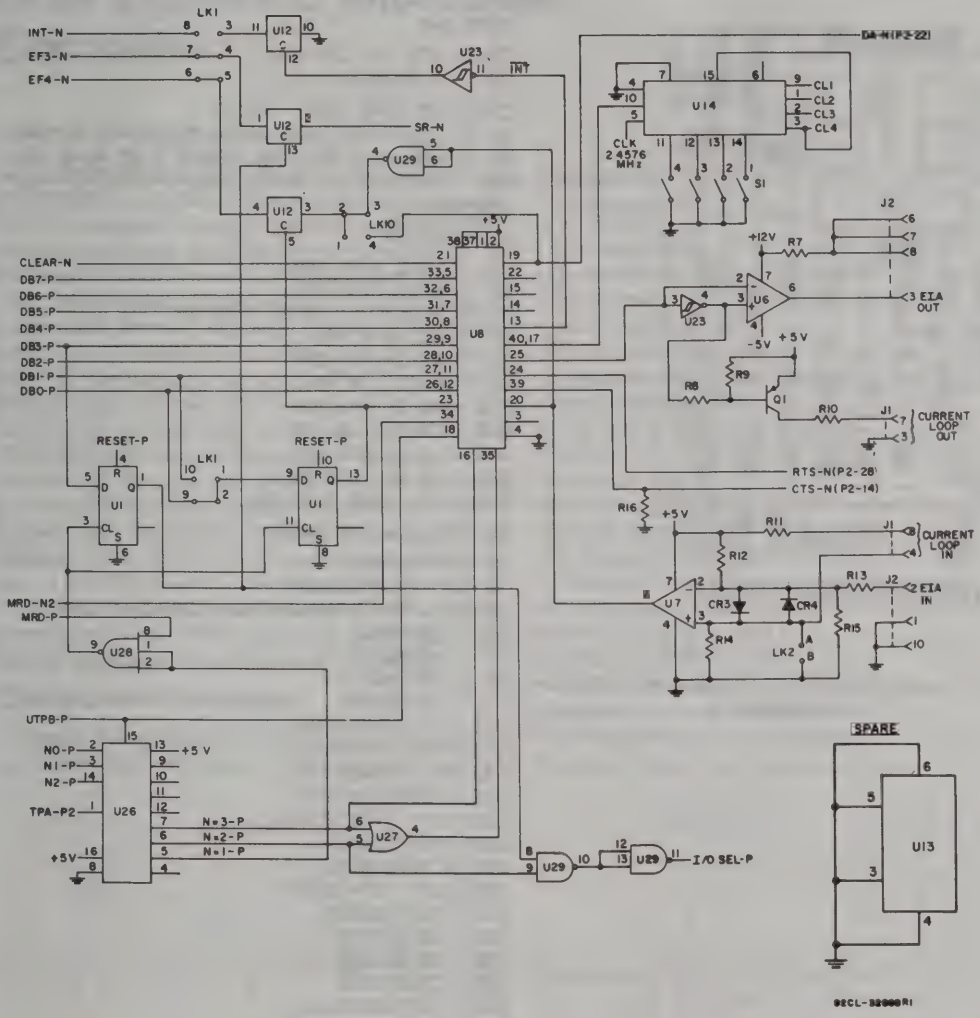


Fig. 5 — Logic Diagram of Microboard Computer CDP18S602 - UART Serial I/O Interface Portion.

CDP18S602

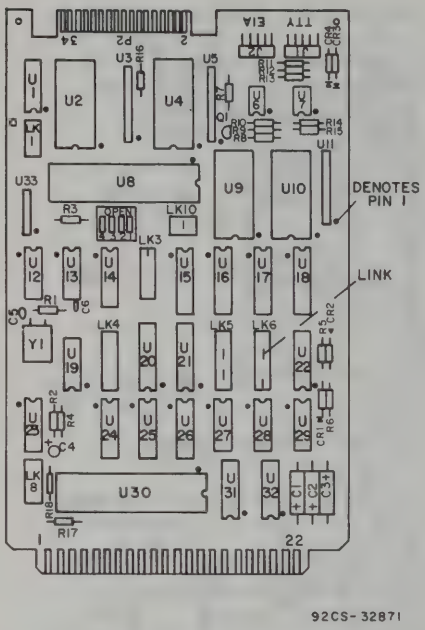


Fig. 6 — Layout Diagram of Microboard Computer CDP18S602.

Parts List

C1, C2, C3 = 15 μF, 20 V
C4 = 1.5 μF, 25 V

CR1, CR2, CR3, CR4 = 1N270
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP86016-1, keying plug — AMP 87077-1, or equivalent)

Q1 = 2N5139

R1 = 22 MΩ, ¼ W, 10%
R2 = 100 kΩ, ¼ W, 5%
R3-R6, R16-R18 = 22 kΩ, ¼ W, 5%
R7 = 3 kΩ, ¼ W, 5%
R8 = 2.7 kΩ, ¼ W, 5%
R9 = 10 kΩ, ¼ W, 5%
R10 = 100 Ω, ¼ W, 5%
R11 = 130 Ω, ¼ W, 5%
R12 = 11 kΩ, ¼ W, 5%
R13 = 4.3 kΩ, ¼ W, 5%
R14, R15 = 1 kΩ, ¼ W, 5%

S1 = 4-rocker DIP switch

U1 = CD4013BE
U2, U4 = CDP1852CE
U3, U5, U11 = resistor module, 22 kΩ, 10 pin
U6 = CA3140AE
U7 = CA3160AE
U8 = CDP1854ACE
U12 = CD4066BE
U13 = 4013 Fairchild
U14 = 4702 Fairchild
U15-U18 = MWS5114E
U19 = 4069 Fairchild
U20, U21 = CDP1866CE
U22 = CDP1858CE
U23 = CD40106BE
U24, U25 = CDP1856CE
U26 = CDP1853CE
U27 = CD4071BE
U28 = CD4023BE
U29 = CD4011BE
U30 = CDP1802ACE
U31, U32 = CD4050BE
U33 = resistor module, 22 kΩ, 6 pin

XU9, XU10 = 24-pin socket

Y1 = 4.9152-MHz crystal

CDP18S603

RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP18S603 is a versatile computer system on a single 4.5×7.5 inch card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S603 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and special requirements of his specific application. The CDP18S603 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC CDOS Development System CDP18S007 facilitating prototype design and the debugging of both hardware and software.

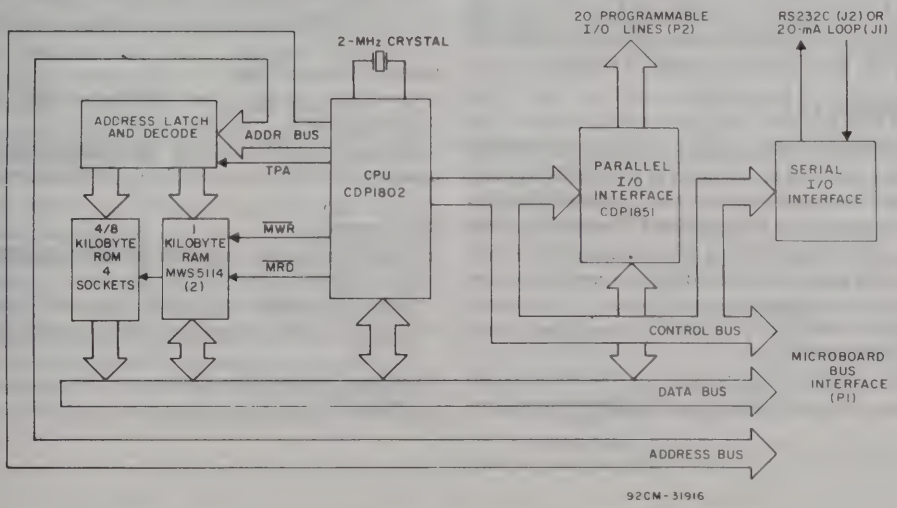
Component Features

Central Processing Unit. The central processor for the CDP18S603 Microboard Computer is the 8-bit

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Current required—7 to 27 mA (typ.)†
- High noise immunity
- 2-MHz crystal clock
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 1 kilobyte of read/write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Flexible memory and I/O expansion
- 20 programmable parallel I/O lines
- 4 flag inputs
- Q serial data output
- RS232C or 20-mA serial I/O
- 65,536-byte memory space
- 44-pin system interface
- Temperature range −0°C to 70°C
- Small board size—4.5×7.5 inches

†Depending whether 20-mA serial interface is used.



Block diagram of RCA COSMAC Microboard Computer CDP18S603.

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silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. By means of two MWS5114 RAM's, the CDP18S603 provides 1 kilobyte of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S603 provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

Application

The COSMAC Microboard Computer CDP18S603 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board. It may also be operated in conjunction with other Microboard System components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S603 Microboard Computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC CDOS Development System CDP18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the applicatcn software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

Specifications

Memory Capacity

On-board RAM: 1 kilobyte

On-board ROM/EPROM: 4 sockets for up to 8 kilobytes.

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map

On-board RAM: Low 1-kilobyte block in any 4-kilobyte block.

On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity

Parallel: 20 lines each programmable as input, output, or bidirectional.

Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.

Operating Temperature Range

0 °C to 70 °C.

Dimensions

4.5 inches × 7.5 inches (114.3 × 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

With CMOS ROM's, with RS232C: +5 V at 7 mA, typical operating

With CMOS ROM's and 20-mA loop: +5 V at 27 mA, typical operating

Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pin.

Clock

CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard Computer CDP18S603 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

DB7 through DB0—Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2—Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$—Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S603 uses EF1 and EF2, conditioned by the secondary I/O address, to test the READY state of I/O ports A and B. The serial data interface input is presented directly on EF4 or EF3 chosen by link LK36. I/O devices using the INT line may make use of the EF lines to identify the device. They may also be used to indicate priority or status.

$\overline{\text{INT}}$—Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

$\overline{\text{DMAI}}$, $\overline{\text{DMAO}}$—Taken directly to the CPU pins and not utilized by the CDP18S603, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0—State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

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TPA, TPB—Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0—Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S603 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$—A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$—A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q—A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. The CDP18S603 may use Q as a serial data output to the RS232C and 20-mA data terminal drivers. It is also available for other uses through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT—A 2-MHz square-wave clock provided for general use. It is derived from the crystal-controlled oscillator in the CPU.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$—Two control inputs to the CPU which determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA IN requests then load memory starting from location zero for as many bytes as there are DMA IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to $\overline{\text{CLEAR}}$.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU—Run Utility Software. A signal supplied to the CDP18S603 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed

as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The RAM on the CDP18S603 is 1 kilobyte of contiguous memory. The high-order four bits of memory address are latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy 1 kilobyte starting at any even 4-kilobyte block in the memory space. Because the 4-kilobyte decoder enables the data buffers U5 and U8, the whole 4-kilobyte block selected for RAM is removed from the available memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

Table I—4-Kilobyte Link Connections

4-Kilobyte Address Space	LINK LK10, LK11, or LK22 Pin Connections
0000 - 0FFF	1:16, 5:12
1000 - 1FFF	1:16, 6:11
2000 - 2FFF	1:16, 7:10
3000 - 3FFF	1:16, 8:9
4000 - 4FFF	2:15, 5:12
5000 - 5FFF	2:15, 6:11
6000 - 6FFF	2:15, 7:10
7000 - 7FFF	2:15, 8:9
8000 - 8FFF	3:14, 5:12
9000 - 9FFF	3:14, 6:11
A000 - AFFF	3:14, 7:10
B000 - BFFF	3:14, 8:9
C000 - CFFF	4:13, 5:12
D000 - DFFF	4:13, 6:11
E000 - EFFF	4:13, 7:10
F000 - FFFF	4:13, 8:9

LINK 11 is associated with the 1-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.

ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

Two types of links are provided and must be made up by the user to suit the particular ROM configuration selected. The first link type is for accommodating the type of ROM selected (CDP1834, 2708, 2758, or 2716. The second link type is for selecting the memory address space to be occupied by the ROM.

Link LK4 is an 18-pin dual-in-line arrangement with preprinted links to accommodate the 2716 ROM's. Table II gives the connections required for each ROM type.

Links LK10 and LK22 are 16-pin dual-in-line arrangements with no preprinted links. A DIP switch may be installed if frequent address changes are expected. Link LK10 provides the high-order four address bits decoded so that two links or jumpers place sockets XU24 and XU25 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK22 does the same for sockets XU26 and XU27. See Table I for address map and link connections.

To avoid having floating inputs to the gates, both links LK10 and LK22 should always have two jumpers. For example, if sockets XU26 and XU27 are unused, LK22 may be jumpered the same as LK10. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

In instances where the ROM sockets are not fully occupied, it may be desirable to jumper links LK10 or LK22, or both, identically with LK11 so that the unused ROM space overlays the RAM space. Although the 1-kilobyte RAM usurps the whole of its 4-kilobyte assignment on LK11, the remaining 3 kilobytes may be filled by (1) leaving socket XU25 empty; (2) populating sockets XU24, XU26, and XU27 with 1 kilobyte devices; and (3) jumpering LK10, LK11, and LK22 identically. If there is to be no ROM on this board, this linking will prevent the unused sockets from being assigned to memory space perhaps needed by other system boards.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK10 and LK22 should be jumpered identically in accordance with Table I. Then, the ROM's should be installed in sockets XU25, XU27, XU24, and XU26, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK10 and LK22 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then, socket XU25 is the low 2 kilobytes and socket XU24 is the high 2 kilobytes of the 4-kilobyte block as set in LK10. Similarly, socket XU27 is the low 2 kilobytes and socket XU26 is the high 2 kilobytes of the 4-kilobyte block set in LK22.

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One-kilobyte ROM type CDP1834 is the only one that may be used in combination with two-kilobyte ROM's type 2716. If all links are set up for the 2-kilobyte ROM's as shown in Table II for LK4, and LK10 and LK22 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU25 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU24, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU24 or socket XU25 while the other is occupied by a 1-kilobyte ROM. Socket XU27 (low 2 kilobytes) and socket XU26 (high 2 kilobytes) may be used in the same manner.

Table II - ROM Type Selection Links

Link LK4 Pins	ROM Type			
	CDP1834	2708	2758	2716*
1:18	X	OPEN	SHORTED	SHORTED
2:17	X	SHORTED	OPEN	OPEN
3:16	SHORTED	SHORTED	SHORTED	OPEN
4:15	OPEN	OPEN	OPEN	SHORTED
5:14	OPEN	OPEN	OPEN	SHORTED
6:13	SHORTED	SHORTED	SHORTED	OPEN
7:12	X	SHORTED	OPEN	OPEN
8:11	X	OPEN	OPEN	SHORTED
9:10	X	OPEN	SHORTED	OPEN

*X = don't care; Link LK4 is prewired to accept 2716.

I/O Operation

Serial I/O Interface. Serial data output is generated by the Q line from the CPU. Thus, software using the SET Q and RESET Q instructions generates data rate and format. Serial data input is presented to either EF3 or EF4, selectable by links as shown in Table III. The software uses the test branch instructions to decode incoming data.

Table III–Link Table for Serial Data In

Link LK36	Function
7:10	Data to EF3
8:9	Data to EF4

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2 respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire in the C5 holes. RS232C data terminals require that +12 volts be available on pin 20 of the backplane and -5 volts be available on pin 11.

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction.

The CDP18S603 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The CDP18S603 uses bit three as the group select; that is, the group number $(08)_{16}$ or $(0000\ 1000)_2$ is transmitted by the 61 output instruction to select the programmable I/O on board.

In general, although Interrupt is not gated by group select, External Flags are gated by the appropriate group select. The serial interface on the CDP18S603, however, uses either EF3 or EF4 with no gating by group number. Therefore, when the serial interface is wired for use, EF3

or EF4, whichever was chosen, is not generally available for other devices.

Parallel I/O Interface. The parallel I/O interface consists of 20 lines provided on connector P2. These 20 lines are generated by the CDP1851 Programmable I/O Interface and may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides the Q line, EF1 through EF4, CLEAR, three different voltages, and a logic ground.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device.

The CDP1851 is assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data = 08 is required before read, write, or control I/O may be performed.

Signal ARDY conditioned by the group select generates EF1; BRDY and group select generates EF2. Link LK41, pins A and B may be jumpered if interrupt-driven software is to be used. Then, INTA or INTB generates INT unconditionally.

Once the group select is accomplished, N1 and N2 are used to address the CDP1851. The following read and write instructions are used to access data, status, and command registers.

62—Write to control register
64—Write to Port A data register (if A is an output)
66—Write to Port B data register (if B is an output)
6A—Read status register
6C—Read Port A data register (if A is an input)
6E—Read Port B data register (if B is an input)

Using the READY Lines for Data Synchronization. The Port A and Port B RDY lines are presented to the CPU EF1 and EF2 lines when the group select is set. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU. Note that there is a logic reversal: when RDY is true, the EF is false. Because of the logic reversal and because the event of interest is RDY going false, the EF true test is used. A test for ARDY might use the B1 instruction (34) which would take the branch if ARDY were false.

When a port designated as an **output** port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true), and load the next output byte. When a port is designated as an **input** port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and then reads the input byte. **In this case, a dummy read after reset is necessary to raise the first RDY.**

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the INTERRUPT Line for Data Synchronization. If link LK41, A:B is jumpered, INTA or INTB generates INT to the CPU. INT is not conditioned by the group select.INT is set by the remote device sending STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table IV summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the group select 08, and then, either testing the RDY lines or reading the status byte. The low-order two bits of the status byte are: bit 0 = INTB; bit 1 = INTA.

Bidirectional Mode. Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, ARDY and ASTB become A INPUT RDY and A INPUT STB; BRDY

Table IV—READY and INTERRUPT Actions for Input and Output Modes.

		Output Port	Input Port
READY	Set By	Loading Data	Reading Data
	Reset by	STB leading edge	STB leading edge
INTERRUPT	Set by	STB trailing edge	STB trailing edge
	Reset by	Loading Data	Reading Data

CDP18S603

becomes A OUTPUT RDY, and BSTB becomes A OUTPUT STB. Each of the eight lines AD0—AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that output data is gated into AD0—AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode. Both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development Systems CDP18S005 or CDP18S007

Replacement of the CDS CPU Module CDP18S102 with the RCA COSMAC Microboard Computer CDP18S603 requires some link changes on the CDP18S603 and wiring changes on the CDS backplane. These changes are:

LK 43—Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D. See Table V.

Table V–Changes on Link LK43 for Installation of CDP18S603 in COSMAC Development System CDP18S005.

LK43	A:B	C:D	A:D	B:C
Microboard	*Closed	*Closed	Open	Open
CDS	Open	Open	Closed	Closed

*Preprinted links

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK 36 —Serial Data In to external flag lines. In the CDS II, if the Terminal Interface Module CDP18S507 is not retained, connect pins 8:9 for EF4 to make the CDP18S603 the operator's terminal interface. If the CDP18S507 is retained, EF3 may be used for another serial interface purpose by connecting pins 7:10. In the CDS III, the UART module in location 14 is the operator's terminal interface and pins 7:10 and 8:9 may be left open.

LK 36—RNU to start ROM's at address 8000. Cut the wire jumper in pins 5:12. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed. This wire should be removed when the CPU Module CDP18S102 is reinstalled. See Table VI.

Table VI–Changes on Link LK36 for Installation of CDP18S603 in COSMAC Development System CDP18S005.

LK36	RNU 5:12	RNU 6:11	EF3 7:10	EF4 8:9
Microboard	¢Closed	Open	Open	¢Closed
CDS	Open	Closed	Open	Closed@

¢Wire jumpers installed
@Assumes the CDP18S603 serial interface is to be the operator terminal interface.

LK 10. 11, and 22—Set up as previously described for the memory address desired, taking care that the CDS memories are not assigned to overlap the assignment of the CDP18S603 Microboard Computer.

Table VII summarizes the required CDS backplane wiring changes.

Table VII–Summary of Backplane Wiring Additions Needed When the CDP18S603 is Installed in the COSMAC Development System CDP18S005.

From		To		
Slot	Pin	Slot	Pin	Function
12	X	13	20	-12 V
12	11	14	11	-5 V
12	12	10	D	RNU-P †

†This connection should be removed when the CDP18S102 is reinstalled.

Parts List

C1, C2, C3 = 15 μF, 20 V
C4 = 1.5 μF, 35 V
C6=39 pF
C7=10 pF

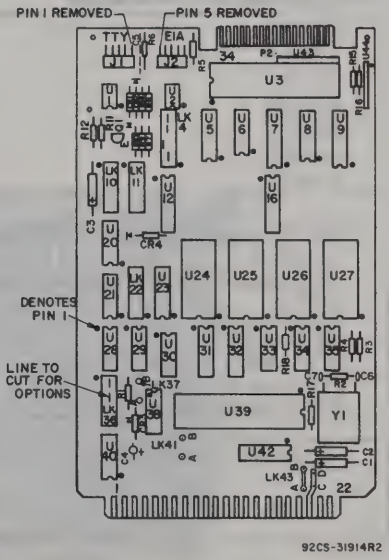
CR1, CR2, CR3, CR4 = 1N270
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP86016-1, keying plug — AMP 87077-1, or equivalent)

P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalents
Q1 = 2N5139

R1 = 100 kΩ, ¼ W, 5%
R2 = 22 MΩ, ¼ W, 5%
R3, R4 = 22 kΩ, ¼ W, 5%
R5 = 3 kΩ, ¼ W, 5%
R6, R14 = 1 kΩ, ¼ W, 5%
R7 = 11 kΩ, ¼ W, 5%
R8 = 4.3 kΩ, ¼ W, 5%
R9 = 130 kΩ, ¼ W, 5%
R10 = 10 kΩ, ¼ W, 5%
R11 = 2.7 kΩ, ¼ W, 5%
R12 = 100 Ω, ¼ W, 5%
R15-R18 = 22 kΩ, ¼ W, 5%

U1 = CA3160
U2 = CA3140
U3 = CDP1851CE
U5, U8 = CDP1856CE
U6 = CD4069BE
U7 = CDP1867CE
U9 = CDP1866CE
U12, U16 = MWS5114
U20, U38 = resistor module, 22 kΩ, 14 pin
U21 = CD4001BE
U23 = CDP1858CE
U28, U29 = CD4012BE
U30 = CD4016BE
U31, U32 = CD4050BE
U33 = CD4025BE
U34 = CD4013BE
U35 = CD4023UBE
U39 = CDP1805CE
U40 = CD4093BE
U42 = resistor module, 22 kΩ, 16 pin
U43 = resistor module SIP, 22 kΩ, 10-pin
U44 = resistor, module SIP, 8-pin

XU3, XU39 = 40-pin socket
XU24-XU27 = 24-pin socket
Y1 = 2.00-MHz crystal



Layout diagram of RCA COSMAC Microboard Computer CDP18S603.

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Table VIII–List of Links and Their Functions

LK4	ROM Type Selection
*1:18	ROM Type 2758, 2716
2:17	ROM Type 2708
3:16	ROM Type 2758, 2708, or CDP1834
*4:15	ROM Type 2716
*5:14	ROM Type 2716
6:13	ROM Type 2758, 2708, or CDP1834
7:12	ROM Type 2708
*8:11	ROM Type 2716
9:10	ROM Type 2758
LK10	**ROM Decoding for XU24 and XU25**
*1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
*5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12
LK11	**RAM Decoding**
1:16	$\overline{A15}$•$\overline{A14}$
*2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
*5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12
LK22	**ROM Decoding for XU26 and XU27**
*1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
5:12	$\overline{A13}$•$\overline{A12}$
*6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12
LK36	
1:16	Not applicable to CDP1802 or CDP1805
*2:15	CLEAR-N
3:14	Not applicable to CDP1802 or CDP1805
*4:13	WAIT-N
¢5:12	RNU-P from P1-3
6:11	RNU-P from P1-12 (CDS installation only)
7:10	EF3 for serial interface in
¢8:9	EF4 for serial interface in
LK37	
*A:B	+5 V V_{DD} to CDP1802
LK41	
A:B	Interrupt from PIO
LK43	
*A:B	Microboard system installation (EF4-N)
*C:D	Microboard system installation (+12 V)
A:D	CDS installation (+12 V)
B:C	CDS installation (EF4-N)

*Preprinted links
¢Wire jumpers installed

Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+ 5V
31	EF2-N	32	– 5V/– 15V
33	EF1-N	34	+ 12V/+ 15V

Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

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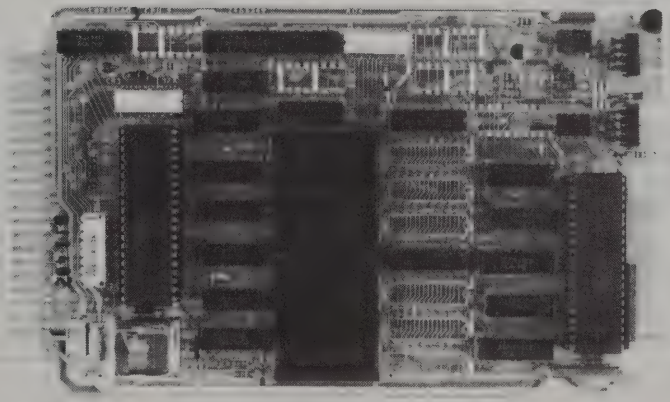
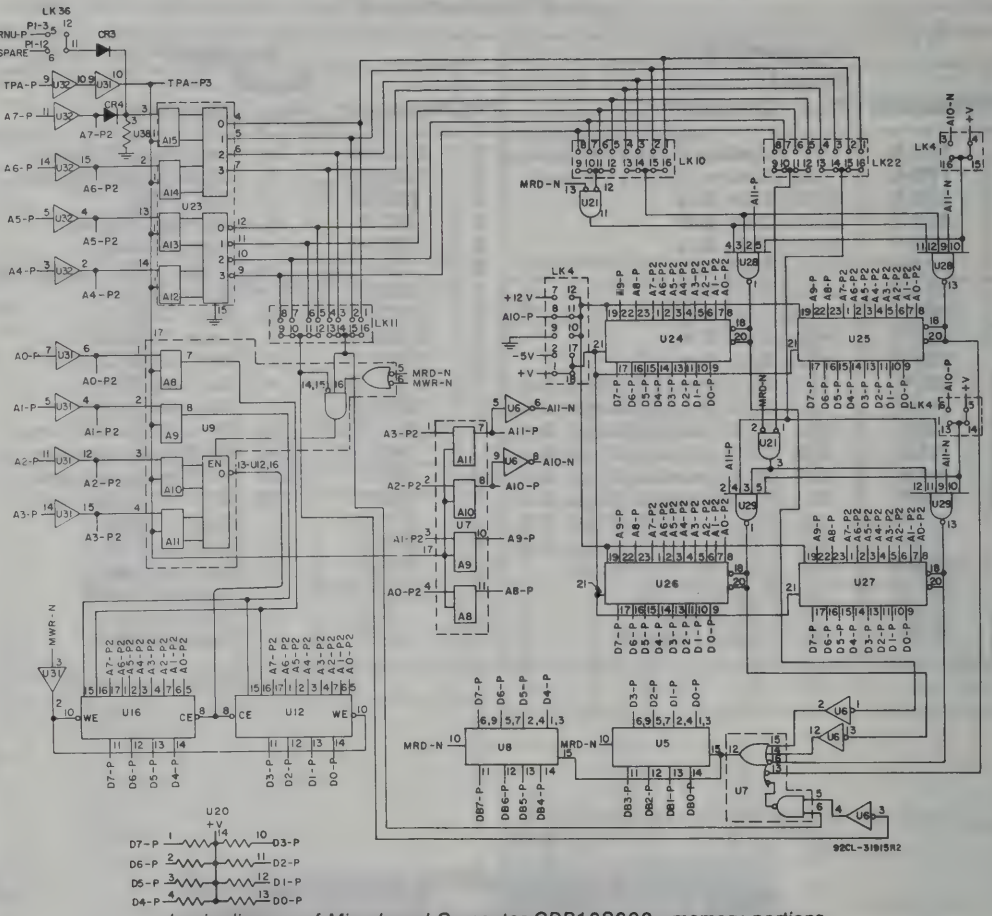
Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector [P1]

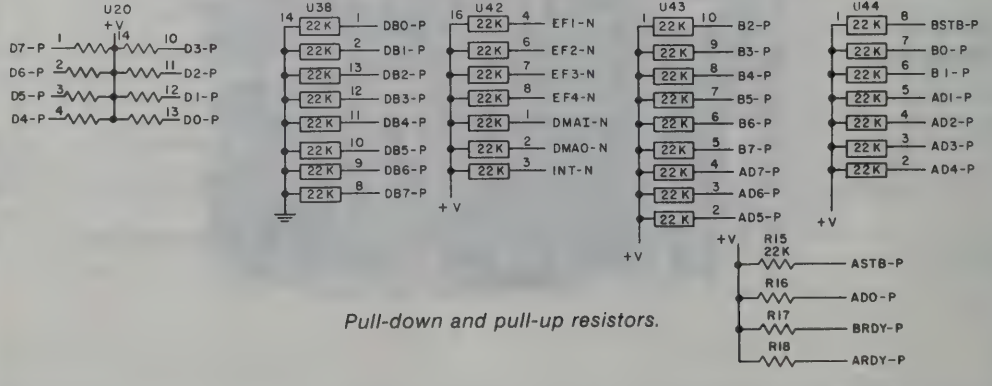
Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility
D	DB1-P	In/Out	Data Bus	4	INT-P	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Control
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Control
M	A0-P	Out	Multiplexed Address Bus	11	−5 V/−15 V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V	In	+5 volts dc	21	+5 V	In	+5 volts dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground



CDP18S603



Logic diagram of Microboard Computer CDP18S603—memory portions.



Pull-down and pull-up resistors.

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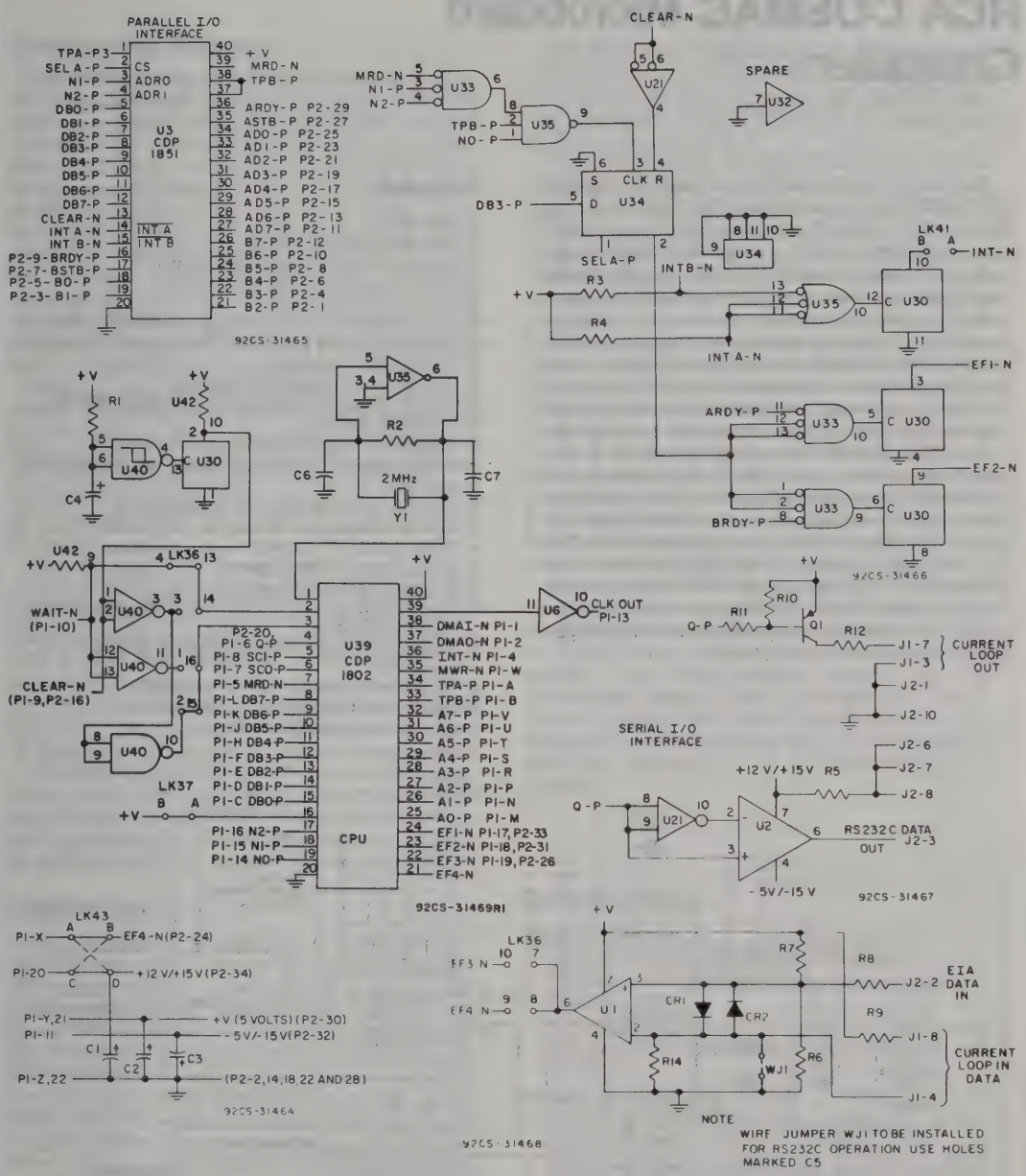

Logic diagram of Microboard Computer CDP18S603—CPU and interface portions.

CDP18S604B
RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP18S604B is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, programmable timer, power-on reset, and a breadboard for user-added features and interfaces. An on-board socket is provided for read-only memory enabling the user to select up to 4 kilobytes of mask-programmable ROM or EPROM depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S604B Microboard Computer is designed to provide at low cost the key hardware for various microcomputer applications thereby enabling the designer to concentrate on the software and the special requirements of his specific application. The CDP18S604B is plug-in compatible with the RCA COSMAC Development System CDP18S005 and the RCA COSMAC DOS Development System CDP18S007, facilitating prototype design and the debugging of both hardware and software.

Features

- Low cost
- Low-power static CMOS
- Operable from single 5-volt supply
- Current required: 4 mA (typ.)†
- High noise immunity
- Crystal-clock CPU frequency of 2.097152 MHz
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 1024 bytes of read/write memory
- Socket for up to 4 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Programmable wide-range timer or retriggerable one-shot
- Flexible memory and I/O expansion
- 8 parallel input and 8 parallel output lines
- 4 flag inputs; Q output
- 65,536-byte memory space
- 44-pin system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Powered through either expansion or I/O connector
- Temperature range: –40°C to +85°C
- Small board size: 4.5 x 7.5 inches
- User area for breadboarding

†With CMOS ROM

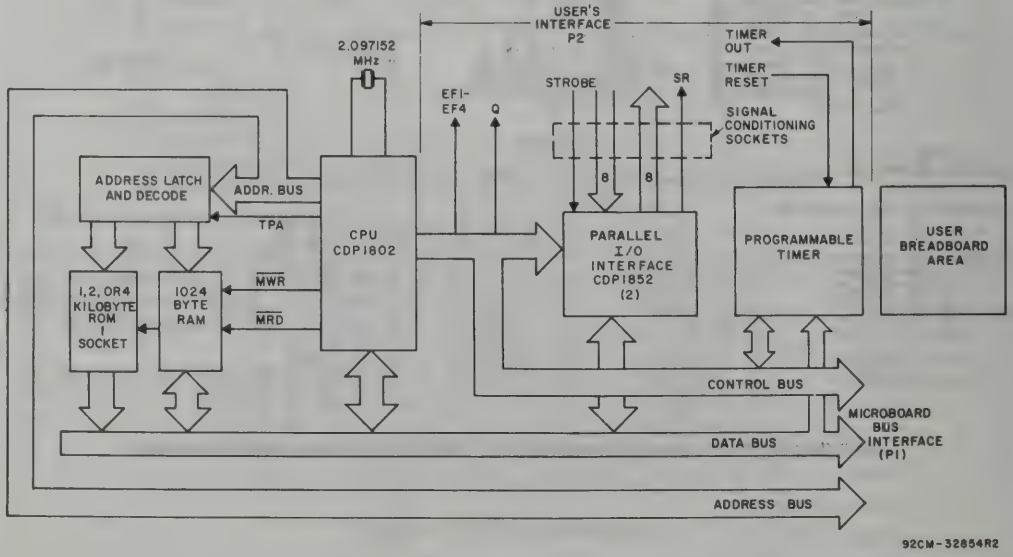

Fig. 1 — Block Diagram of RCA COSMAC Microboard Computer CDP18S604B

CDP18S604B

Component Features

Central Processing Unit. The central processor for the CDP18S604B Microboard Computer is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. The CDP18S604B provides 1024 bytes of CMOS read-write memory. In addition, a socket is provided for one, two, or 4 kilobytes of nonvolatile read-only memory. RCA CDP1832 or CDP1834 mask-programmed CMOS ROM's or 2758, 2716, or 2732 EPROM's may be used in this socket. The memory type selected may be placed independently in the 65,536-byte memory space.

I/O. By means of two parallel I/O ports, type CDP1852, the CDP18S604B provides eight input and eight output lines. Each port has a handshaking line to indicate whether a byte has been written to or read from a port. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. The user's edge connector provides, in addition to the two 8-line input and output ports, access to four flags, Q, timer output and control, and system clear.

A programmable timer provides a means for generating periodic interrupt, a square-wave output or a programmable, retriggerable one-shot for either interrupt or external use. The start and retrigger signal may be generated either by software or external signal.

Application

The COSMAC Microboard Computer CDP18S604B may stand alone and be operated as a complete system. It may also be operated in conjunction with other Microboard Systems Components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 22-card Microboard Chassis (CDP18S670). The user breadboard area provides over four square inches of space for custom designs in addition to DIP locations for signal conditioning the I/O ports. Power may be supplied through the Microboard Bus Interface connector or through the I/O connector.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S604B Microboard Computer may be installed in the card nest of the COSMAC Development System CDP18S005 CDS II or the COSMAC DOS Development System CDP18S007 CDS III in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When the CDP18S604B Microboard Computer is used with the Microboard Control and Display Module CDP18S640 some debugging capability is available even in such a two-card minimum system. By means of the control switches provided with the CDP18S640 (RESET, RUN PROGRAM, RUN UTILITY, and STEP/CONT) and the six-digit hexadecimal display, the operator can observe the address and data sequences of both the fetch and execute cycles.

Specifications

Memory Capacity

On-board RAM: 1024 bytes

On-board ROM/EPROM: 1 socket for up to 4 kilobytes

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM

Memory Address Map

On-board RAM: 1024 bytes assignable to any 1-kilobyte block.

Links are factory installed for RAM at address 4000_{16}.

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Specifications (Continued)

On-board ROM/EPROM:
For CDP1832, 512 bytes assignable to any 1-kilobyte block.
ROM will "wrap" in low and high half of assigned space.
For CDP1834 or 2758, 1 kilobyte on any 1-kilobyte boundary. Links are preprinted for ROM 2716 at address 0000.
For 2716, 2 kilobytes on any 2-kilobyte boundary.
For 2732, 4 kilobytes on any 4-kilobyte boundary.

I/O Capacity
Parallel: 8 input lines and 8 output lines with handshaking for each port.

Timer
A programmable one- to-24 stage counter, having a period of 7.6 us to 64 seconds which may be used as a retriggerable one-shot or a square-wave generator, with a programmable pause feature. Programmed or external start/stop.

Operating Temperature Range
–40°C to +85°C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
With CMOS ROM's: +5 V at 4 mA, typical operating

Connectors
System Interface: Edge fingers, 44 pins on 0.156-inch centers
Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers

Clock
CPU and Timer crystal-controlled 2.097152-MHz oscillator.

Microboard Bus Interface Signals
(Connector P1, See Table 8)

The following signals, are generated or received by the COSMAC Microboard Computer CDP18S604B and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802A (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.**

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high, $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O. Available to user for I/O expansion at connector P1 (P1-14, P1-15, P1-16).

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$ External Flags — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The service request line from the input port is gated to EF3 by the group select signal through an open drain device.

$\overline{INT}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

The service request line from the input port can be connected through link LK36, pins 2:3 to the interrupt input. The timer can be connected through link LK36, pins 1:4 to the interrupt input. These two interrupts are distinguished by testing EF2 for timer and EF3 for input port. Of course, the proper group select must be set. (See section on I/O addressing.)

All connections to INT and the external flags should be through an open drain, open collector, or other high-impedance device, so that other boards may wire "OR" into these lines.

The conventional implementation of INTERRUPT I/O is to have each interrupting device identify itself by means of flag (EF1, EF2, EF3, or EF4) gated by its group select. In this way, the software may identify an interrupting device by polling the assigned group numbers, establishing priority by the order of polling.

$\overline{DMAI}$, $\overline{DMAO}$ — Taken directly to the CPU pins and not utilized by the CDP18S604B, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an

S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch.the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S604A buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge, when data lines are stable.

$\overline{\text{MRD}}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. It is available for use through the Microboard Bus (P1) and Parallel I/O (P2) connectors and may be used to implement a serial output port. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A 2.097152-MHz square-wave clock signal derived from the CDP1802A crystal-controlled oscillator.

WAIT, CLEAR — Two control inputs to the CPU that determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	Mode
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA-IN requests then load memory starting from location zero for as many bytes as there are DMA-IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and O's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to CLEAR.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the

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CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S604B to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000. When the CDP18S604B is used in a stand-alone mode with a utility program located at 8000_{16}, an RNU-P signal must be supplied to connector P1-3 and Pins 7:10 must be connected on link LK6. When the CDP18S604B is used with Control and Display Module CDP18S640, only pins 7:10 on link LK6 need be connected.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard DIP dimensions.

RAM Address — The 1-kilobyte RAM may be placed in any 1-kilobyte location within the 64-kilobyte memory space. Bits A4, A5, A6, and A7 are latched, at TPA trailing edge, in the CDP1858 (U17) becoming A12, A13, A14 and A15 of the high-order address byte. Bits A3 and A2 are latched in the CDP1867 (U16) becoming A10 and A11 of the high-order address.

Bits A15 and A14 are decoded into one of the 4 lines to link LK24, and A13 and A12 into 4 additional lines to LK24. One link for each pair of bits combined by gates in U11 and U12 provides a 4-kilobyte decode. Bits A10 and A11 inputs to the same gates provide the required 1-kilobyte decode which drives the RAM chips and the memory buffer drivers.

See Table 2 for detailed linking instructions.

ROM Address — One 24-pin socket is provided to accommodate various ROM types. Link LK31 is used to select the ROM type, links LK30, LK33 and LK25 are used to place the ROM in any place in memory space. ROM types which may be used are 2732 (4 kilobytes), 2716 (2 kilobytes), 2758 (1 kilobyte), CDP1834 (1 kilobyte) and CDP1832 (512 bytes; will wrap within a 1-kilobyte address space).

Link LK25 is used to establish the 4-kilobyte space, just as link LK24 does for the RAM. For 4-kilobyte ROM's the LK25 is sufficient. For 2-kilobyte ROM's the CDP1866 (U32) latches bit A11 and link LK30 selects the polarity for the ROM chip enable. For 1-kilobyte ROM's, the CDP1866 (U32) latches and decodes bits A10 and A11 for four lines to link LK30 where one line is chosen as Chip Enable.

See Tables 3 through 5 for linkage for any ROM type.

I/O Operation

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus the number of addresses provided is 15-binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP-18S604B does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

Input Port

The input port has, in addition to the eight data lines, a strobe (STB) line input which will latch the data into the port at its trailing edge. The port is a feed-

through latch, so that when a strobe is not desired, the STB line may be left open or at a high logic level, allowing the data to feed through during the read instruction. If the STB is used, its trailing edge will generate a service request signal which is gated to EF3 by the proper I/O group select. The service request may be linked to the interrupt line if desired. The service request is cleared by reading the port or by power on or system clear.

The input port is pre-linked to I/O group $(08)_{16}$ and is read by an INP2 $(6A)_{16}$ instruction.

Output Port

The output port has, in addition to its eight data lines, a service request (SR) out. This SR goes high after data has been latched into the port and low at the following TPB. The SR pulse may be used to indicate the arrival of a new data byte, or ignored where not required. SR will be initially low, due to power on or system reset.

The output port is pre-linked to I/O group $(08)_{16}$ and is loaded by an OUT 2 $(62)_{16}$ instruction.

Table 2 — Memory Map and Link Connections for RAM

LK 24		LK4	Address
1-16	*5-12	2-7* and 4-5*	0000-03FF
		1-8 and 4-5	0400-07FF
		2-7 and 3-6	0800-0BFF
		1-8 and 3-6	0C00-0FFF
	6-11	2-7* and 4-5*	1000-13FF
		1-8 and 4-5	1400-17FF
		2-7 and 3-6	1800-1BFF
		1-8 and 3-6	1C00-1FFF
	7-10	2-7* and 4-5*	2000-23FF
		1-8 and 4-5	2400-27FF
		2-7 and 3-6	2800-2BFF
		1-8 and 3-6	2C00-2FFF
	8-9	2-7* and 4-5*	3000-33FF
		1-8 and 4-5	3400-37FF
		2-7 and 3-6	3800-3BFF
		1-8 and 3-6	3C00-3FFF
*2.15	*5-12	2-7* and 4-5*	4000-43FF
		1-8 and 4-5	4400-47FF
		2-7 and 3-6	4800-4BFF
		1-8 and 3-6	4C00-4FFF
	6-11	2-7* and 4-5*	5000-53FF
		1-8 and 4-5	5400-57FF
		2-7 and 3-6	5800-5BFF
		1-8 and 3-6	5C00-5FFF
	7-10	2-7* and 4-5*	6000-63FF
		1-8 and 4-5	6400-67FF
		2-7 and 3-6	6800-6BFF
		1-8 and 3-6	6C00-6FFF
	8-9	2-7* and 4-5*	7000-73FF
		1-8 and 4-5	7400-77FF
		2-7 and 3-6	7800-7BFF
		1-8 and 3-6	7C00-7FFF

LK24		LK4	Address
3-14	*5-12	2-7* and 4-5*	8000-83FF
		1-8 and 4-5	8400-87FF
		2-7 and 3-6	8800-8BFF
		1-8 and 3-6	8C00-8FFF
	6-11	2-7* and 4-5*	9000-93FF
		1-8 and 4-5	9400-97FF
		2-7 and 3-6	9800-9BFF
		1-8 and 3-6	9C00-9FFF
	7-10	2-7* and 4-5*	A000-A3FF
		1-8 and 4-5	A400-A7FF
		2-7 and 3-6	A800-ABFF
		1-8 and 3-6	AC00-AFFF
	8-9	2-7* and 4-5*	B000-B3FF
		1-8 and 4-5	B400-B7FF
		2-7 and 3-6	B800-BBFF
		1-8 and 3-6	BC00-BFFF
4-13	*5-12	2-7* and 4-5*	C000-C3FF
		1-8 and 4-5	C400-C7FF
		2-7 and 3-6	C800-CBFF
		1-8 and 3-6	CC00-CFFF
	6-11	2-7* and 4-5*	D000-D3FF
		1-8 and 4-5	D400-D7FF
		2-7 and 3-6	D800-DBFF
		1-8 and 3-6	DC00-DFFF
	7-10	2-7* and 4-5*	E000-E3FF
		1-8 and 4-5	E400-E7FF
		2-7 and 3-6	E800-EBFF
		1-8 and 3-6	EC00-EFFF
	8-9	2-7* and 4-5*	F000-F3FF
		1-8 and 4-5	F400-F7FF
		2-7 and 3-6	F800-FBFF
		1-8 and 3-6	FC00-FFFF

*Factory-installed link connections

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Table 3 — Memory Map and Link Connections for ROM Types CDP1834 and 2758

LK31		LK33	LK25		LK30		Address
For 2758 1-10 and 4-7	For 1834 "DON'T CARE"	1-8 and 3-6	*1-16	*5-12	6-9	*1-14	0000-03FF
						2-13	0400-07FF
						3-12	0800-0BFF
						4-11	0C00-0FFF
				6-11		*1-14	1000-13FF
						2-13	1400-17FF
						3-12	1800-1BFF
						4-11	1C00-1FFF
				7-10		*1-14	2000-23FF
						2-13	2400-27FF
						3-12	2800-2BFF
						4-11	2C00-2FFF
				8-9		*1-14	3000-33FF
						2-13	3400-37FF
						3-12	3800-3BFF
						4-11	3C00-3FFF
			2-15	*5-12		*1-14	4000-43FF
						2-13	4400-47FF
						3-12	4800-4BFF
						4-11	4C00-4FFF
				6-11		*1-14	5000-53FF
						2-13	5400-57FF
						3-12	5800-5BFF
						4-11	5C00-5FFF
				7-10		*1-14	6000-63FF
						2-13	6400-67FF
						3-12	6800-6BFF
						4-11	6C00-6FFF
				8-9		*1-14	7000-73FF
						2-13	7400-77FF
						3-12	7800-7BFF
						4-11	7C00-7FFF
			3-14	*5-12		*1-14	8000-83FF
						2-13	8400-87FF
						3-12	8800-8BFF
						4-11	8C00-8FFF
				6-11		*1-14	9000-93FF
						2-13	9400-97FF
						3-12	9800-9BFF
						4-11	9C00-9FFF
				7-10		*1-14	A000-A3FF
						2-13	A400-A7FF
						3-12	A800-ABFF
						4-11	AC00-AFFF
				8-9		*1-14	BC00-B3FF
						2-13	B400-B7FF
						3-12	B800-BFFF
						4-11	BC00-BFFF

*Preprinted link connections.

Table 3 — Memory Map and Link Connections for ROM Types CDP1834 and 2758 -Cont'd

LK31		LK33	LK25		LK30		Address
For 2758 1-10 and 4-7	For 1834 "DON'T CARE"	1-8 and 3-6	4-13	*5-12	6-9	*1-14	C000-C3FF
						2-13	C400-C7FF
						3-12	C800-CBFF
						4-11	CC00-CFFF
				6-11		*1-14	D000-D3FF
						2-13	D400-D7FF
						3-12	D800-DBFF
						4-11	DC00-DFFF
				7-10		*1-14	E000-E3FF
						2-13	E400-E7FF
						3-12	E800-EBFF
						4-11	EC00-EFFF
				8-9		*1-14	F000-F3FF
						2-13	F400-F7FF
						3-12	F800-FBFF
						4-11	FC00-FFFF

*Preprinted link connections.

Timer

The timer is programmed by a control byte transmitted by an OUT 3 $(63)_{16}$ instruction, with I/O group $(08)_{16}$ selected.

The timer consists of a divide-by-eight prescaler CD4018BE driven by the 2.097152 MHz clock. The prescaler output goes to the CD4536BE (U13) counter which is a 24-stage binary counter with control inputs. The output of the CD4536BE counter drives a "D"-type flip-flop which in turn is gated to EF2 by the group select and also may be linked to the interrupt through link LK36 pins 1 and 4. The CD4536BE timer output is also provided on the user connector P2 pin 9.

Loading the control register resets the "D"-type flip-flop which generates EF2 flag and interrupt signal INT, so that interrupt or branch service should re-load the control register in order to remove the INT and flag EF2.

The timer control register provides the following control functions (See Fig. 2 Programmable-Timer-Control Word Definition).

Bits 0 through 3 — The low-order four bits select the timer output to be one of the 16 high-order bits of the counter.

Bit 4 — Causes the low-order eight stages of the counter to be by-passed, in effect reducing it from a 24-bit to a 16-bit counter.

Bit 5 — Sets all stages of the counter, including the output.

Bit 6 — Resets all stages of the counter, including the output.

Bit 7 — Pause. While bit 7 is true, counting is suspended without disturbing the current value. When bit 7 is cleared, counting resumes.

Square-Wave Generation — A square wave may be generated by setting bits 0 through 4 to the period desired with bits 5, 6 and 7 zeros. If interrupt is linked, the interrupt period will be a full period of the square wave as will EF2. Reset (bit 6 or pin P2-14) or Set (bit 5) may be used to stop at any time and restart in a known state (all zeros or all ones). (Note that after a Reset, the first interrupt is a full period but after a Set, the first interrupt is a half period, then a full period thereafter.) Pause (bit 7) may be used at any time to leave the counter in its present state until bit 7 is cleared, then resume.

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Table 4 — Memory Map and Link Connections for ROM Type 2716

LK31	LK25		LK33	LK30		Address
					*1-14	0000-07FF
		*5-12			2-13	0800-0FFF
					*1-14	1000-17FF
	*1-16	6-11			2-13	1800-1FFF
					*1-14	2000-27FF
		7-10			2-13	2800-2FFF
					*1-14	3000-37FF
		8-9			2-13	3800-3FFF
					*1-14	4000-47FF
		*5-12			2-13	4800-4FFF
					*1-14	5000-57FF
	2-15	6-11			2-13	5800-5FFF
					*1-14	6000-67FF
		7-10			2-13	6800-6FFF
					*1-14	7000-77FF
*2-9		8-9	*2-7		2-13	7800-7FFF
and			and	6-9	*1-14	8000-87FF
4-7		*5-12	4-5		2-13	8800-8FFF
					*1-14	9000-97FF
	*1-16	6-11			2-13	9800-9FFF
					*1-14	A000-A7FF
		7-10			2-13	A800-AFFF
					*1-14	B000-B7FF
		8-9			2-13	B800-BFFF
					*1-14	C000-C7FF
		*5-12			2-13	C800-CFFF
					*1-14	D000-D7FF
	2-15	6-11			2-13	D800-D7FF
					*1-14	E000-E7FF
		7-10			2-13	E800-EFFF
					*1-14	F000-F7FF
		8-9			2-13	F800-FFFF

*Preprinted link connections.

Table 5 — Memory Map and Link Connections for ROM Type CDP2732.

LK30	LK33	LK31	LK25		Address
5-10 and 7-8	"DON'T CARE"	2-9 and 5-6	*1-16	*5-12	0000-0FFF
				6-11	1000-1FFF
				7-10	2000-2FFF
				8-9	3000-3FFF
			2-15	*5-12	4000-4FFF
				6-11	5000-5FFF
				7-10	6000-6FFF
				8-9	7000-7FFF
			3-14	*5-12	8000-8FFF
				6-11	9000-9FFF
				7-10	A000-AFFF
				8-9	B000-BFFF
			4-13	*5-12	C000-CFFF
				6-11	D000-DFFF
				7-10	E000-EFFF
				8-9	F000-FFFF

*Preprinted link connections.

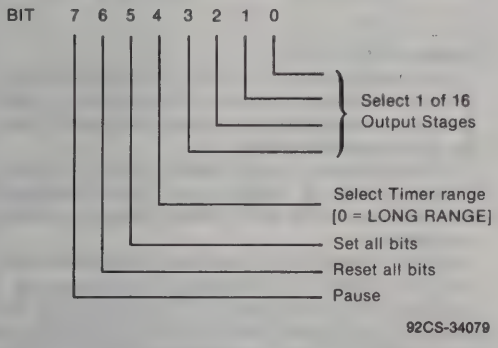

Fig. 2 — Programmable-timer-control word definition

One-Shot Method — Software release of Reset (bit 6) or hardware release of Reset (P2-14) starts the count at zero and when the stage selected by bits 0 through 4 is clocked true TIMER OUT-P goes high. When the stage is clocked false, TIMER OUT-P goes low and INT and EF2 are enabled. Either hardware or software can then do a reset to end the one-shot cycle. See Figs. 3a and 3b. If Set (bit 5) is used instead of Reset the cycle is the same except that it starts with TIMER-OUT-P going high and INT and EF2 are set after a half period. Pause (bit 7) may be used at any time to stop counting without resetting.

A retrigger function can be done before time out by asserting Reset or Set by either hardware or software. See Fig. 3b.

Another one-shot method uses an RC time constant to limit the duration of the TIMER-OUT signal. Replacing R6 with a capacitor and adding R5 causes the TIMER-OUT signal to be reset after the end of the RC time period. INT and EF2 are generated at the trailing edge of TIMER OUT. Unless Reset or Set are asserted, the counter continues to count its full period. The width of the positive timer output using this monostable option is poorly regulated. R5 should be greater than 2 kΩ, R5=10 kΩ and C4=1000 pF will give about 3 μs. (See Fig. 6.)

Machine Cycle Timing — The timer and the CPU share the 2.097152 MHz clock. Therefore, a definite relationship may be established between the counter and the CPU/software timing. Both the CPU TP generator and the counter pre-scaler are eight state devices, so that the timer is incremented once per ma-

CDP18S604B

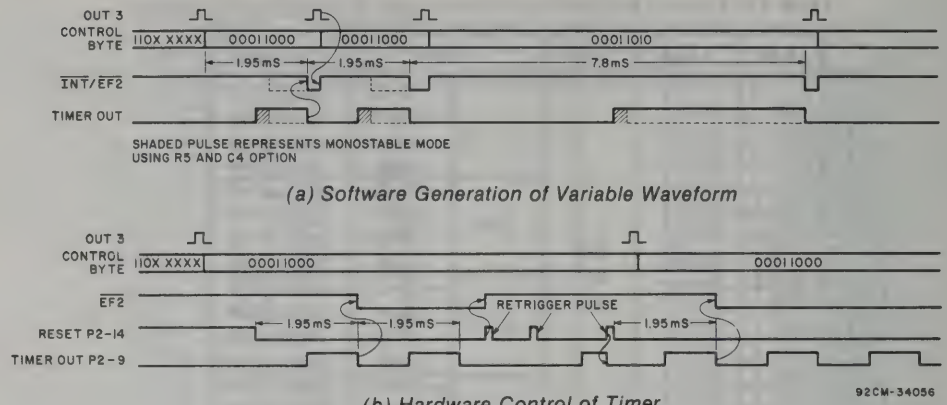

Fig. 3 — Timer waveforms of RCA COSMAC Microboard Computer CDP18S604B

chine cycle, unless WAIT states are encountered, in which case the timer continues in real time while the CPU pauses.

In order to establish a known relationship between timer and CPU, the RESET and PAUSE bits in the control word are used together. When the two bits are cleared during the TPB of the execute cycle of the OUT3, the CD4018BE pre-scaler will generate the first increment to the timer three clock periods later and thereafter every eight clock periods. Because of the variance of propagation delays, a minus zero plus one clock period (2.097152 MHz) uncertainty exists in the phase relationshp of the counter input and the machine cycles.

The timing then is such that the timer increment occurs after TPA of each machine cycle, and before TPB. EF2 is sampled during TPA of the execute cycle of the branch instruction inside the CPU, and INT will be taken after any execute cycle unless a DMA cycle is pending. One can thus calculate how many machine cycles are available for software action before the interrupt occurs or EF2 may be detected.

For long counts, an uncertainty of plus one or two machine cycles should be added, since the ripple time of the counter is long, up to 30 ns per stage. For worst case, one cycle per 10 stages of counter should be added for ripple time.

Use of the PAUSE bit alone allows a time out feature. This time can be an integral number of machine cycles. The counter is started by use of both the RESET and PAUSE bits; both set until the starting 63 command resets them. If the RESET bit alone or the external RESET is used to start, the PAUSE mode may have an uncertainty of plus 8 clock bits (3.8 μs).

Breadboarding Area

The breadboard area is a 16 x 24 matrix of 0.035-inch plated-through holes on 0.10-inch centers. A total of seven holes are missing at corners, leaving 409 holes for mounting components.

To aid the user, some signals needed for Input-Output circuits are brought near to the breadboard area and provided with plated holes for solder attachment.

DB0-P through DB7-P are next to the breadboard area and marked by silkscreen.

N=7-P, N=6-P, N=5-P and N=4-P are next to U7 and marked by silkscreen. These signals are generated by the CDP1853 (U7) and are conditioned by the Group Select 08. Thus these signals provide the complete two-level I/O decoding and their timing is from the trailing edge of TPA to the trailing edge of TPB.

The data lines of the input and output ports are available on links LK2 and LK1, respectively.

+5 Volts may be found adjacent to pin 24 of U5 and ground, adjacent to pin 11 of link LK1.

Table 6 — Setting the Timer Period

Bits 0 through 4 of the control byte determines the period generated by the Timer in all modes. Two ranges are available, determined by Bit 4. When Bit 4 is true; the range is 7.63 us to 250 ms. When Bit 4 is false, the range is 1.95 ms to 64s as shown.

LOW-RANGE CONTROL BITS 4 3 2 1 0	HIGH-RANGE CONTROL BITS 4 3 2 1 0	TIMER PERIOD	TIMER FREQUENCY Hz
1 0 0 0 0		7.629 μs	131,072
1 0 0 0 1		15.26 μs	65,536
1 0 0 1 0		30.52 μs	32,768
1 0 0 1 1		61.04 μs	16,384
1 0 1 0 0		122.1 μs	8192
1 0 1 0 1		244.1 μs	4096
1 0 1 1 0		488.3 μs	2048
1 0 1 1 1		976.6 μs	1024
1 1 0 0 0	0 0 0 0 0	1.953 ms	512
1 1 0 0 1	0 0 0 0 1	3.906 ms	256
1 1 0 1 0	0 0 0 1 0	7.813 ms	128
1 1 0 1 1	0 0 0 1 1	15.63 ms	64
1 1 1 0 0	0 0 1 0 0	31.25 ms	32
1 1 1 0 1	0 0 1 0 1	62.5 ms	16
1 1 1 1 0	0 0 1 1 0	125 ms	8
1 1 1 1 1	0 0 1 1 1	250 ms	4
	0 1 0 0 0	500 ms	2
	0 1 0 0 1	1.0 s	1
	0 1 0 1 0	2.0 s	0.5
	0 1 0 1 1	4.0 s	0.25
	0 1 1 0 0	8.0 s	0.125
	0 1 1 0 1	16.0 s	0.0625
	0 1 1 1 0	32.0 s	0.03125
	0 1 1 1 1	64.0 s	0.015625

Power-On Reset

An RCA integrator (R1 and C1 in the control circuit logic diagram) provides a true CLEAR signal for approximately 100 milliseconds when the +5-volt supply is turned on. This signal drives the CLEAR input to the CPU, the parallel I/O interface, and the I/O group select latch. After the CLEAR signal, the I/O group select is reset, the output port and its SR is reset, and the input port goes to a high-impedance state with SR reset. The CPU initializes and starts processing at location 0000 provided the WAIT line is not asserted.

External circuits may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C1 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development Systems CDP18S005 and CDP18S007

Replacement of CDS CPU Module CDP18S102 or CDP18S102V1 with the RCA COSMAC Microboard Computer CDP18S604B requires some link changes on the CDP18S604B. These changes are:

LK34 — Cut A:B and C:D and install B:C. Install A:D only if a connection to the plus auxiliary voltage is

CDP18S604B

needed on P2 or the breadboard area.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK35 — RNU to start ROM's at address 8000. Connect a wire jumper between 1 and 4 on link LK35, and remove the wire jumper between 2 and 3. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000_{16} after the RESET, RUN U switches are pressed. The wire jumper to the CDS backplane should be removed before the CDP18S102 is reinstalled.

Memory Address Links. The desired memory addresses should be set up according to the memory maps of Tables 2 through 5. Care should be taken that the CDS memories are not assigned to overlap the assignment of the CDP18S604B Microboard Computer.

Connector Matching Cables Available Separately

CDP18S517 — I/O Interface Cable

Fits connector P2; 36 inches long; 34-pin flat ribbon cable; output end unterminated.

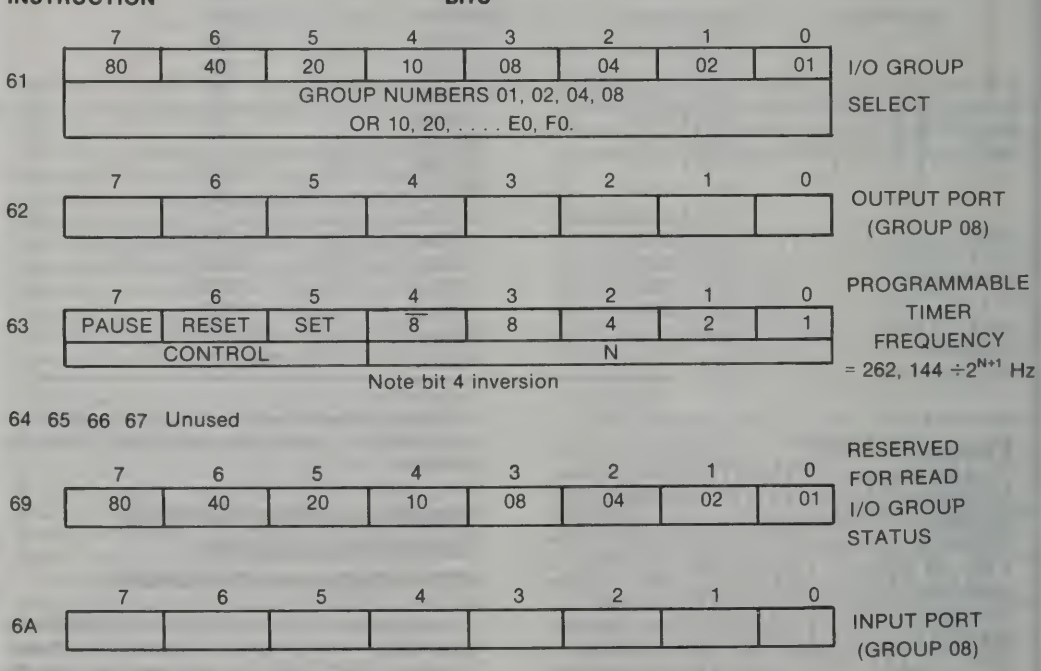

Fig. 4 — Programmers I/O Reference for RCA COSMAC Microboard Computer CDP18S604B.

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Table 7 — List of Links and Their Functions

LK1 OUTPUT PORT

†2:19	DO3-P	
†3:18	DO2-P	
†4:17	DO1-P	LINKS MAY BE CUT
†5:16	DO0-P	TO INSERT
†6:15	SR-P	RESISTOR NETWORKS
†7:14	DO7-P	OR POWER DRIVERS,
†8:13	DO6-P	SUCH AS SN75498
†9:12	DO5-P	
†10:11	DO4-P	

LK2 INPUT PORT

†1:18	DI4-P	
†2:17	DI5-P	LINKS MAY BE CUT
†3:16	DI6-P	TO INSERT
†4:15	DI7-P	RESISTOR NETWORKS
†5:14	DI0-P	OR OTHER SIGNAL
†6:13	DI1-P	CONDITIONER
†7:12	DI2-P	
†8:11	DI3-P	
†9:10	STB-P	

LK4 RAM DECODING

1:8	A10
*2:7	$\overline{\text{A10}}$
3:6	A11
*4:5	$\overline{\text{A11}}$

LK24 RAM DECODING

1:16	$\overline{\text{A15}}$.$\overline{\text{A14}}$
*2:15	$\overline{\text{A15}}$.A14
3:14	A15.$\overline{\text{A14}}$
4:13	A15.A14
*5:12	$\overline{\text{A13}}$.$\overline{\text{A12}}$
6:11	$\overline{\text{A13}}$.A12
7:10	A13.$\overline{\text{A12}}$
8:9	A13.A12

LK25 ROM DECODING

*1:16	$\overline{\text{A15}}$.$\overline{\text{A14}}$
2:15	$\overline{\text{A15}}$.A14
3:14	A15.$\overline{\text{A14}}$
4:13	A15.A14
*5:12	$\overline{\text{A13}}$.$\overline{\text{A12}}$
6:11	$\overline{\text{A13}}$.A12
7:10	A13.$\overline{\text{A12}}$
8:9	A13.A12

LK30 ROM DECODING

†1:14	1 kilobyte — $\overline{\text{A11}}$-$\overline{\text{A10}}$, 2 kilobytes — $\overline{\text{A11}}$
2:13	1 kilobyte — $\overline{\text{A11}}$-A10, 2 kilobytes — A11
3:12	1 kilobyte — A11-$\overline{\text{A10}}$
4:11	1 kilobyte — A11-A10
5:10	4 kilobytes
†6:9	1 kilobyte, 2 kilobytes
7:8	4 kilobytes

LK31 ROM TYPE SELECTION

1:10	ROM Type 2758
*2:9	ROM Type 2716 or 2732
3:8	NOT USED
*4:7	ROM Type 2758 or 2716
5:6	ROM Type 2732

LK33 ROM DECODING

1:8	1 kilobyte
*2:7	2 kilobytes
3:6	1 kilobyte
*4:5	2 kilobytes

LK34 CDS INSTALLATION

*A:B	
*C:D	

LK35 RNU

1:4	CDS
*2:3	MICROBOARD

*Factory-installed link connections
†Preprinted links

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Table 8 — Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

Table 9 — Microboard Computer CDP18S604B Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	DI2-P	2	GND
3	DI1-P	4	DI3-P
5	DI0-P	6	DI4-P
7	STB-P	8	DI5-P
9	TIMER OUT-P	10	DI6-P
11	DO7-P	12	DI7-P
13	DO6-P	14	TIMER RESET-P
15	DO5-P	16	CLEAR-N
17	DO4-P	18	GND
19	DO3-P	20	Q-P
21	DO2-P	22	SPARE
23	DO1-P	24	EF4-N
25	DO0-P	26	EF3-N
27	SPARE	28	GND
29	SR-P	30	+5 V
31	EF2-N	32	+5 V/−15 V
33	EF1-N	34	+12 V/+15 V

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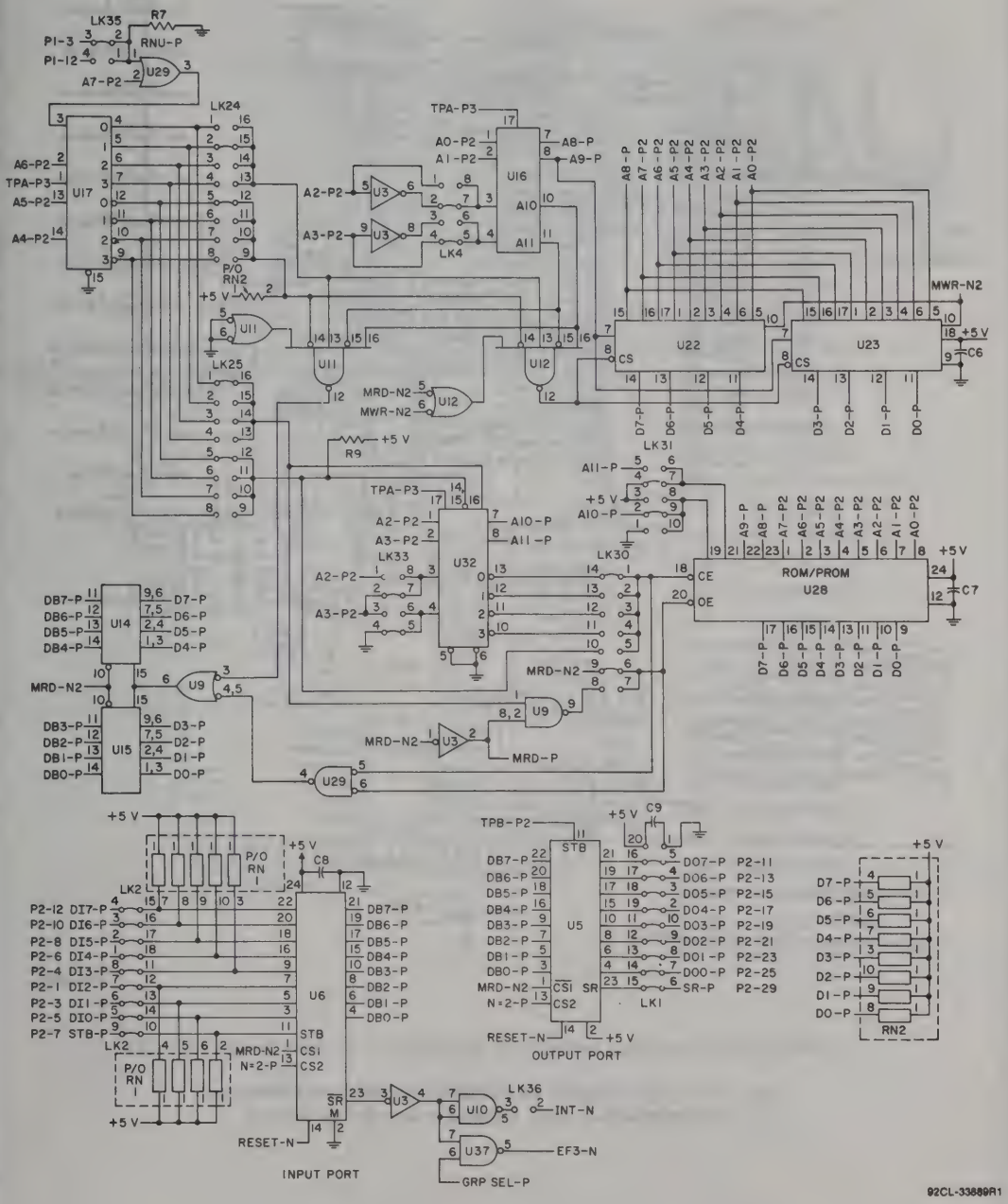


Fig. 5 — Logic Diagram of COSMAC Microboard Computer. CDP18S604B — Memory Portion.

CDP18S604B

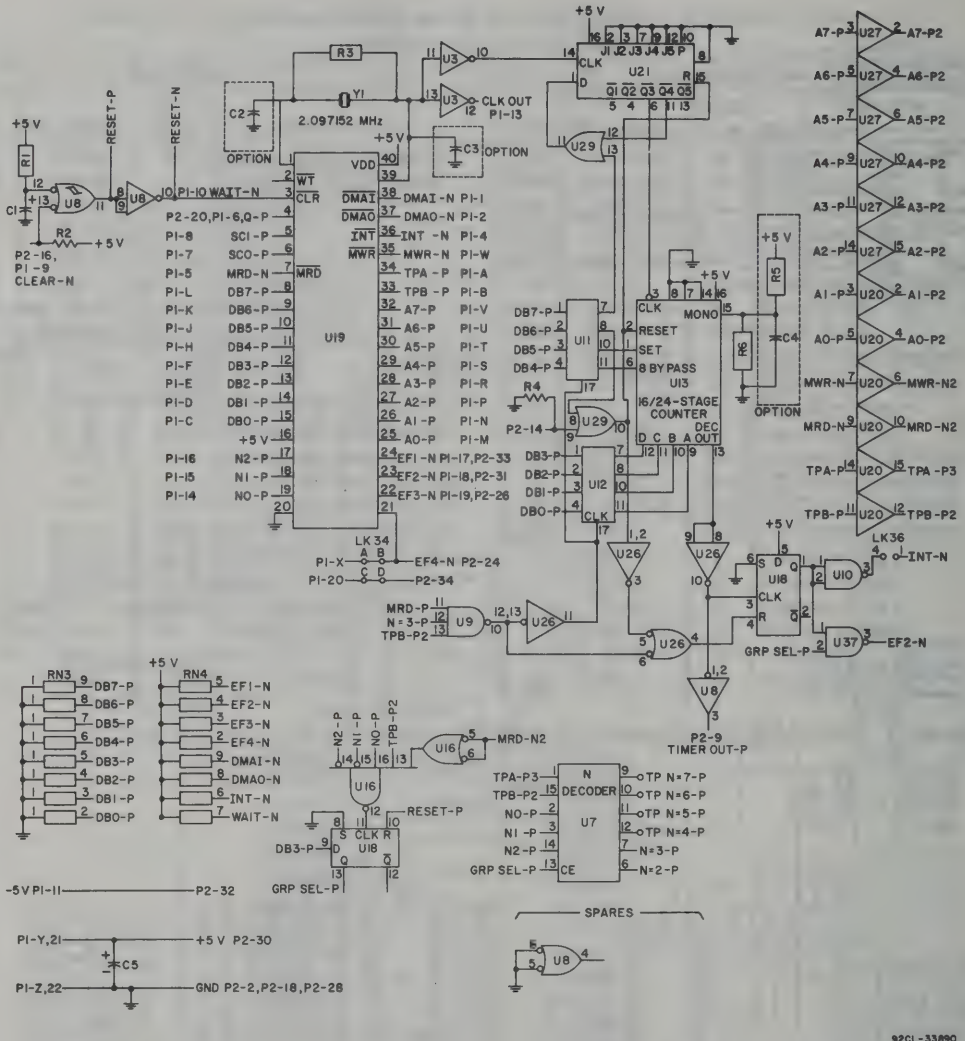
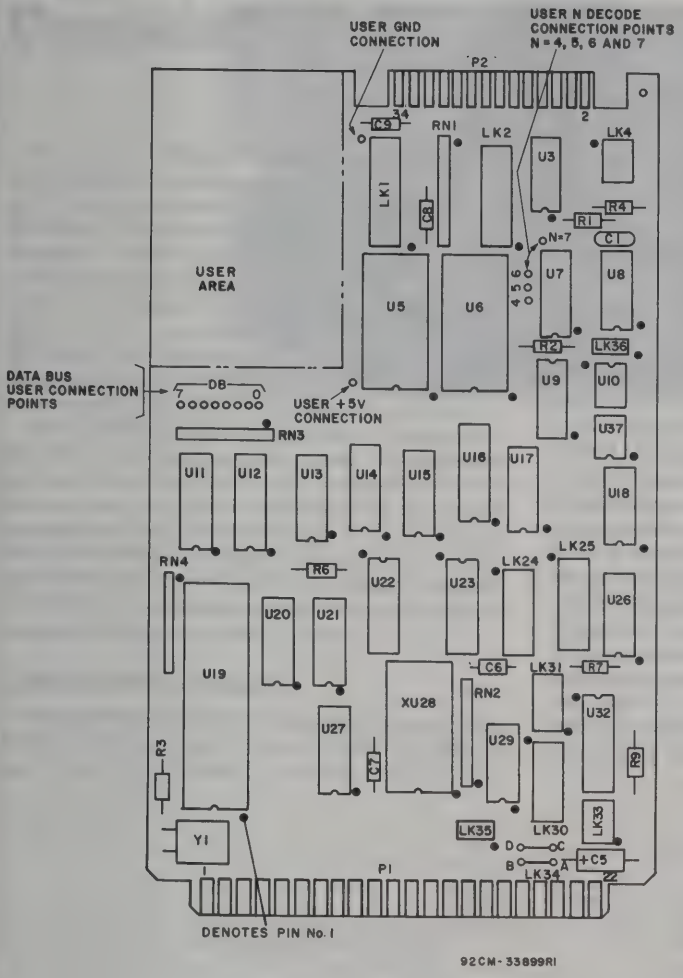


Fig. 6 — Logic Diagram of COSMAC Microboard Computer. CDP18S604B — CPU, Oscillator, and Buffer Portion.

CDP18S604B

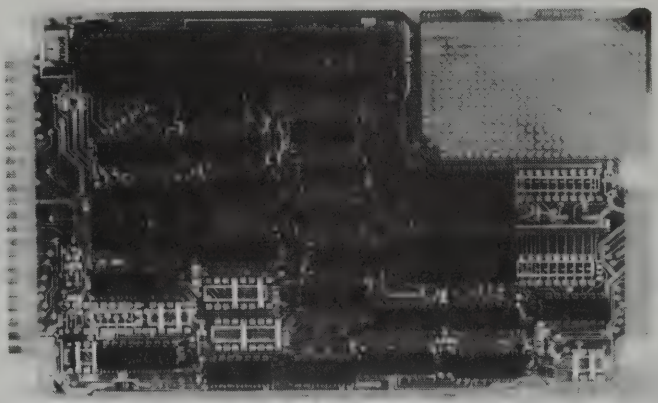


PARTS LIST

C1 = 1.5 uF, 25 V
C5 =22 uF, 100 V
C6-C9 = 0.1 uF, 15 V
R1 = 100 kΩ, 1/4 W, 5%
R2 = 22 kΩ, 1/4 W, 5%
R3 = 22 MΩ, 1/4 W, 5%
R4,R6,R7,R9 = 22 kΩ, 1/4 W, 5%
RN1-RN4 = Resistor Module SIP, 22kΩ, 10-Pin
U3 = CD4069UBE
U5, U6 = CDP1852CE
U7 = CDP1853CE
U8 = CD4093BE
U9 =CD4023UBE
U10 = CD40107BE
U11, U12 = CDP1867CE
U13 = CD4536BE
U14, U15, = CD1856CE
U16 = CDP1867CE
U17 = CDP1858CE
U18 = CD4013BE
U19 = CDP1805CE
U20 = CD4050BE
U21 = CD4018BE
U22, U23 = MWS5114
U26 = CD4011BE
U27 = CD4050BE
U29 = CD4071BE
U32 = CDP1866CE
U37 = CD40107BE
XU19 = 40-Pin Socket
XU28 = 24-Pin Socket
Y1 = Crystal, 2.097152 MHz

Fig. 7 — Layout Diagram of COSMAC Microboard Computer CDP18S604B.

CDP18S604B



CDP18S605

RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP18S605 is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, a UART serial communications interface, power-on-reset, and expansion interface. Two on-board sockets are provided for read-only memory enabling the user to select 2 or 4 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of the CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S605 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and the special requirements of his specific applications. The CDP18S605 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC DOS Development System III CDP18S007, facilitating prototype design and the debugging of both hardware and software.

Component Features

Central Processing Unit. The central processor for the CDP18S605 Microboard Computer is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802.

Features

- **Low-power static CMOS**
- **High noise immunity**
- **Crystal clock—selectable rates: 2.4576, 1.2288, 0.6144 or 0.3072 MHz**
- **Compatible with COSMAC Development Systems**
- **Stand-alone capability**
- **2 kilobytes of read/write memory**
- **Sockets for 2/4 kilobytes of ROM/PROM**
- **Power-on reset**
- **COSMAC Microprocessor architecture**
- **Flexible memory and I/O expansion**
- **UART-driven serial I/O port**
- **14 selectable baud rates: 50 to 19200 baud**
- **RS232C serial I/O**
- **65,536-byte memory space**
- **44-pin system interface**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Powered through either expansion or I/O connector**
- **Wide temperature range: −40° C to 85° C**
- **Small board size: 4.5 x 7.5 inches**

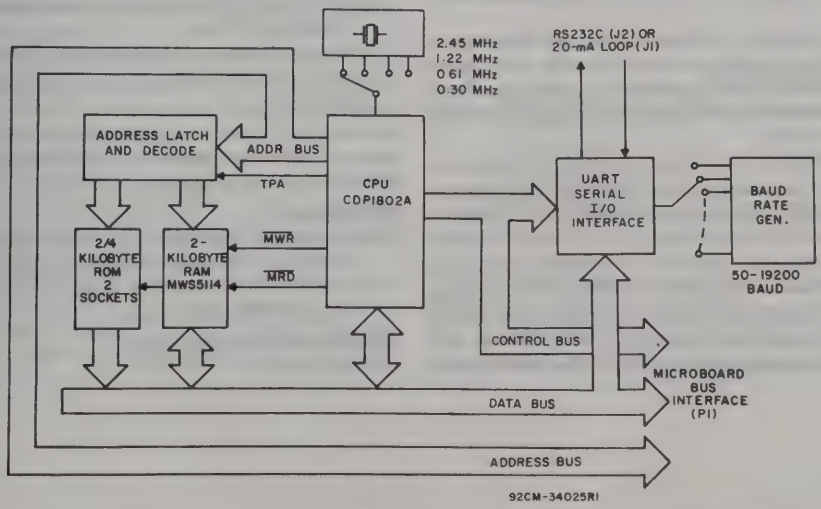


Fig. 1 - Block diagram of RCA COSMAC Microboard Computer CDP18S605.

CDP18S605

The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks and the like. One register each is designated for DMA and interrupt pointers. The CDP1802 provides a serial data-out connection, Q, and four external flag input pins, EF1 through EF4, whose logic levels may be tested with conditional branch instructions.

Memory. By means of four MWS5114 RAM's, the CDP18S605 provides 2 kilobytes of CMOS read-write memory. In addition, two sockets are provided for two or four kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM or 2758 or 2716-type EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on boundaries in accordance with the memory maps given in Tables II through IV.

I/O. A serial communications interface, having an EIA RS232C capability, is driven by an on-board UART, the CDP1854A. Right-angle headers are provided for the serial communications interface.

The data format is determined by software. There are 14 baud rates available, from 50 to 19200 bauds, selectable by a four-rocker DIP switch.

Application

The CDP18S605 may also be operated in conjunction with other Microboard Systems Components installed in any location in the five-card Microboard Chassis (CDP-18S675) or in the 22-card Microboard Chassis (CDP-18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S605 Microboard computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC DOS Development System III CDP18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When the CDP18S605 Microboard Computer is used with the Microboard Control and Display Module CDP18S640V1, some debugging capability is available even in such a two-card minimum system. By means of the control switches provided with the CDP18S640V1 (RESET, RUN PROGRAM, RUN UTILITY, AND STEP/CONT) and the six-digit hexadecimal display, the operator can observe the address and data sequences of both the fetch and execute cycles.

Specifications

Memory Capacity

On-board RAM: 2 kilobytes

On-board ROM/EPROM: 2 sockets for up to 4 kilobytes

Off-board Expansion: Any user-specified combination of RAM, ROM, and EPROM, up to a total of 65,536 bytes on-board and off-board

Memory Address Map

(See Tables II through IV)

On-board RAM: 2 kilobytes contiguous on any 2 kilobyte boundary: Links are preprinted for RAM at address 8800_{16}

On-board ROM and EPROM: For CDP1834 and 2758, 2 kilobytes contiguous on any 2-kilobyte boundary

For 2716, 4 kilobytes contiguous on any 4-kilobyte boundary. Links are preprinted for ROM types CDP1834 and 2758 and for address start at 8000.

I/O Capacity

Serial: UART-controlled input and output lines. EIA RS232C interface. User-programmed data format. 14 selectable baud rates, 50 to 19200 baud. CTS and RTS control lines.

Operating Temperature Range

–40°C to 85°C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
With CMOS ROM's and RS232C: +5 V at 8 mA, typical operating
Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical

Connectors
System Interface: Edge fingers, 44 pins on 0.156-inch centers
Serial I/O: One right-angle header, 10 pins

Clock
CPU and Interface: crystal-controlled oscillator; selectable frequencies: 2.4576, 1.2288, 0.6144, and 0.3072 MHz. A preprinted link selects 2.4576 MHz as the CPU clock frequency.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard Computer CDP18S605 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802A (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

DB7 through DB0—Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2—Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$—Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The UART Serial Data In (SDI) line is gated to EF4 by the UART Group Select through a pre-printed link.

$\overline{INT}$—Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{INT}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter. The interrupt line from the UART can be presented directly to this input via link LK1.

$\overline{DMAI}$, $\overline{DMAO}$—Taken directly to the CPU pins and not utilized by the CDP18S605, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0—State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB—Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

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A7 through A0—Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S605 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$—A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$—A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q—A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. It is available for use through the Microboard Bus (P1) connector. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT—A square-wave clock signal derived from an external crystal-controlled oscillator. One of four clock frequencies can be selected, 2.4576, 1.2288, 0.6144, or 0.3072 MHz. This signal is made available on connectors P1 and P2 by a preprinted link across pins 8 and 5 of link LK8. A preprinted link across pins 7 and 8 of link LK3 selects 2.4576 MHz as the CPU clock frequency.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$—Two control inputs to the CPU that determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA-IN requests then load memory starting from location zero for as many bytes as there are DMA-IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and O's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to CLEAR.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU - Run Utility Software. A signal supplied to the CDP18S605 to force the most significant address bit true. As a result, the program start is at memory location 8000 instead of 0000. When the CDP18S605 is used in a stand-alone mode and a utility program is included at 8000, an RNU-P signal must be supplied to connector P1-3, and pins 12:1 must be connected on link LK8. When the CDP18S605 is used with Control and Display Module CDP18S640V1, the preprinted link LK8 pins 12:1, provides the RNU to the on-board memory decoder. Since the ROM sockets are pre-linked to start at 8000, there would be a conflict with the ROM on the CDP18S640V1, unless the linking is changed to place the on-board RAM and ROM elsewhere in memory space. See Tables I, II, and III.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-

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board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described in Tables I through IV. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The CDP18S605 Microboard Computer has two kilobytes of contiguous memory which can occupy any 2-kilobyte block in memory space on 2-kilobyte boundaries. The high-order byte of the memory address is latched and decoded. Bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two wire jumpers on link LK5. One jumper on link LK4 will enable the next level of decoding; selecting either A11 or A11 inverted enables the RAM decoder U21. If the latched bit A11 is not inverted, the low half of a 4-kilobyte block is enabled. Bit A10 will next select 1-kilobyte segments within the 2kilobyte block.

To set up the RAM address, it is necessary to install two jumpers in link LK5 and one in link LK4 as given in the memory map of Table I. As an alternative, DIP switches may be installed if frequent link changes are anticipated.

To avoid having floating inputs to CMOS gates, links LK5 and LK4 must always have jumpers installed.

Table I - Memory Map and Link Connections for RAM

LK5		LK4	RAM	Address
1:16	*5:12	7:10	U16/U18 U15/U17	0000-03FF 0400-07FF
		*8:9	U16/U18 U15/U17	0800-0BFF 0C00-0FFF
	6:11	7:10	U16/U18 U15/U17	1000-13FF 1400-17FF
		*8:9	U16/U18 U15/U17	1800-1BFF 1C00-1FFF
	7:10	7:10	U16/U18 U15/U17	2000-23FF 2400-27FF
		*8:9	U16/U18 U15/U17	2800-2BFF 2C00-2FFF
	8:9	7:10	U16/U18 U15/U17	3000-33FF 3400-37FF
		*8:9	U16/U18 U15/U17	3800-3BFF 3C00-3FFF
2:15	*5:12	7:10	U16/U18 U15/U17	4000-43FF 4400-47FF
		*8:9	U16/Y18 U15/U17	4800-4BFF 4C00-4FFF
	6:11	7:10	U16/U18 U15/U17	5000-53FF 5400-57FF
		*8:9	U16/U18 U15/U17	5800-5BFF 5C00-5FFF
	7:10	7:10	U16/U18 U15/U17	6000-63FF 6400-67FF
		*8:9	U16/U18 U15/U17	6800-6BFF 6C00-6FFF
	8:9	7:10	U16/U18 U15/U17	7000-73FF 7400-77FF
		*8:9	U16/U18 U15/U17	7800-7BFF 7C00-7FFF

LK5		LK4	RAM	Address
*3:14	*5:12	7:10	U16/U18 U15/U17	8000-83FF 8400-87FF
		*8:9	U16/U18 U15/U17	8800-8BFF 8C00-8FFF
	6:11	7:10	U16/U18 U15/U17	9000-93FF 9400-97FF
		*8:9	U16/U18 U15/U17	9800-9BFF 9C00-9FFF
	7:10	7:10	U16/U18 U15/U17	A000-A3FF A400-A7FF
		*8:9	U16/U18 U15/U17	A800-ABFF AC00-AFFF
	8:9	7:10	U16/U18 U15/U17	B000-B3FF B400-B7FF
		*8:9	U16/U18 U15/U17	B800-BBFF BC00-BFFF
4:13	*5:12	7:10	U16/U18 U15/U17	C000-C3FF C400-C7FF
		*8:9	U16/Y18 U15/U17	C800-CBFF CC00-CFFF
	6:11	7:10	U16/U18 U15/U17	D000-D3FF D400-D7FF
		*8:9	U16/U18 U15/U17	D800-DBFF DC00-DFFF
	7:10	7:10	U16/U18 U15/U17	E000-E3FF E400-E7FF
		*8:9	U16/U18 U15/U17	E800-EBFF EC00-EFFF
	8:9	7:10	U16/U18 U15/U17	F000-F3FF F400-F7FF
		*8:9	U16/U18 U15/U17	F800-FBFF FC00-FFFF

*Preprinted link connections.

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ROM Address. Two 24-pin sockets (XU9 and XU10) are provided for user-programmed ROM's. Three ROM types are suitable: CDP1834 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes). The address decoding technique prevents "wrap-around" in memory space for any memory type.

Table II shows the LK3 and LK4 link connections needed for the ROM selected. Tables III and IV give the additional link connections needed and the memory address information.

Table II - Connections for Link LK3 and LK4 for ROM

Link	CDP1834 or 2758	2716
LK4 1:16*	C	O
LK4 2:15	O	C
LK4 4:13	O	C
LK4 5:12*	X	O
LK4 6:11	X	O
LK3 1:14*	C	O
LK3 2:13	O	C

O=Open; C=Closed; *Preprinted link connections
X=See Table III.

For testing or debugging, all ROM space can be inhibited by connecting A and B on link LK7.

When ROM's CDP1834 or 2758 are used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. One jumper on link LK4 enables the next level of decoding; selecting either A11 or A11 inverted enables ROM decoder U20.

If bit A11 is not inverted, the low half of the 2-kilobyte block is selected. If bit A11 is inverted by U19, the high half of the block is enabled. Another jumper on link LK4 connects bit A10 to the decoder selecting one of the two 1-kilobyte blocks. For the CDP1834 and 2758, input pin 19 of the ROM is grounded. Note that to avoid floating inputs, links LK6 and LK4 must have jumpers installed.

When ROM 2716 is used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. With another jumper connecting pins 2:15 on link LK4, bit A11 now selects 2-kilobyte segments within a 4-kilobyte block. Link LK3 is used to connect address bit A10 to pin 19 of the 2716 ROM.

Note that with type 2716 also, jumpers must always be present to avoid floating inputs to CMOS gates. Note that the CDP18S605 is initially configured for ROM types CDP1834 and 2758 at address 8000.

Input/Output Interfacing

Serial I/O Interfacing. Serial output data is generated by the UART. In Microboard systems including the Control and Display Module CDP18S640V1, the utility software UT61 sets the data format. This format is one start bit, eight data bits (no parity), and two stop bits. The utility also determines when to read data from the UART and when to write to it by reading its status word. The user, of course, has the option in a stand-alone system of writing his own UART routine.

The UART interrupt line is wired to link LK1 where the user may jumper it either to the CPU's interrupt input or to one of the flag lines (EF3) or both. See the data sheet for UART CDP1854A (File No. 1193).

Because the SDI line is connected to EF4 by means of a preprinted link, a break condition may be conveniently detected.

Any one of the 14 baud rates available from the baud rate generator can be selected through a four-bit binary code determined by the setting of a four-rocker DIP switch. The switch settings are given in Table V.

Two-Level I/O Interfacing. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard System the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function. Any I/O function is assigned to a group number and only responds when its group number and its appropriate N register code are transmitted.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded

Table III – Additional Link Connections and Memory Addresses for ROM Types CDP1834 and 2758

LK6	LK4	ROM	Address
1:16	*5:12	U9	0000-03FF
		U10	0400-07FF
	6:11	U9	0800-0BFF
		U10	0C00-0FFF
6:11	*5:12	U9	1000-13FF
		U10	1400-17FF
	6:11	U9	1800-1BFF
		U10	1C00-1FFF
7:10	*5:12	U9	2000-23FF
		U10	2400-27FF
	6:11	U9	2800-2BFF
		U10	2C00-2FFF
8:9	*5:12	U9	3000-33FF
		U10	3400-37FF
	6:11	U9	3800-3BFF
		U10	3C00-3FFF
2:15	*5:12	U9	4000-43FF
		U10	4400-47FF
	6:11	U9	4800-4BFF
		U10	4C00-4FFF
6:11	*5:12	U9	5000-53FF
		U10	5400-57FF
	6:11	U9	5800-5BFF
		U10	5C00-5FFF
7:10	*5:12	U9	6000-63FF
		U10	6400-67FF
	6:11	U9	6800-6BFF
		U10	6C00-6FFF
8:9	*5:12	U9	7000-73FF
		U10	7400-77FF
	6:11	U9	7800-7BFF
		U10	7C00-7FFF
*3:14	*5:12	U9	8000-83FF
		U10	8400-87FF
	6:11	U9	8800-8BFF
		U10	8C00-8FFF
6:11	*5:12	U9	9000-93FF
		U10	9400-97FF
	6:11	U9	9800-9BFF
		U10	9C00-9FFF
7:10	*5:12	U9	A000-A3FF
		U10	A400-A7FF
	6:11	U9	A800-ABFF
		U10	AC00-AFFF
8:9	*5:12	U9	B000-B3FF
		U10	B400-B7FF
	6:11	U9	B800-BBFF
		U10	BC00-BFFF
4:13	*5:12	U9	C000-C3FF
		U10	C400-C7FF
	6:11	U9	C800-CBFF
		U10	CC00-CFFF
6:11	*5:12	U9	D000-D3FF
		U10	D400-D7FF
	6:11	U9	D800-DBFF
		U10	DC00-DFFF
7:10	*5:12	U9	E000-E3FF
		U10	E400-E7FF
	6:11	U9	E800-EBFF
		U10	EC00-EFFF
8:9	*5.12	U9	F000-F3FF
		U10	F400-F7FF
	6:11	U9	F800-FBFF
		U10	FC00-FFFF

*Preprinted link connections.

plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.

- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S605 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The user may place the UART in one of two I/O groups by the position of a jumper wire on link LK1. If data bit DB0 is used as a group select, the group number $(0000\ 0001)_2$ is transmitted by the 61 output instruction to select the UART. The CDP18S605 comes with the link preprinted for group 1. The user also has the option of using data bit DB1 or group number $(0000\ 0010)_2$ for selecting the UART. When the UART is selected, the I/O instruc-

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Table IV - Additional Link Connections and Memory Addresses for ROM Type 2716

	LK6	ROM	Address
*1:16	*5:12	U9	0000-07FF
		U10	0800-0FFF
	6:11	U9	1000-17FF
		U10	1800-1FFF
	7:10	U9	2000-27FF
		U10	2800-2FFF
	8:9	U9	3000-37FF
		U10	3800-3FFF
2:15	*5:12	U9	4000-47FF
		U10	4800-4FFF
	6:11	U9	5000-57FF
		U10	5800-5FFF
	7:10	U9	6000-67FF
		U10	6800-6FFF
	8:9	U9	7000-77FF
		U10	7800-7FFF
3:14	*5:12	U9	8000-87FF
		U10	8800-8FFF
	6:11	U9	9000-97FF
		U10	9800-9FFF
	7:10	U9	A000-A7FF
		U10	A800-AFFF
	8:9	U9	B000-B7FF
		U10	B800-BFFF
4:13	*5:12	U9	C000-C7FF
		U10	C800-CFFF
	6:11	U9	D000-D7FF
		U10	D800-DFFF
	7:10	U9	E000-E7FF
		U10	E800-EFFF
	8:9	U9	F000-F7FF
		U10	F800-FFFF

*Preprinted link connections.

Table V - Baud Rate Selection Chart

Switch S1				Output Rate
4	3	2	1	Baud*
C	C	C	C	19200
C	C	O	C	50
C	C	O	O	75
C	O	C	C	134.5
C	O	C	O	200
C	O	O	C	600
C	O	O	O	2400
O	C	C	C	9600
O	C	C	O	4800
O	C	O	C	1800
O	C	O	O	1200
O	O	C	C	2400
O	O	C	O	300
O	O	O	C	150
O	O	O	O	110

*Actual input to UART is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.
O=Open; C=Closed.

tions 62, 63, 6A, and 6B are reserved for use in utility programs UT61 for operating the UART. When the CDP18S605 is used with Microboard Control and Display Module CDP18S640V1, which contains the utility program UT61, the UART must be linked for group 1, and the RAM and ROM on the CDP18S605 must be placed at a new location to avoid the UT61 and RAM on the CDP18S640V1.

Table VI - UART Linking Arrangements

UART Group Select
Group 1 (01_{16}): LK1 2:9 Closed; LK1 1:10 Open
Group 2 (02_{16}): LK1 2:9 Open; LK1 1:10 Closed

SDI to EF4-N
LK1 6:5 Closed

UART INT-N to CPU INT-N and EF3
LK1 3:8 Closed; LK1 4:7 Closed

Table VII - List of Links and Their Functions

LK1	
1:10	Select UART - Group 02_{16}
*2:9	Select UART - Group 01_{16}
3:8	UART Interrupt Line to CPU Interrupt
*4:7	UART Interrupt Line to EF3
*5:6	Serial Data-In Line to EF4
LK2	
*A:B	EIA Receiver Operation
LK3	
*1:14	ROM CDP1834/2758 Operation
2:13	ROM 2716 Operation
3:12	1.2288 MHz CPU Frequency
4:11	0.6144 MHz CPU Frequency
5:10	0.3072 MHz CPU Frequency
§6:9	4.9152 MHz CPU Frequency
*7:8	2.4576 MHz CPU Frequency
LK4	
*1:16	ROM Decoding
2:15	ROM Decoding
3:14	Permanent Connection
4:13	ROM Decoding
*5:12	ROM Decoding
6:11	ROM Decoding
7:10	RAM Decoding
*8:9	RAM Decoding

LK5		**LK6**	
1:16	RAM Decoding	1:16	ROM Decoding
2:15	RAM Decoding	2:15	ROM Decoding
*3:14	RAM Decoding	*3:14	ROM Decoding
4:13	RAM Decoding	4:13	ROM Decoding
*5:12	RAM Decoding	*5:12	ROM Decoding
6:11	RAM Decoding	6:11	ROM Decoding
7:10	RAM Decoding	7:10	ROM Decoding
8:9	RAM Decoding	8:9	ROM Decoding

LK7	
A:B	Inhibit ROM
LK8	
*1:12	RUN U
2:11	RUN U if installed in CDP18S005 or CDP18S007
3:10	Not Used
4:9	Not Used
*5:8	Clock Frequency Out
*6:7	+5 V to CDP1802 V_{DD}
LK9	
*A:B	$\overline{EF4}$ to Backplane
*C:D	+12 V/+15 V
LK11	
A:B	PWR-ON RESET
LK12	
*1:5	$\overline{CLEAR}$
*2:3	$\overline{WAIT}$
5:6	Not Used
2.4	Not Used

*Preprinted links.
§Not applicable to CDP18S605.

Power-On Reset

An RC integrator (R2 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U23) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU. The CPU initializes and starts processing at location 0000 provided the WAIT line is not asserted.

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 using transmission gates, three-state, or open-collector devices.

To enable the power-on reset, install a jumper in LK11, A:B.

Installation in the COSMAC Development Systems CDP18S005 (II) and CDP18S007 (III)

Replacement of the CDS CPU Module CDP18S102 or CDP18S102V1 with the RCA COSMAC Microboard Computer CDP18S605 requires some link changes on the CDP18S605. These changes are:

LK9—Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter), do not install A:D.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut link LK1 so that when it is re-installed, no conflict

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results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK8—RNU to start ROM's at address 8000. If there is ROM at 8000 containing a utility program, connect a wire jumper between 11 and 2 on link LK8 and cut link between 12 and 1 on link LK8. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after the RESET RUN U switches are pressed.

Memory Address Links—The desired memory addresses should be set up according to the memory maps of Tables I through IV. Care should be taken that the CDS memories are not assigned to overlap the assignment of the CDP18S605 Microboard Computer.

Power—Add a wire from location 12 pin 11 to location 14 pin 11 to provide -5 volts. This connection is needed only for the RS232C serial interface.

Table VIII - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

92CS-34444

Table IX - Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

Connector Matching Cable - Available Separately

CDP18S516 - EIA Terminal Interface Cable
Fits connector J2; 15 feet long; has 25-pin delta and mating male connectors for EIA RS232C Terminal.

CDP18S605

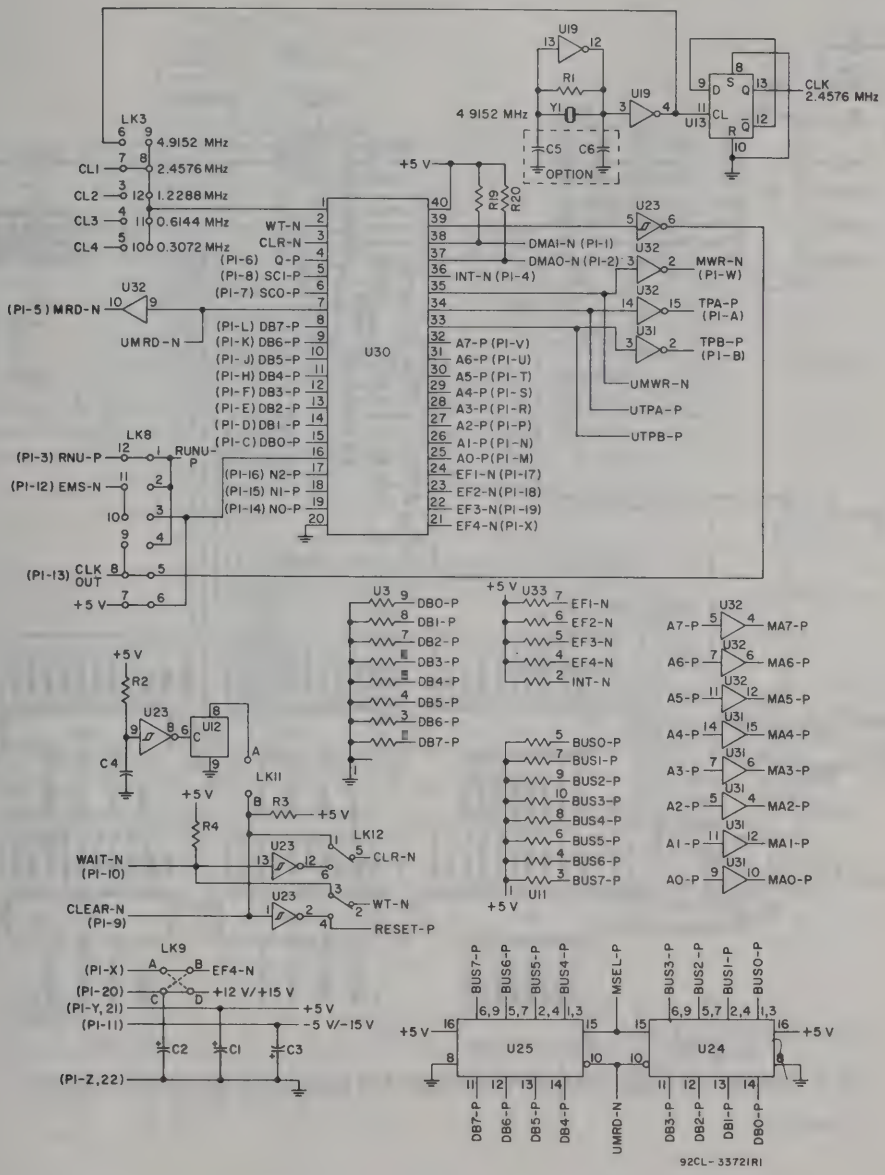


Fig. 2 - Microboard Computer CDP18S605 logic and circuit diagram - microprocessor and clock portion.

CDP18S605

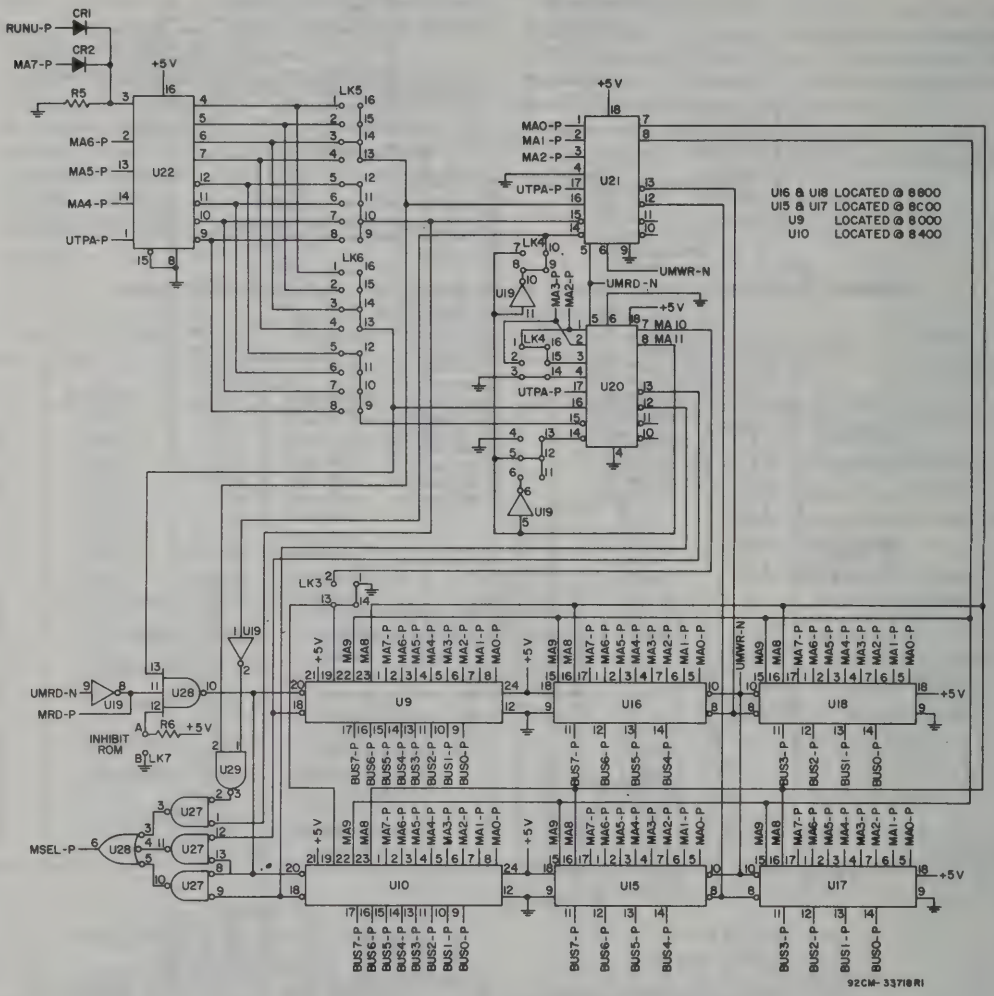


Fig. 3 - Microboard Computer CDP18S605 logic and circuit diagram - memory portion.

CDP18S605

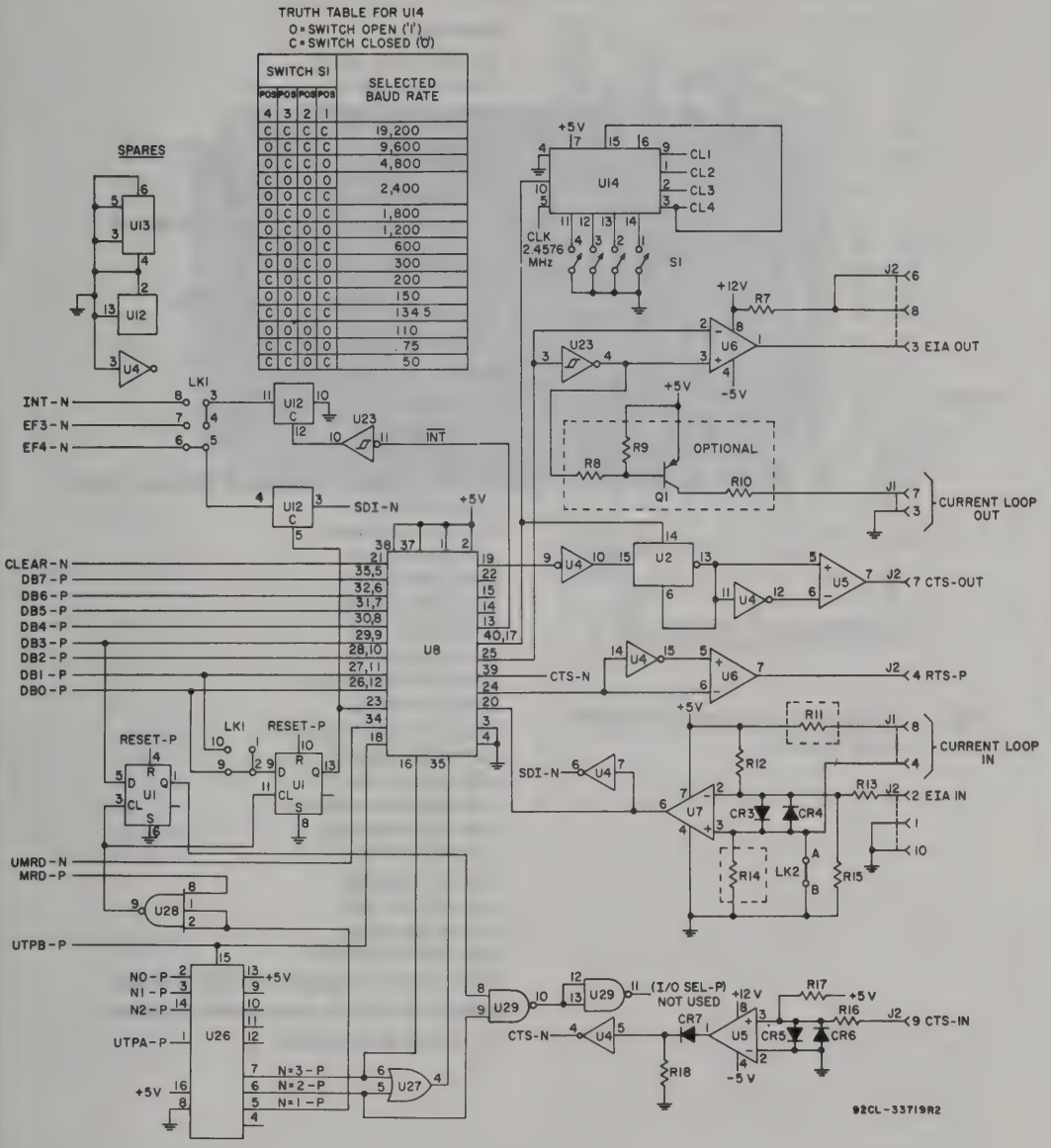


Fig. 4 - Microboard Computer CDP18S605 logic and circuit diagram - I/O portion.

CDP18S605

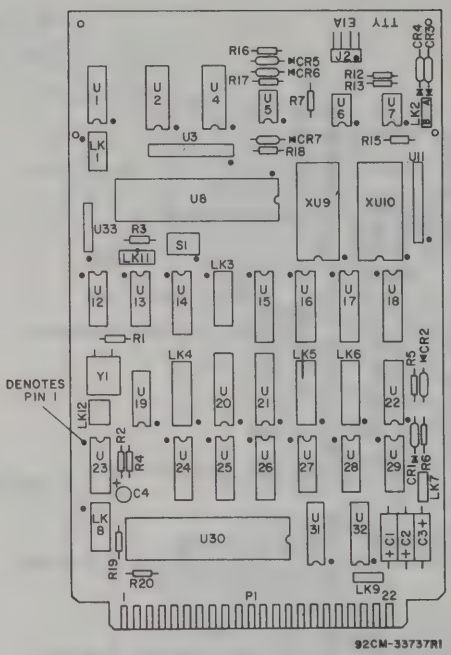
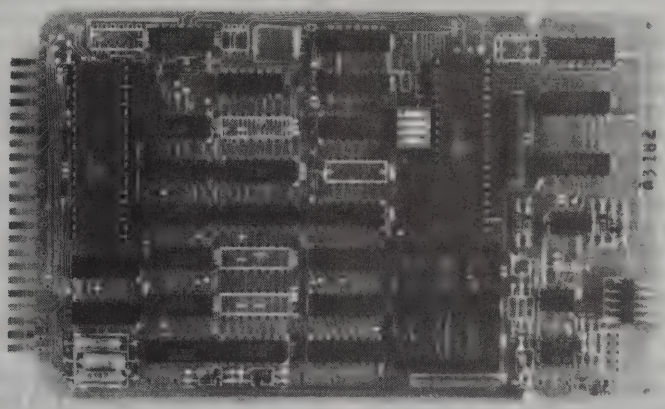


Fig. 5 - Microboard Computer CDP18S605 layout diagram.

Parts List

C1-C3'15 μF, 50 V
C4=1.5 μF, 25 V
CR1-CR7=1N270
J2=connector, right angle, 10 pin
R1=22 megohms, 0.25 W, 5%
R2=100 kilohms, 0.25 W, 5%
R3-R6,R19,R20=22 kilohms, 0.25 W, 5%
R7=3 kilohms, 0.25 W, 5%
R12=11 kilohms, 0.25 W, 5%
R13,R16=4.3 kilohms, 0.25 W, 5%
R15=1000 ohms, 0.25 W, 5%
R17=47 kilohms, 0.25 W, 5%
R18=10 kilohms, 0.25 W, 5%
S1=4-rocker DIP switch
U1=CD4013BE
U2=CD4017BE
U3,U11=resistor network, 22 kilohms, 10 pin
U4=CD4049UBE
U5,U6=CA3240AE
U7=CA3160AE
U8=CDP1854CE
U12=CD4066BE
U13=F34013PC
U14=F34702PC
U15-U18=MWS5114
U19=F34069PC
U20,U21=CDP1866CE
U22=CDP1858CE
U23=CD40106BE
U24,U25=CDP1856CE
U26=CDP1853CE
U27=CD4071BE
U28=CD4023BE
U29=CD4011BE
U30=CDP1802A
U31,U32=CD4050BE
U33=resistor network, 22 kilohms, 6 pin
XU9,XU10=24-pin, low-profile, IC socket
Y1=4.9152 MHz, crystal

CDP18S605



CDP18S606
RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP-18S606 is a versatile computer system on a single 4.5 x 7.5 inch card. The card contains a CDP1805 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on-reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S606 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and the special requirements of his specific application. The CDP18S606 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC CDOS Development System CDP18S007, facilitating prototype design and the debugging of both hardware and software.

Component Features

Central Processing Unit. The central processor for the CDP18S606 Microboard Computer is the 8-bit CMOS RCA COSMAC Microprocessor CDP1805. The CDP-1805 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1805 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Current required – 10 mA (typ.)†**
- **High noise immunity**
- **2-MHz crystal clock**
- **Compatible with COSMAC Development Systems**
- **Stand-alone capability**
- **4 kilobytes of read/write memory**
- **Sockets for 4/8 kilobytes of ROM/PROM**
- **Counter-timer**
- **Power-on reset**
- **COSMAC Microprocessor architecture with enhanced instruction set**
- **Flexible memory and I/O expansion**
- **20 programmable parallel I/O lines**
- **4 flag inputs**
- **Q serial data output**
- **RS232C or 20-mA serial I/O**
- **65,536-byte memory space**
- **44-pin system interface**
- **Temperature range: -40° C to +85° C**
- **Small board size — 4.5 x 7.5 inches**

† With CMOS ROM and RS232C serial interface.

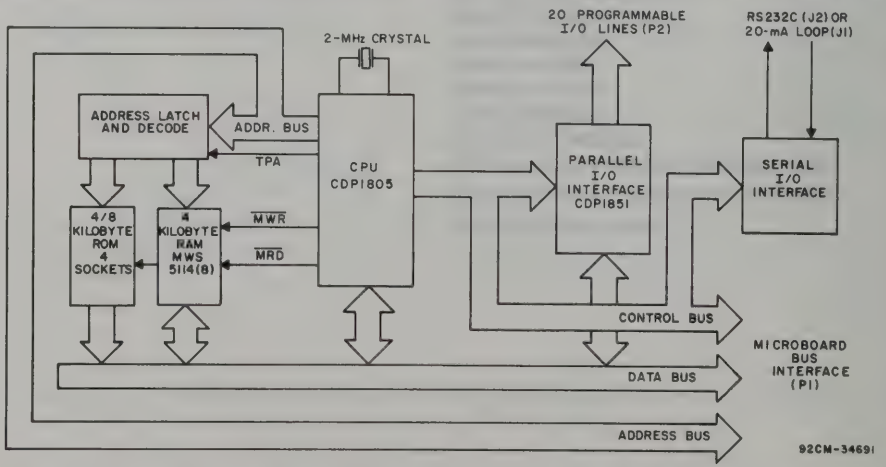


Fig. 1 — Block diagram of RCA COSMAC Microboard Computer CDP18S606.

branch conditions independently. The counter-timer feature is discussed below.

Memory. By means of eight MWS5114 RAMs, the CDP18S606 provides 4 kilobytes of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716-type EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S606 provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

Counter-Timer and Controls

The CDP1805 provides an on-chip 8-bit presettable timer-counter. Software control of the counter allows the clock input to be TPA ÷ 32, EF1, EF2, TPA•EF1, or TPA•EF2, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 2 consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

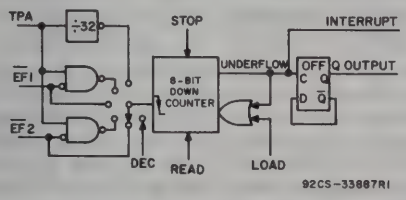


Fig. 2 — Timer/Counter diagram for CDP1805.

During a load instruction to the counter, the counter and its buffer register are loaded, and any previous interrupts cleared. If in an active state the counter must be stopped with a STPC instruction prior to issuing a LDC command. Read operations do not affect the counter.

The counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the EF1 terminal. The high-to-low transition decrements the counter.

2. Event Counter 2: Input to counter is connected to the EF2 terminal. The high-to-low transition decrements the counter.

3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC instruction.

4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

5. Pulse Duration Measurement 2: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF2}$ terminal is low. On the transition of $\overline{EF2}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) command clears the counter mode and stops counting.

In addition to the five programmable modes, the **Decrement Counter Instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the Event Counter mode, the instruction should be used only after the mode has been cleared by a Stop Counter Instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This action is independent of the Counter mode and the Interrupt Enable flip-flops.

CDP18S606

Application

The COSMAC Microboard Computer CDP18S606 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board. It may also be operated in conjunction with other Microboard Systems components installed in any location in the five-card Microboard Chassis (CDP18S675), in the 22-card Microboard Chassis (CDP18S670), or in any of the MSI Series of Industrial Chassis.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S606 Microboard computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC CDOS Development System CDP18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

Specifications

Memory Capacity
- On-board RAM: 4 kilobytes.
- On-board ROM/EPROM: 4 sockets for up to 8 kilobytes.
- Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map
- On-board RAM: Any even 4-kilobyte block.
- On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity
- Parallel: 20 lines each programmable as input, output, or bidirectional.
- Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.
- Counter: 8-bit timer-counter with 5 programmable modes.

Operating Temperature Range
- −40°C to +85°C

Dimensions
- 4.5 inches x 7.5 inches (114.3 x 190.5 mm)
- Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
- With CMOS ROM's and RS232C: +5 V at 10 to 30 mA, typical operating
- With CMOS ROM's and 20-mA loop: +5 V at 30 mA, typical operating
- Optional voltages used only for RS232C interface: +12 to +15 V at 8 mA, typical −5 to −15 V at 8 mA, typical

Connectors
- System Interface: Edge fingers, 44 pins on 0.156-inch centers.
- Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.
- Serial I/O: Two right-angle headers, 10 pin.

Clock
- CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard Computer CDP18S606 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1805 (File No. 1309). For a list of the pins and signals for the RCA COSMAC Universal Backplane Connector (P1) and used on the CDP18S606 Microboard Computer, see Table XI.

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S606 uses $\overline{EF1}$ and $\overline{EF2}$, conditioned by the secondary I/O address to test the READY state of I/O ports A and B. The serial data interface input is presented directly on $\overline{EF4}$ or $\overline{EF3}$ chosen by link LK36. I/O devices using the $\overline{INT}$ line may make use of the EF lines to identify the device. They may also be used to indicate priority or status.

$\overline{INT}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{INT}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

$\overline{DMAI}$, $\overline{DMAO}$ — Taken directly to the CPU pins and not utilized by the CDP18S606 these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S606 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{MWR}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{MRD}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. $\overline{MRD}$ must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while $\overline{MRD}$ is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless $\overline{MRD}$ is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. The CDP18S606 may use Q as a serial data output to the RS232C and 20-mA data terminal drivers. It is also available for other uses through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A 2-MHz square-wave clock provided for general use: It is derived from the crystal-controlled oscillator in the CPU.

$\overline{WAIT}$, $\overline{CLEAR}$ — Two control inputs to the CPU which determine the mode of operation.

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Not allowed
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

CDP18S606

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt. Power-up reset-run can be realized by connecting an RC network to $\overline{\text{CLEAR}}$.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 3).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 3). When run is initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle.

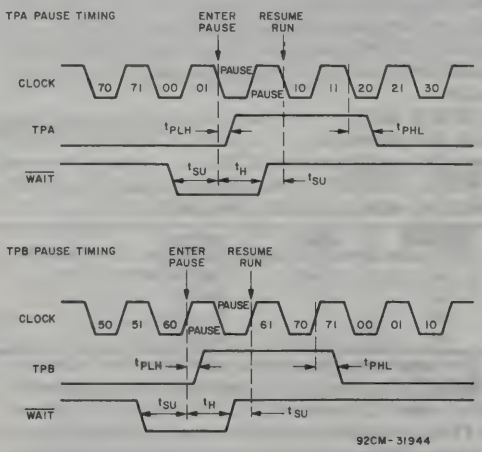


Fig. 3 — Pause mode timing waveforms.

The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S606 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The RAM on the CDP18S606 is 4 kilobytes of contiguous memory. The high-order four bits of the memory address is latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy any even 4-kilobyte block in the memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

Table I — 4-Kilobyte Link Connections

4-Kilobyte Address Space	Link LK10, LK11, or LK22 Pin Connections
0000-0FFF	1:16, 5:12
1000-1FFF	1:16, 6:11
2000-2FFF	1:16, 7:10
3000-3FFF	1:16, 8:9
4000-4FFF	2:15, 5:12
5000-5FFF	2:15, 6:11
6000-6FFF	2:15, 7:10
7000-7FFF	2:15, 8:9
8000-8FFF	3:14, 5:12
9000-9FFF	3:14, 6:11
A000-AFFF	3:14, 7:10
B000-BFFF	3:14, 8:9
C000-CFFF	4:13, 5:12
D000-DFFF	4:13, 6:11
E000-EFFF	4:13, 7:10
F000-FFFF	4:13, 8:9

LINK 11 is associated with the 4-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.

ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

Two types of links are provided and must be made up by the user to suit the particular ROM configuration selected. The first link type is for accommodating the type of ROM selected (CDP1834, 2708, 2758, or 2716). The second link type is for selecting the memory address space to be occupied by the ROM.

Link LK4 is an 18-pin dual-in-line arrangement with preprinted links to accommodate the 2716 ROM's. Table II gives the connections required for each ROM type.

Links LK10 and LK22 are 16-pin dual-in-line arrangements with no preprinted links. A DIP switch may be installed if frequent address changes are expected. Link LK10 provides the high-order four address bits decoded so that two links or jumpers place sockets XU24 and XU25 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK22 does the same for sockets XU26 and XU27. See Table I for address map and link connections.

To avoid having floating inputs to the gates, both links LK10 and LK22 should always have two jumpers. For example, if sockets XU26 and XU27 are unused, LK22 may be jumpered the same as LK10. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

In instances where no ROM sockets are used, it may be desirable to jumper links LK10, LK11, and LK12 identically so that the unused ROM space overlays the RAM space. In this way, no memory space is taken from the system's 64-kilobyte space for the unused ROM sockets.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK10 and LK22 should be jumpered identically in accordance with Table I. Then, the ROM's should be installed in sockets XU25, XU27, XU24, and XU26, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK10 and LK22 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then, socket XU25 is the low 2 kilobytes and socket XU24 is the high 2 kilobytes of the 4-kilobyte block as set in LK10. Similarly, socket XU27 is the low 2 kilobytes and socket XU26 is the high 2 kilobytes of the 4-kilobyte block set in LK22.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with two-kilobyte ROM's type 2716. If all links are set up for the 2-kilobyte ROM's as shown in Table II for LK4, and LK10 and LK22 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU25 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU24, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU24 or socket XU25 while the other socket is occupied by a 1-kilobyte ROM. Socket XU27 (low 2 kilobytes) and socket XU26 (high 2 kilobytes) may be used in the same manner.

Table II — ROM Type Selection Links

LINK LK4 Pins	ROM Type			
	CDP1834	2708	2758	2716*
1:18	X	OPEN	SHORTED	SHORTED
2:17	X	SHORTED	OPEN	OPEN
3:16	SHORTED	SHORTED	SHORTED	OPEN
4:15	OPEN	OPEN	OPEN	SHORTED
5:14	OPEN	OPEN	OPEN	SHORTED
6:13	SHORTED	SHORTED	SHORTED	OPEN
7:12	X	SHORTED	OPEN	OPEN
8:11	X	OPEN	OPEN	SHORTED
9:10	X	OPEN	SHORTED	OPEN

*X = don't care; Link LK4 is prewired to accept 2716.

I/O Operation

Serial I/O Interface. Serial data output is generated by the Q line from the CPU. Thus, software using the SET Q and RESET Q instructions generates data rate and format. Serial data input is presented to either EF3 or EF4, selectable by links as shown in Table III. The software uses the test branch instructions to decode incoming data.

Table III — Link Table for Serial Data In

Link LK36	Function
7:10	Data to EF3
8:9	Data to EF4

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2 respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire in the C5 holes. RS232C data terminals require that +12 volts be available on pin 20 of the backplane and -5 volts be available on pin 11.

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three

CDP18S606

bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S606 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The CDP18S606 uses bit three as the group select; that is, the group number $(08)_{16}$ or $(0000\ 1000)_2$ is transmitted by the 61 output instruction to select the programmable I/O on board.

In general, although Interrupt is not gated by group select, External Flags are gated by the appropriate group select. The serial interface on the CDP18S606, however, uses either EF3 or EF4 with no gating by group number. Therefore, when the serial interface is wired for use, EF3 or EF4, whichever was chosen, is not generally available for other devices.

Parallel I/O Interface. The parallel I/O interface consists of 20 lines provided on connector P2. These 20 lines are generated by the CDP1851 Programmable I/O Interface and may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides the Q line, EF1 through EF4, CLEAR, three different voltages, and a logic ground.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device.

The CDP1851 is assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data=08 is required before read, write, or control I/O may be performed.

Signal ARDY conditioned by the group select generates EF1; BRDY and group select generates EF2. Link LK41, pins A and B may be jumpered if interrupt-driven software is to be used. Then, INTA or INTB generates INT unconditionally.

Once the group select is accomplished, N1 and N2 are used to address the CDP1851. The following read and write instructions are used to access data, status, and command registers.

62 or 63 — Write to control register
64 or 65 — Write to Port A data register (if A is an output)
66 or 67 — Write to Port B data register (if B is an output)
6A or 6B— Read status register
6C or 6D— Read Port A data register (if A is an input)
6E or 6F — Read Port B data register (if B is an input)

Using the READY Lines for Data Synchronization. The Port A and Port B RDY lines are presented to the CPU EF1 and EF2 lines when the group select is set. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU. Note that there is a logic reversal: when RDY is true, the EF is false. Because of the logic reversal and because the event of interest is RDY going false, the EF true test is used. A test for ARDY might use the B1 instruction (34) which would take the branch if ARDY were false.

When a port designated as an **output** port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true), and load the next output byte. When a port is designated as an **input** port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and then reads the input byte. **In this case, a dummy read after reset is necessary to raise the first RDY.**

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the INTERRUPT Line for Data Synchronization. If link LK41, A:B is jumpered, INTA or INTB

generates INT to the CPU. INT is not conditioned by the group select. INT is set by the remote device sending STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table IV summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the group select 08, and then, either testing the RDY lines or reading the status byte. The low-order two bits of the status byte are: bit 0 = INTB; bit 1 = INTA.

Bidirectional Mode. Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, ARDY and ASTB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and BSTB becomes A OUTPUT STB. Each of the eight lines AD0-AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that output data is gated into AD0-AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode. Both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development Systems CDP18S005 (CDSII) or CDP18S007 (CDSIII)

Replacement of the CDS CPU Module CDP18S102 with the RCA COSMAC Microboard Computer CDP18S606 requires some link changes on the CDP18S606 and wiring changes on the CDS backplane. These changes are:

LK43 — Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D. See Table V.

Table IV — READY and INTERRUPT Actions for Input and Output Modes.

		Output Port	Input Port
READY	Set By Reset by	Loading Data STB leading edge	Reading Data STB leading edge
INTERRUPT	Set by Reset by	STB trailing edge Loading Data	STB trailing edge Reading Data

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Table V — Changes on Link LK43 for Installation of CDP18S606 in COSMAC Development System CDP18S005.

LK43	A:B	C:D	A:D	B:C
Microboard	*Closed	*Closed	Open	Open
CDS	Open	Open	Closed	Closed

*Preprinted links

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK36 — Serial Data In to external flag lines. In the CDS II, if the Terminal Interface Module CDP18S507 is not retained, connect pins 8:9 for EF4 to make the CDP18S606 the operator's terminal interface. If the CDP18S507 is retained, EF3 may be used for another serial interface purpose by connecting pins 7:10. In the CDS III, the UART module in location 14 is the operator's terminal interface and pins 7:10 and 8:9 may be left open.

LK36 — RNU to start ROM's at address 8000. Cut the wire jumper in pins 5:12. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed. This wire should be removed when the CPU Module CDP18S102 is reinstalled. See Table VI.

Table VI — Changes on Link LK36 for Installation of CDP18S606 in COSMAC Development System CDP18S005.

LK36	RNU 5:12	RNU 6:11	EF3 7:10	EF4 8:9
Microboard	*Closed	Open	Open	*Closed
CDS	Open	Closed	Open	Closed†

*Wire jumpers installed
†Assumes the CDP18S606 serial interface is to be the operator terminal interface.

LK10, LK11, and LK22 — Set up as previously described for the memory address desired, taking care that the CDS memories are not assigned to overlap the assignment of the CDP18S606 Microboard Computer.

Table VII summarizes the required CDS backplane wiring changes.

Table VII — Summary of Backplane Wiring Additions Needed When the CDP18S606 is Installed in the COSMAC Development System CDP18S005.

From		To		
Slot	Pin	Slot	Pin	Function
12	X	13	20	-12 V
12	11	14	11	-5 V
12	12	10	D	RNU-P†

†This connection should be removed when the CDP18S102 is reinstalled.

Table VIII — Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+ 5V
31	EF2-N	32	-5V/-15V
33	EF1-N	34	+12V/+15V

Table IX
Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

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Table X — List of Links and Their Functions

LK4	ROM Type Selection
*1:18	ROM Type 2758, 2716
2:17	ROM Type 2708
3:16	ROM Type 2758, 2708, or CDP1834
*4:15	ROM Type 2716
*5:14	ROM Type 2716
6:13	ROM Type 2758, 2708, or CDP1834
7:12	ROM Type 2708
*8:11	ROM Type 2716
9:10	ROM Type 2758

LK10	ROM Decoding for XU24 and XU25
*1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
*5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK11	RAM Decoding
1:16	$\overline{A15}$•$\overline{A14}$
*2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
*5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK22	ROM Decoding for XU26 and XU27
*1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
5:12	$\overline{A13}$•$\overline{A12}$
*6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK36	
*1:16	WAIT-N
*2:15	CLEAR-N
3:14	Not applicable to CDP1805
4:13	Not applicable to CDP1805
†5:12	RNU-P from P1-3
6:11	RNU-P from P1-12 (CDS installation only)
7:10	EF3 for serial interface in
†8:9	EF4 for serial interface in

LK37	
*A:B	+5 V V_{DD} to CDP1805

LK41	
A:B	Interrupt from PIO

LK43	
*A:B	Microboard system installation (EF4-N)
*C:D	Microboard system installation (+12 V)
A:D	CDS installation (+12 V)
B:C	CDS installation (EF4-N)

*Preprinted links
†Wire jumpers installed

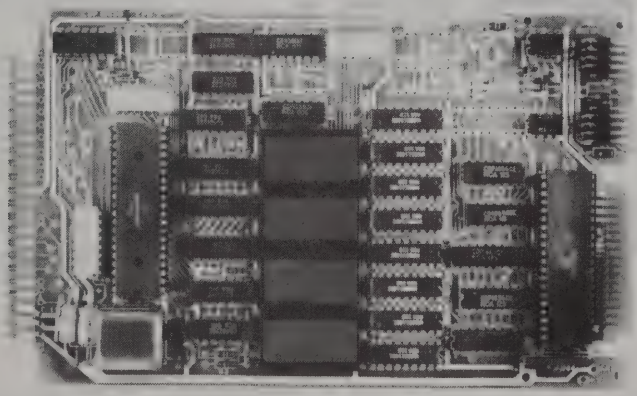

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Table XI — Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

92CS-34444

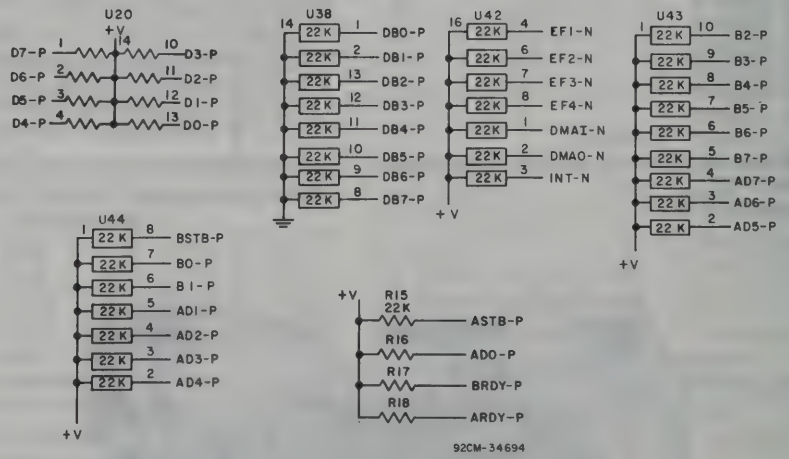

Fig. 4 — Pull-down and pull-up resistors.

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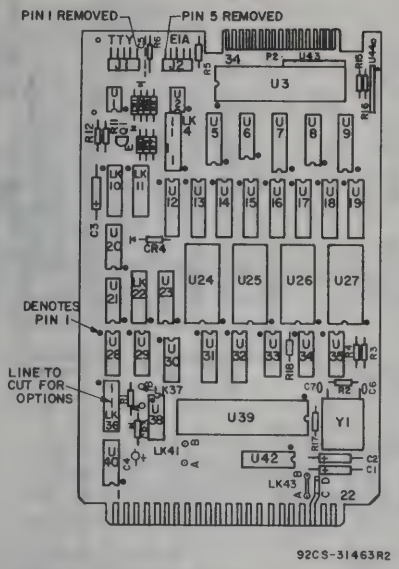

Fig. 5 — Layout diagram of RCA COSMAC Microboard Computer CDP18S606.

Parts List

C1, C2, C3 = 15 μF, 20 V
C4 = 1.5 μF, 35 V
C6=39 pF
C7=10 pF

CR1, CR2, CR3, CR4 = 1N270

J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP86016-1, keying plug — AMP 87077-1, or equivalent)

P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalents

Q1 = 2N5139

R1 = 100 kΩ, ¼ W, 5%
R2 = 22 MΩ, ¼ W, 5%
R3, R4 = 22 kΩ, ¼ W, 5%
R5 = 3 kΩ, ¼ W, 5%
R6, R14 = 1 kΩ, ¼ W, 5%
R7 = 11 kΩ, ¼ W, 5%
R8 = 4.3 kΩ, ¼ W, 5%
R9 = 130 kΩ, ¼ W, 5%
R10 = 10 kΩ, ¼ W, 5%
R11 = 2.7 kΩ, ¼ W, 5%
R12 = 100 Ω, ¼ W, 5%
R15-R18 = 22 kΩ, ¼ W, 5%

U1 = CA3160
U2 = CA3140
U3 = CDP1851CE
U5, U8 = CDP1856CE
U6 = CD4069BE
U7 = CDP1867CE
U9 = CDP1866CE
U12–U19 = MWS5114
U20, U38 = resistor module, 22 kΩ, 14 pin
U21 = CD4001BE
U23 = CDP1858CE
U28, U29 = CD4012BE
U30 = CD4016BE
U31, U32 = CD4050BE
U33 = CD4025BE
U34 = CD4013BE
U35 = CD4023UBE
U39 = CDP1805CE
U40 = CD4093BE
U42 = resistor module, 22 kΩ, 16 pin
U43 = resistor module SIP, 22 kΩ, 10-pin
U44 = resistor, module SIP, 8-pin

XU3, XU39 = 40-pin socket
XU24-XU27 = 24-pin socket

Y1 = 2.00-MHz crystal

CDP18S606

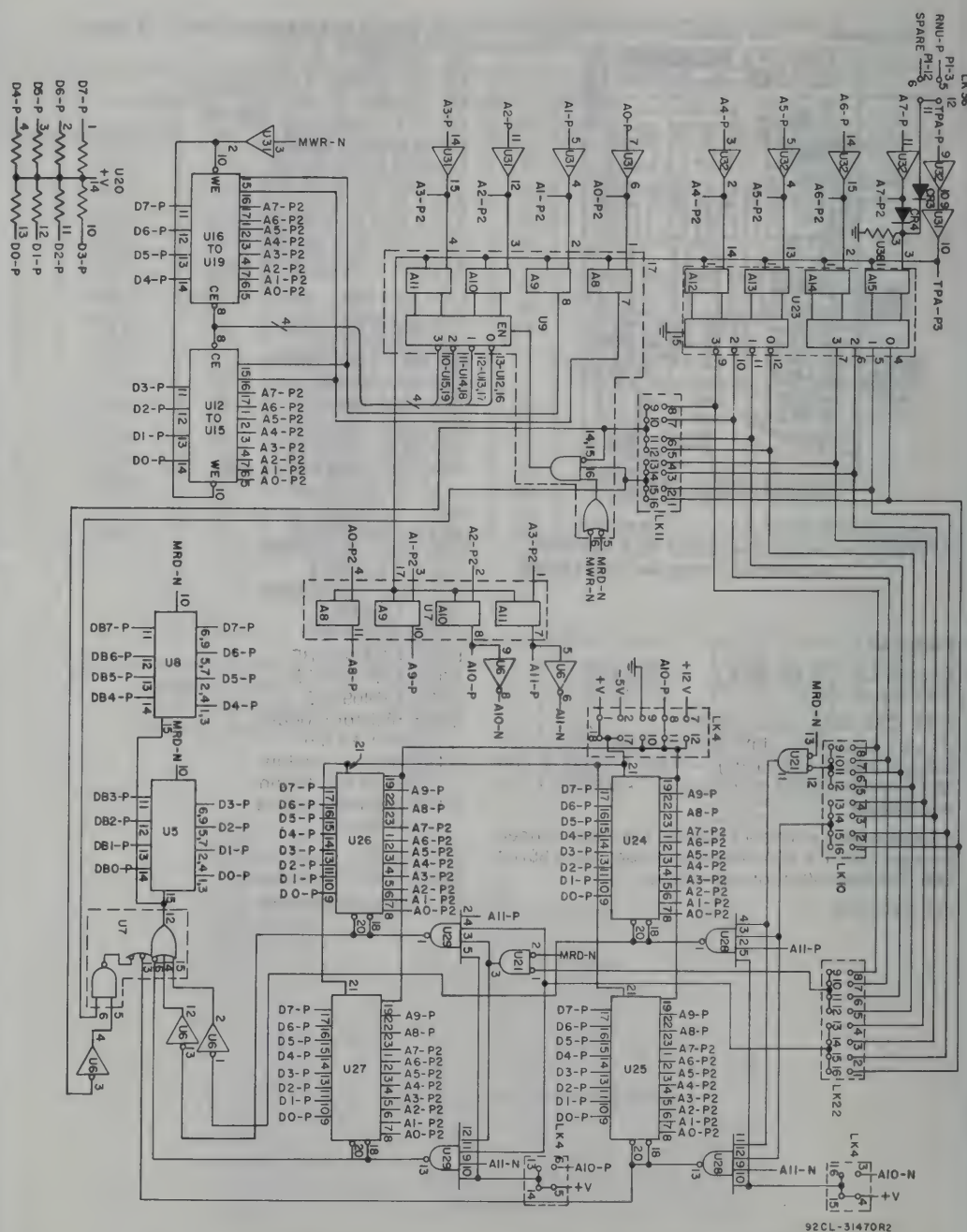

Fig. 6 — Logic diagram of Microboard Computer CDP18S606 — memory portions.

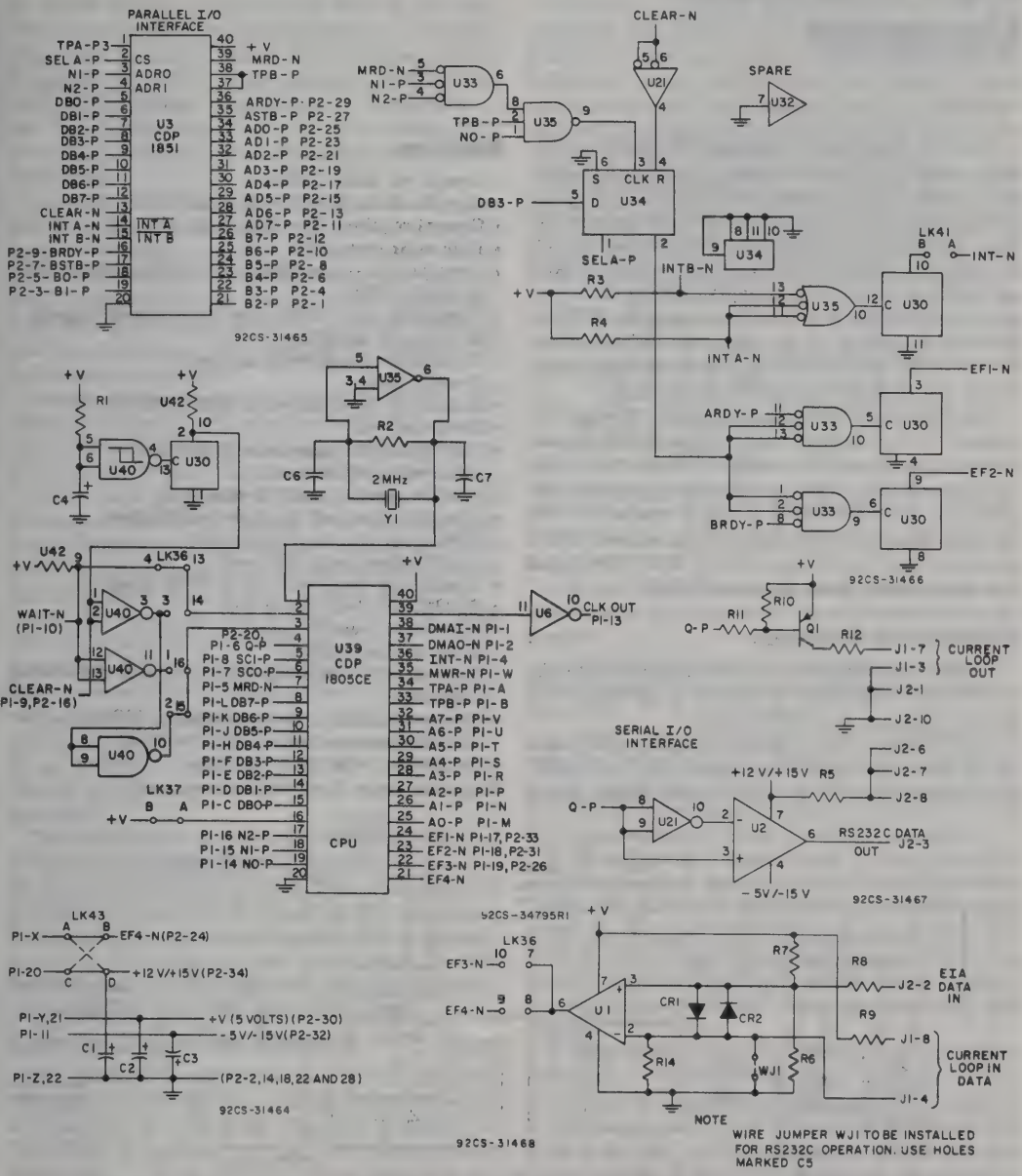

Fig. 7 — Logic diagram of Microboard Computer CDP18S606-CPU and interface portions.

CDP18S607
RCA Microboard Computer

The RCA Microboard Computer CDP18S607 is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card. The card contains a CDP1805CE CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a UART serial communications interface, power-on-reset, and expansion interface. Two on-board sockets are provided for read-only memory enabling the user to select 2 or 4 kilobytes of mask-programmable ROM or EPROM, depending on the application. Because of the CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S607 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and the special requirements of his specific applications. The CDP18S607 is plug-in compatible with the RCA MSI Series of Industrial Chassis. For detailed information on these Chassis, refer to **RCA Microboard Industrial Chassis Series Brochure,** MB-8.

Component Features

Central Processing Unit. The central processor for the CDP18S607 Microboard Computer is the RCA 8-bit CMOS Microprocessor CDP1805CE.

The CDP1805CE has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Current required: 8 to 28 mA (typ.)***
- **High noise immunity**
- **Crystal clock — selectable rates: 2.4576, 1.2288, 0.6144, or 0.3072 MHz**
- **Compatible with 1800-Series Development Systems**
- **Stand-alone capability**
- **2 kilobytes of read/write memory**
- **Counter-timer**
- **Sockets for 2/4 kilobytes of ROM/PROM**
- **Power-on reset**
- **1800-Series Microprocessor architecture with enhanced instruction set**
- **Flexible memory and I/O expansion**
- **8 parallel input and 8 parallel output lines**
- **4 flag inputs; Q serial data output**
- **UART-driven serial I/O port**
- **14 selectable baud rates: 50 to 19200 baud**
- **RS232C or 20-mA serial I/O**
- **65,536-byte memory space**
- **44-pin system interface**
- **Expandable by use of the RCA Microboard Universal Backplane**
- **Powered through either expansion or I/O connector**
- **Wide temperature range: -40°C to 85°C**
- **Small board size: 4.5 x 7.5 inches**

*Depending whether 20-mA serial interface is used.

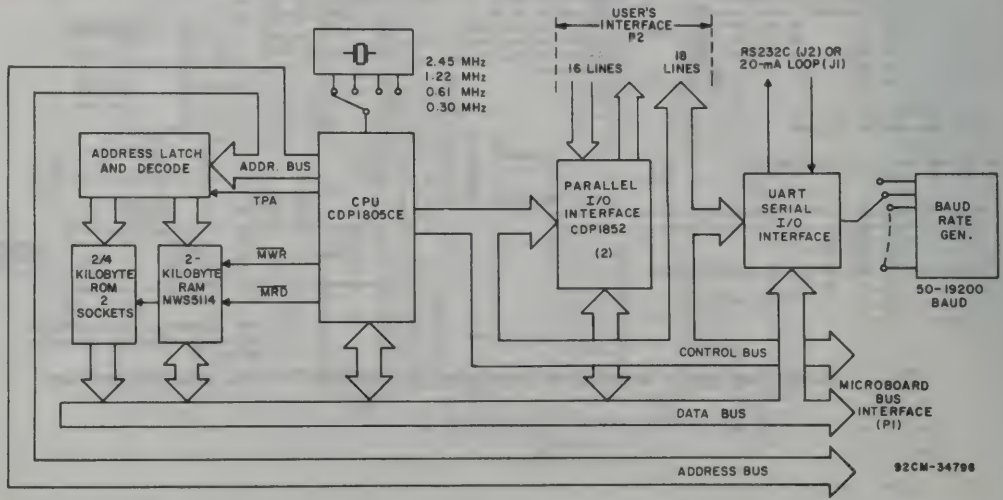

Fig. 1 — Block diagram of RCA Microboard Computer CDP18S607.

the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks and the like. One register each is designated for DMA and interrupt pointers. The CDP1805CE provides a serial data-out connection, Q, and four external flag input pins, EF1 through EF4, whose logic levels may be tested with conditional branch instructions.

The CDP1805CE features 113 instructions, 22 more than its predecessor CDP1802. These additional instructions include several powerful instructions such as call and return, 16-bit register operations, and interrupt controls. The on-chip counter-timer with its control instructions provides a versatile tool for a variety of timing and counting applications. The counter-timer feature is described more fully below.

Memory. By means of four MWS5114 RAM's, the CDP18S607 provides 2 kilobytes of CMOS read-write memory. In addition, two sockets are provided for two or four kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM or 2758 or 2716-type EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on boundaries in accordance with the memory maps given in Tables I through IV.

I/O. By means of two parallel I/O ports, type CDP1852, the CDP18S607 provides eight input and eight output lines. Each port has a handshaking line to indicate whether a byte has been written to or read from a port. A serial communications interface, having both a 20-milliampere loop and EIA RS232C capability, is driven by an on-board UART, the CDP1854A. Right-angle headers are provided for the serial communications interfaces.

The data format is determined by software. There are 14 baud rates available, from 50 to 19200 bauds, selectable by a four-rocker DIP switch. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. The user's edge connector provides, in addition to the two 8-line input and output ports, 18 other lines giving access to, among others, four flags, Q, interrupt, clock frequency, and three UART lines.

Counter-Timer and Controls

The CDP1805CE provides an on-chip 8-bit presettable timer-counter. Software control of the counter allows the clock input to be TPA ÷ 32, EF1, EF2, TPA•EF1, or TPA•EF2, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 2 consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a load instruction to the counter, the counter and its buffer register are loaded, and any previous interrupts cleared. If in an active state the counter must be stopped with a STPC instruction prior to issuing a LDC command. Read operations do not affect the counter.

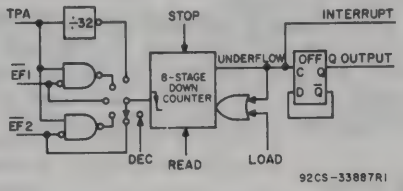

Fig. 2 — Timer/Counter diagram for CDP1805CE.

The counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the EF1 terminal. The high-to-low transition decrements the counter.

2. Event Counter 2: Input to counter is connected to the EF2 terminal. The high-to-low transition decrements the counter.

3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC instruction.

4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

5. Pulse Duration Measurement 2: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF2}$ terminal is low. On the transition of $\overline{EF2}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input

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is low, interrupt will also be set, but the counter will continue.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) command clears the counter mode and stops counting.

In addition to the five programmable modes, the **Decrement Counter Instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the Event Counter mode, the instruction should be used only after the mode has been cleared by a Stop Counter Instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This action is independent of the Counter mode and the Interrupt Enable flip-flops.

Application

The Microboard Computer CDP18S607 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or through the I/O connector. The CDP18S607 may be conveniently operated in conjunction with other Microboard Systems Components in the MSI Series of Industrial Chassis.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

When the CDP18S607 Microboard Computer is used with the Microboard Control and Display Module CDP18S640A1, some debugging capability is available even in such a two-card minimum system. By means of the control switches provided with the CDP18S640A1 (RESET, RUN PROGRAM, RUN UTILITY, AND STEP/CONT) and the six-digit hexadecimal display, the operator can observe the address and data sequences of both the fetch and execute cycles.

Specifications

Microprocessor
- CMOS 8-Bit CDP1805CE with
  - Call and return instructions
  - On-chip timer-counter
  - 16 registers each 16-bits wide
  - 16-bit register operations.

Memory Capacity
- On-board RAM: 2 kilobytes.
- On-board ROM/EPROM: 2 sockets for up to 4 kilobytes.
- Off-board Expansion: Any user-specified combination of RAM, ROM, and EPROM, up to a total of 65,536 bytes on-board and off-board.

Memory Address Map
(See Tables I through IV)
- On-board RAM: 2 kilobytes contiguous on any 2 kilobyte boundary: Links are preprinted for RAM at address 4000_{16}.
- On-board ROM and EPROM: For CDP1834 and 2758, 2 kilobytes contiguous on any 2-kilobyte boundary.
- For 2716, 4 kilobytes contiguous on any 4-kilobyte boundary. Links are preprinted for ROM types CDP1834 and 2758 and for address start at 0000.

I/O Capacity
- Parallel: 8 input lines and 8 output lines.
- Serial: UART-controlled input and output lines. Choice of 20-mA loop or EIA RS232C interface. User-programmed data format. 15 selectable baud rates, 50 to 19200 baud. CTS and RTS control lines.
- Counter: 8-bit timer-counter with 5 programmable modes.

Operating Temperature Range
- –40°C to 85°C

Dimensions
- 4.5 inches x 7.5 inches (114.3 x 190.5 mm)
- Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
- With CMOS ROM's and RS232C: +5 V at 32 mA, typical operating on-board RAM; 8 mA, off-board RAM.
- With CMOS ROM's and 20-mA loop: +5 V at 54 mA, typical operating on-board RAM; 30 mA off-board RAM.
- Optional voltages used only for RS232C interface:
  - +12 to +15 V at 8 mA, typical
  - –5 to –15 V at 8 mA, typical

Connectors
- System Interface: Edge fingers, 44 pins on 0.156-inch centers.
- Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pins.

Clock

CPU and Interface: crystal-controlled oscillator; selectable frequencies: 2.4576, 1.2288, 0.6144, and 0.3072 MHz. A preprinted link selects 2.4576 MHz as the CPU clock frequency.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the Microboard Computer CDP18S607. For additional information on these signals, refer to the published data for the CDP1805CE CMOS 8-Bit Microprocessor (File No. 1309).

These signals are summarized in Table XI which gives a list of the pins and the signals for the RCA Universal Backplane Connector (P1).

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The service request line from the input port can be jumped via LK1 to either EF3 or EF4 flag lines to indicate status. A preprinted link connects the input port's SR (Service Request) line to EF3 and the SDI (Serial Data In) line to EF4, conditioned by the proper select signal. The timer-counter may use EF1 or EF2 as input under software control.

$\overline{\text{INT}}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{\text{INT}}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter. The interrupt line from the UART can be presented directly to this input via link LK1.

$\overline{\text{DMAI}}$, $\overline{\text{DMAO}}$ — Taken directly to the CPU pins and not utilized by the CDP18S607, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S607 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

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$\overline{MRD}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions or by the counter output when enabled by the ETQ $(6809)_{16}$ instruction. It is also available for use through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A square-wave clock signal derived from an external crystal-controlled oscillator. One of four clock frequencies can be selected, 2.4576, 1.2288, 0.6144, or 0.3072 MHz. This signal is made available on connectors P1 and P2 by a preprinted link across pins 8 and 5 of link LK8. A preprinted link across pins 7 and 8 of link KL3 selects. 2.4576 MHz as the CPU clock frequency.

$\overline{WAIT}$, $\overline{CLEAR}$ — Two control inputs to the CPU which determine the mode of operation.

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Not Allowed
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

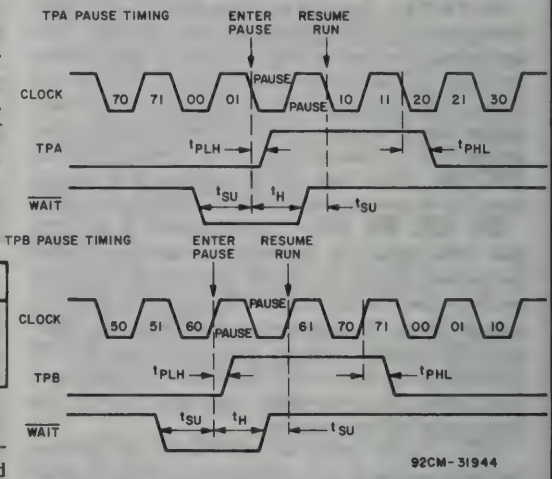
RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt. CDP18S607 provides an on-board RESET.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 3).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 3). When run is initiated from the



NOTE:
PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 3 — Pause mode timing waveforms.

Reset operation, the first machine cycle following Reset is always the initialization cycle.

The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S607 to force the most significant address bit true. As a result, the program start is at memory location 8000 instead of 0000. When the CDP18S607 is used in a stand-alone mode and a utility program is included at 8000, an RNU-P signal must be supplied to connector P1-3, and pins 12:1 must be connected on link LK8. When the CDP18S607 is used with Control and Display Module CDP18S640A1 RNU-P is provided.

Note: The board is supplied with a preprinted link — pins 12:1 on link LK8.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described in Tables I through IV. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The CDP18S607 Microboard Computer has two kilobytes of contiguous memory which can occupy any 2-kilobyte block in memory space on 2-kilobyte boundaries. The high-order byte of the memory address is latched and decoded. Bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two wire jumpers on link LK5. One jumper on link LK4 will enable the next level of decoding; selecting either A11 or A11 inverted enables the RAM decoder U21. If the

Table I - Memory Map and Link Connections for RAM

LK5		LK4	RAM	Address
1:16	*5:12	*7:10	U16/U18 U15/U17	0000-03FF 0400-07FF
		8:9	U16/U18 U15/U17	0800-0BFF 0C00-0FFF
	6:11	*7:10	U16/U18 U15/U17	1000-13FF 1400-17FF
		8:9	U16/U18 U15/U17	1800-1BFF 1C00-1FFF
	7:10	*7:10	U16/U18 U15/U17	2000-23FF 2400-27FF
		8:9	U16/U18 U15/U17	2800-2BFF 2C00-2FFF
	8:9	*7:10	U16/U18 U15/U17	3000-33FF 3400-37FF
		8:9	U16/U18 U15/U17	3800-3BFF 3C00-3FFF
*2:15	*5:12	*7:10	U16/U18 U15/U17	4000-43FF 4400-47FF
		8:9	U16/Y18 U15/U17	4800-4BFF 4C00-4FFF
	6:11	*7:10	U16/U18 U15/U17	5000-53FF 5400-57FF
		8:9	U16/U18 U15/U17	5800-5BFF 5C00-5FFF
	7:10	*7:10	U16/U18 U15/U17	6000-63FF 6400-67FF
		8:9	U16/U18 U15/U17	6800-6BFF 6C00-6FFF
	8:9	*7:10	U16/U18 U15/U17	7000-73FF 7400-77FF
		8:9	U16/U18 U15/U17	7800-7BFF 7C00-7FFF
3:14	*5:12	*7:10	U16/U18 U15/U17	8000-83FF 8400-87FF
		8:9	U16/U18 U15/U17	8800-8BFF 8C00-8FFF
	6:11	*7:10	U16/U18 U15/U17	9000-93FF 9400-97FF
		8:9	U16/U18 U15/U17	9800-9BFF 9C00-9FFF
	7:10	*7:10	U16/U18 U15/U17	A000-A3FF A400-A7FF
		8:9	U16/U18 U15/U17	A800-ABFF AC00-AFFF
	8:9	*7:10	U16/U18 U15/U17	B000-B3FF B400-B7FF
		8:9	U16/U18 U15/U17	B800-BBFF BC00-BFFF
4:13	*5:12	*7:10	U16/U18 U15/U17	C000-C3FF C400-C7FF
		8:9	U16/Y18 U15/U17	C800-CBFF CC00-CFFF
	6:11	*7:10	U16/U18 U15/U17	D000-D3FF D400-D7FF
		8:9	U16/U18 U15/U17	D800-DBFF DC00-DFFF
	7:10	*7:10	U16/U18 U15/U17	E000-E3FF E400-E7FF
		8:9	U16/U18 U15/U17	E800-EBFF EC00-EFFF
	8:9	*7:10	U16/U18 U15/U17	F000-F3FF F400-F7FF
		8:9	U16/U18 U15/U17	F800-FBFF FC00-FFFF

*Preprinted link connections.

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Table II - Connections for Link LK3 and LK4 for ROM

Link	CDP1834 or 2758	2716
LK4 1:16*	C	O
LK4 2:15	O	C
LK4 4:13	O	C
LK4 5:12*	X	O
LK4 6:11	X	O
LK3 1:14	O	C
LK3 2:13*	C	O

O = Open; C = Closed; *Preprinted link connections.
X = See Table III.

latched bit A11 is not inverted, the low half of a 4-kilobyte block is enabled. Bit A10 will next select 1-kilobyte segments within the 2-kilobyte block.

To set up the RAM address, it is necessary to install two jumpers in link LK5 and one in link LK4 as given in the memory map of Table 1. As an alternative, DIP switches may be installed if frequent link changes are anticipated.

To avoid having floating inputs to CMOS gates, links LK5 and LK4 must always have jumpers installed.

ROM Address. Two 24-pin sockets (XU9 and XU10) are provided for user-programmed ROM's. Three ROM types are suitable: CDP1834 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes). The address decoding technique prevents "wrap-around" in memory space for any

Table III — Additional Link Connections and Memory Addresses for ROM Types CDP1834 and 2758

LK6		LK4	ROM	Address
*1:16	*5:12	*5:12	U9	0000-03FF
			U10	0400-07FF
		6:11	U9	0800-0BFF
			U10	0C00-0FFF
	6:11	*5:12	U9	1000-13FF
			U10	1400-17FF
		6:11	U9	1800-1BFF
			U10	1C00-1FFF
	7:10	*5:12	U9	2000-23FF
			U10	2400-27FF
		6:11	U9	2800-2BFF
			U10	2C00-2FFF
	8:9	*5:12	U9	3000-33FF
			U10	3400-37FF
		6:11	U9	3800-3BFF
			U10	3C00-3FFF
2:15	*5:12	*5:12	U9	4000-43FF
			U10	4400-47FF
		6:11	U9	4800-4BFF
			U10	4C00-4FFF
	6:11	*5:12	U9	5000-53FF
			U10	5400-57FF
		6:11	U9	5800-5BFF
			U10	5C00-5FFF
	7:10	*5:12	U9	6000-63FF
			U10	6400-67FF
		6:11	U9	6800-6BFF
			U10	6C00-6FFF
	8:9	*5:12	U9	7000-73FF
			U10	7400-77FF
		6:11	U9	7800-7BFF
			U10	7C00-7FFF
3:14	*5:12	*5:12	U9	8000-83FF
			U10	8400-87FF
		6:11	U9	8800-8BFF
			U10	8C00-8FFF
	6:11	*5:12	U9	9000-93FF
			U10	9400-97FF
		6:11	U9	9800-9BFF
			U10	9C00-9FFF
	7:10	*5:12	U9	A000-A3FF
			U10	A400-A7FF
		6:11	U9	A800-ABFF
			U10	AC00-AFFF
	8:9	*5:12	U9	B000-B3FF
			U10	B400-B7FF
		6:11	U9	B800-BBFF
			U10	BC00-BFFF
4:13	*5:12	*5:12	U9	C000-C3FF
			U10	C400-C7FF
		6:11	U9	C800-CBFF
			U10	CC00-CFFF
	6:11	*5:12	U9	D000-D3FF
			U10	D400-D7FF
		6:11	U9	D800-DBFF
			U10	DC00-DFFF
	7:10	*5:12	U9	E000-E3FF
			U10	E400-E7FF
		6:11	U9	E800-EBFF
			U10	EC00-EFFF
	8:9	*5:12	U9	F000-F3FF
			U10	F400-F7FF
		6:11	U9	F800-FBFF
			U10	FC00-FFFF

*Preprinted link connections.

Table IV - Additional Link Connections and Memory Addresses for ROM Type 2716

LK6		ROM	Address
*1:16	*5:12	U9	0000-07FF
		U10	0800-0FFF
	6:11	U9	1000-17FF
		U10	1800-1FFF
	7:10	U9	2000-27FF
		U10	2800-2FFF
	8:9	U9	3000-37FF
		U10	3800-3FFF
2:15	*5:12	U9	4000-47FF
		U10	4800-4FFF
	6:11	U9	5000-57FF
		U10	5800-5FFF
	7:10	U9	6000-67FF
		U10	6800-6FFF
	8:9	U9	7000-77FF
		U10	7800-7FFF
3:14	*5:12	U9	8000-87FF
		U10	8800-8FFF
	6:11	U9	9000-97FF
		U10	9800-9FFF
	7:10	U9	A000-A7FF
		U10	A800-AFFF
	8:9	U9	B000-B7FF
		U10	B800-BFFF
4:13	*5:12	U9	C000-C7FF
		U10	C800-CFFF
	6:11	U9	D000-D7FF
		U10	D800-DFFF
	7:10	U9	E000-E7FF
		U10	E800-EFFF
	8:9	U9	F000-F7FF
		U10	F800-FFFF

*Preprinted link connections.

memory type.

Table II shows the LK3 and LK4 link connections needed for the ROM selected. Tables III and IV give the additional link connections needed and the memory address information.

For testing or debugging, all ROM space can be inhibited by connecting A and B on link LK7.

When ROM's CDP1834 or 2758 are used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. One jumper on link LK4 enables the next level of decoding; selecting either A11 or A11 inverted enables ROM decoder U20.

If bit A11 is not inverted, the low half of the 2-kilobyte block is selected. If bit A11 is inverted by U19, the high half of the block is enabled. Another jumper on link LK4 connects bit A10 to the decoder selecting one of the two 1-kilobyte blocks. For the CDP1834 and 2758, input pin 19 of the ROM is grounded. Note that to avoid floating inputs, links LK6 and LK4 must have jumpers installed.

When ROM 2716 is used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. With another jumper connecting pins 2:15 on link LK4, bit A11 now selects 2-kilobyte segments within a 4-kilobyte block. Link LK3 is used to connect address bit A10 to pin 19 of the 2716 ROM.

Note that with type 2716 also, jumpers must always be present to avoid floating inputs to CMOS gates. Note that the CDP18S607 is initially configured for ROM types CDP1834 and 2758 at address 0000.

Input/Output Interfacing

Serial I/O Interfacing. Serial output data is generated by the UART. In Microboard systems including the Control and Display Module CDP18S640A1, the utility software UT61 sets the data format. This format is one start bit, eight data bits (no parity), and two stop bits. The utility also determines when to read data from the UART and when to write to it by reading its status word. The user, of course, has the option in a stand-alone system of writing his own UART routine.

The UART interrupt line is wired to link LK1 where the user may jumper it either to the CPU's interrupt input or to one of two flag lines (EF3 or EF4).

Three signals from the UART are available on the user connector P2. These signals, DA (data available), RTS (request to send), and CTS (clear to send), are useful for handshaking with modems. See the data sheet for UART CDP1854A (File No. 1193).

Because the SDI line is connected to EF4 by means of a preprinted link, a break condition may be conveniently detected.

Any one of the 14 baud rates available from the baud rate generator can be selected through a four-bit binary code determined by the setting of a four-rocker DIP switch. The switch settings are given in Table V.

Electrical interfaces for either the 20-mA loop or

CDP18S607

RS232C data terminals are provided on connectors J1 and J2 respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire between pins A and B on link LK2, and supplying +12 V and -5 V power.

Two-Level I/O Interfacing. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard System the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function. Any I/O function is assigned to a group number and only responds when its group number and its appropriate N register code are transmitted.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S607 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

Table V - Baud Rate Selection Chart

Switch S1				Output Rate
4	3	2	1	Baud*
C	C	C	C	19200
C	C	O	C	50
C	C	O	O	75
C	O	C	C	134.5
C	O	C	O	200
C	O	O	C	600
C	O	O	O	2400
O	C	C	C	9600
O	C	C	O	4800
O	C	O	C	1800
O	C	O	O	1200
O	O	C	C	2400
O	O	C	O	300
O	O	O	C	150
O	O	O	O	110

*Actual input to UART is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.
O = Open; C = Closed

Table VI - UART Linking Arrangements

UART Group Select
Group 1 (01_{16}): LK1 2:9 Closed; LK1 1:10 Open Group 2 (02_{16}): LK1 2:9 Open; LK1 1:10 Closed
SDI to EF4-N
LK1 6:5 Closed; LK10 2:3 Closed; LK10 1:4 Open
UART DA-N to EF4-N
LK1 6:5 Closed; LK10 2:3 Open; LK10 1:4 Closed
UART INT-N to CPU INT-N
LK1 3:8 Closed

The user may place the UART in one of two I/O groups by the position of a jumper wire on link LK1. If data bit DB0 is used as a group select, the group number $(0000\ 0001)_2$ is transmitted by the 61 output instruction to select the UART. The CDP18S607 comes with the link preprinted for group 1.The user also has the option of using data bit DB1 or group number $(0000\ 0010)_2$ for selecting the UART. When the UART is selected, the I/O instructions 62, 63, 6A, and 6B are reserved for use in the utility programs UT61 for operating the UART. When the CDP18S607 is used with Microboard Control and Display Module CDP18S640V1, which contains the utility program UT61, the UART must be linked for group 1.

Other settings of links LK1 and LK10, as shown in Table VI, make it possible to monitor UART signals by connecting them to flag and interrupt lines.

Parallel I/O Interfacing. The parallel I/O interface consists of 20 lines provided on connector P2. Two CDP1852's provide one input and one output port. The input port sets a service request line (SR) when data is strobed into it. SR is initially linked to EF3. The output port provides a data available signal (DA) when a byte is

written into it. For details, see the data sheet for the CDP1852 (File No. 1166).

The two ports are assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data $=08_{16}$ is required before read or write may be performed. Then I/O instructions 62 and 6A select the output or input port, respectively.

Power-On Reset

An RC integrator (R2 and C4 in the logic diagram of Fig. 5) and a Schmitt-trigger circuit (U23) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, UART, and the I/O group-select latches. After the CLEAR signal, the I/O group selects are reset, the output port and its DA are reset, and the input port goes to a high-impedance state with SR reset. The CPU initializes and starts processing at location 0000 provided the WAIT line is not asserted.

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the RCA Development Systems CDP18S005 (II) and CDP18S007 (III)

Replacement of the CDS CPU Module CDP18S102 or CDP18S102V1 with the RCA Microboard Computer CDP18S607 requires some link changes on the CDP18S607. These changes are:

LK9 — Cut A:B and C:D and install A:D and B:C. If

Table VII - List of Links and Their Functions

LK1	
1:10	Select UART - Group 02_{16}
*2:9	Select UART - Group 01_{16}
3:8	UART Interrupt Line to CPU Interrupt
*4:7	Input Port Service Request to EF3
*5:6	Serial Data-In Line to EF4
LK2	
A:B	EIA Receiver Operation
LK3	
1:14	ROM 2716 Operation
*2:13	ROM CDP1834/2758 Operation
3:12	1.2288 MHz CPU Frequency
4:11	0.6144 MHz CPU Frequency
5:10	0.3072 MHz CPU Frequency
§6:9	4.9152 MHz CPU Frequency
*7:8	2.4576 MHz CPU Frequency
LK4	
*1:16	ROM Decoding
2:15	ROM Decoding
3:14	Permanent Connection
4:13	ROM Decoding
*5:12	ROM Decoding
6:11	ROM Decoding
*7:10	RAM Decoding
8:9	RAM Decoding

*Preprinted links.
§Not applicable to CDP18S607.

LK5		**LK6**	
1:16	RAM Decoding	*1:16	ROM Decoding
*2:15	RAM Decoding	2:15	ROM Decoding
3:14	RAM Decoding	3:14	ROM Decoding
4:13	RAM Decoding	4:13	ROM Decoding
*5:12	RAM Decoding	*5:12	ROM Decoding
6:11	RAM Decoding	6:11	ROM Decoding
7:10	RAM Decoding	7:10	ROM Decoding
8:9	RAM Decoding	8:9	ROM Decoding

LK7	
A:B	Inhibit ROM
LK8	
*1:12	RUN U
2:11	RUN U If Installed in CDP18S005 or CDP18S007
3:10	Not Used
4:9	Not Used
*5:8	Clock Frequency Out
*6:7	+5 V
LK9	
*A:B	$\overline{EF4}$ to Backplane
*C:D	+12 V/+15 V
LK10	
1:4	UART DA Line to $\overline{EF4}$
*2:3	Serial Data In to $\overline{EF4}$
LK11	
*1:5	$\overline{CLEAR}$
*2:3	$\overline{WAIT}$
5:6	Not Used
2:4	Not Used

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+12-volt supply is not needed (it is required only for the RS232C data terminal transmitter), do not install A:D.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK8 — RNU to start ROM's at address 8000. If there is ROM at 8000 containing a utility program, connect a wire jumper between 11 and 2 on link LK8 and cut link between 12 and 1 on link LK8. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after the RESET RUN U switches are pressed.

Power — On the CDS backplane, add a wire from location 12 pin 11 to location 14 pin 11 to provide -5 volts. This connection is needed only for the RS232C serial interface, if required.

Memory Address Links. The desired memory addresses should be set up according to the memory maps of Tables I through IV. Care should be taken that the CDS memories are not assigned to overlap the assignment of the CDP18S607 Microboard Computer.

Connector Matching Cables — Available Separately

CDP18S515 — TTY Terminal Interface Cable
Fits connector J1; 15 feet long; has Molex connector for 20-mA TTY terminal.

CDP18S516 - EIA Terminal Interface Cable
Fits connector J2; 15 feet long; has 25-pin delta and mating male connectors for EIA RS232C Terminal.

CDP18S517 - I/O Interface Cable
Fits connector P2; 36 inches long; 34-pin flat ribbon cable; output end unterminated.

Table VIII
Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	DI2-P	2	GND
3	DI1-P	4	DI3-P
5	DI0-P	6	DI4-P
7	STROBE P	8	DI5-P
9	CLOCK OUT	10	DI6-P
11	DO7-P	12	DI7-P
13	DO6-P	14	CTS-N
15	DO5-P	16	CLEAR-N
17	DO4-P	18	GND
19	DO3-P	20	Q-P
21	DO2-P	22	DA-N
23	DO1-P	24	EF4-N
25	DO0-P	26	EF3-N
27	INT-N	28	RTS-N
29	DA-P	30	+5 V
31	EF2-N	32	−5 V/−15 V
33	EF1-N	34	+12 V/+15 V

Table IX
Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Table X
Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

Table XI - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

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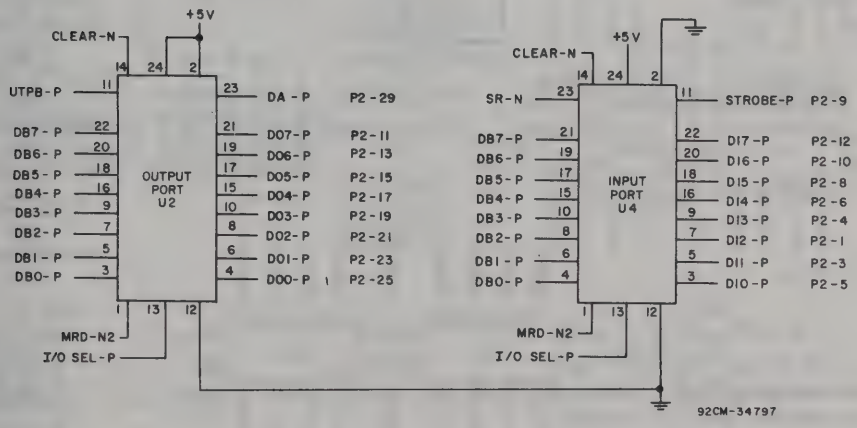


Fig. 4 — Logic Diagram of Microboard Computer CDP18S607 — Parallel I/O Interface Portion.

CDP18S607

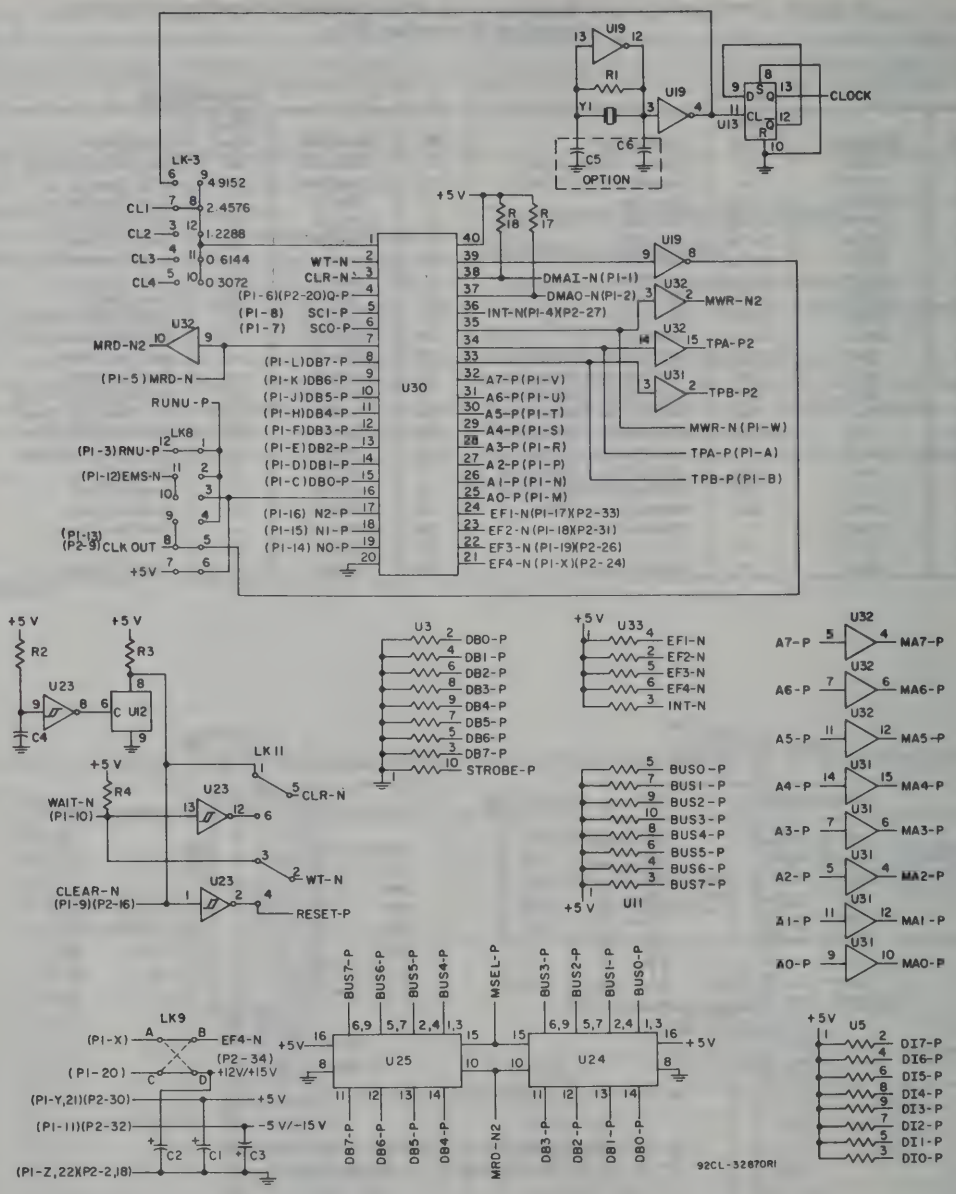


Fig. 5 — Logic diagram of Microboard Computer CDP18S607 — CPU, Oscillator, and Buffer Portion.

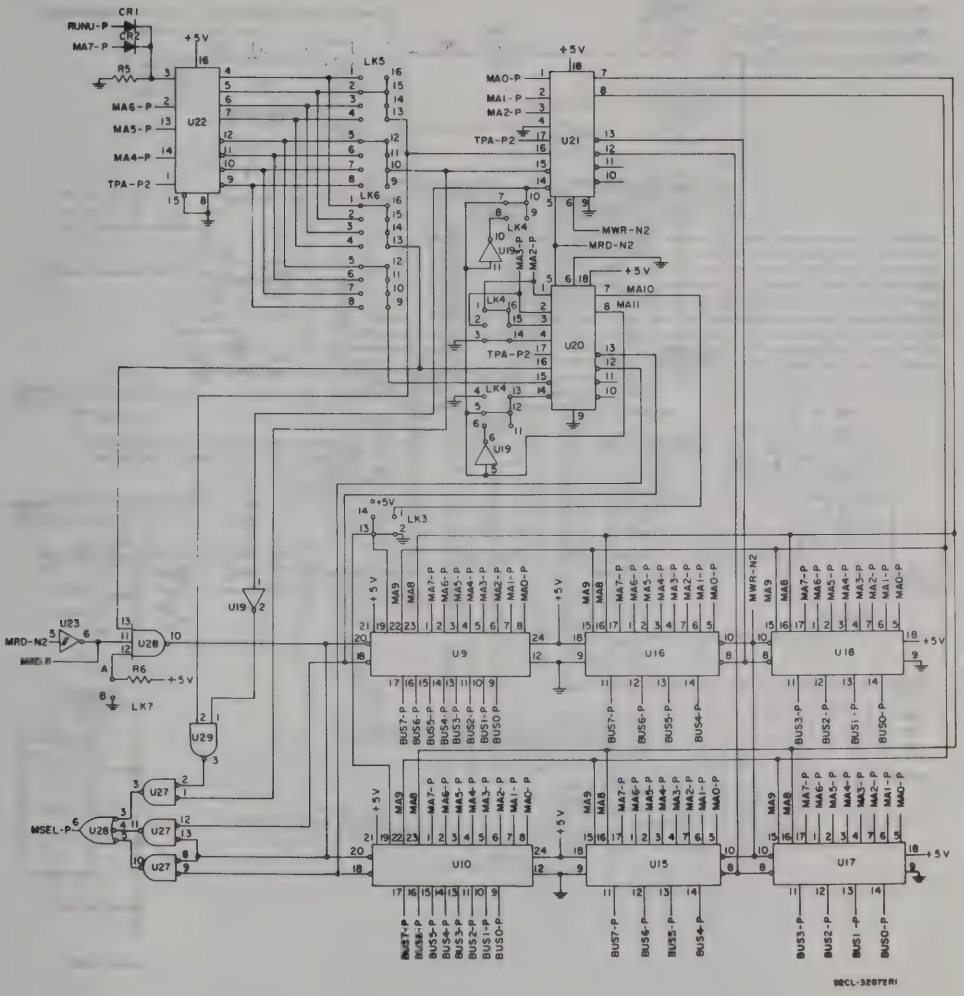


Fig. 6 — Logic diagram of Microboard Computer CDP18S607 — Memory Portion.

CDP18S607

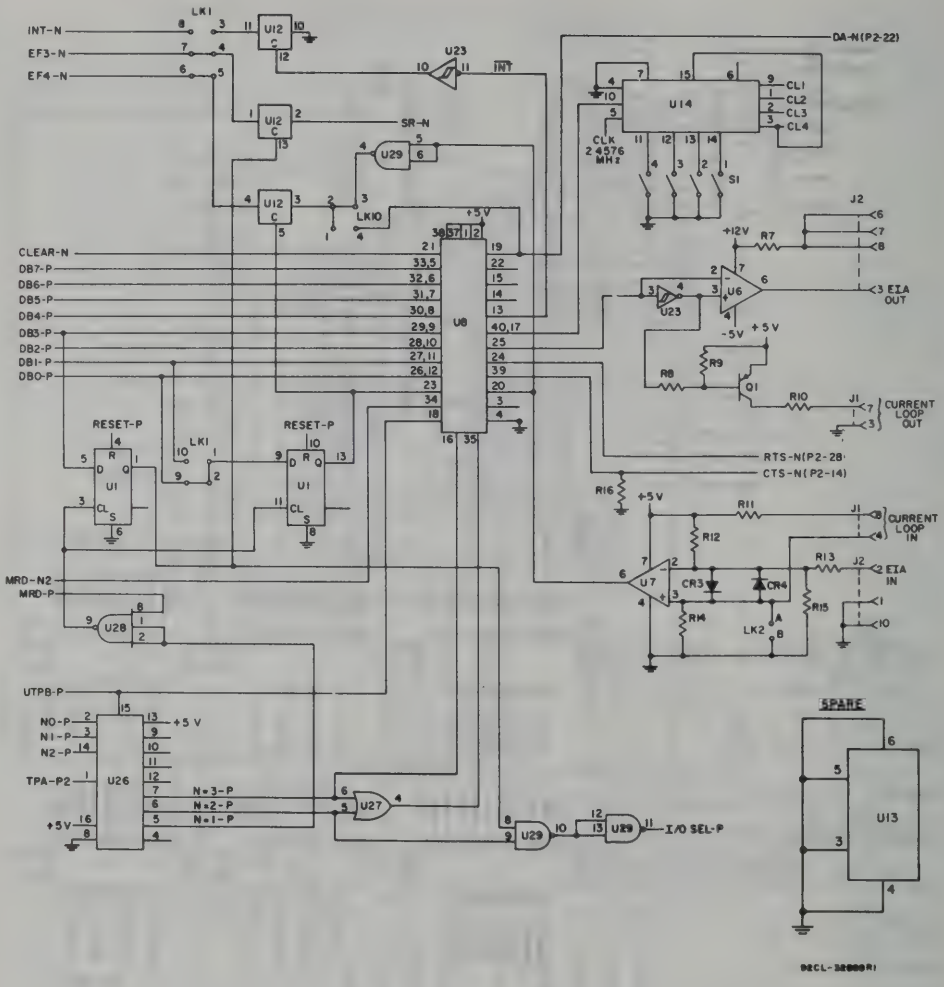


Fig. 7 — Logic Diagram of Microboard Computer CDP18S607 — UART Serial I/O Interface Portion.

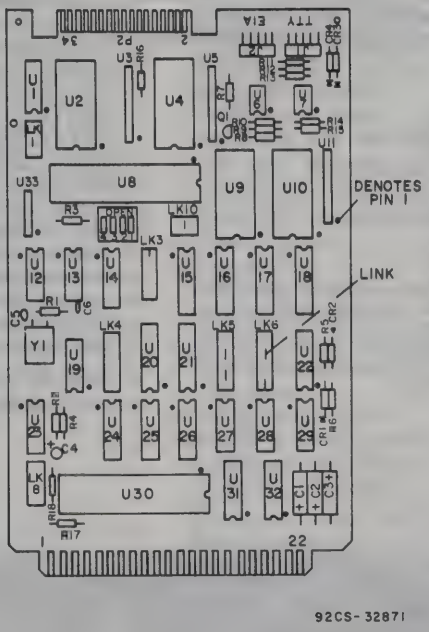


Fig. 8 — Layout Diagram of Microboard Computer CDP18S607.

CDP18S607

Parts List

C1, C2, C3 = 15 μF, 20 V
C4 = 1.5 μF, 25 V

CR1, CR2, CR3, CR4 = 1N270
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP86016-1, keying plug — AMP 87077-1, or equivalent)

Q1 = 2N5139

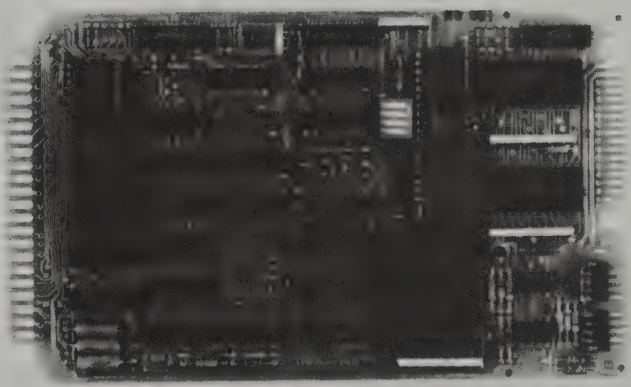
R1 = 22 MΩ, ¼ W, 10%
R2 = 100 kΩ, ¼ W, 5%
R3-R6, R16-R18 = 22 kΩ, ¼ W, 5%
R7 = 3 kΩ, ¼ W, 5%
R8 = 2.7 kΩ, ¼ W, 5%
R9 = 10 kΩ, ¼ W, 5%
R10 = 100 Ω, ¼ W, 5%
R11 = 130 Ω, ¼ W, 5%
R12 = 11 kΩ, ¼ W, 5%
R13 = 4.3 kΩ, ¼ W, 5%
R14, R15 = 1 kΩ, ¼ W, 5%

S1 = 4-rocker DIP switch

U1 = CD4013BE
U2, U4 = CDP1852CE
U3, U5, U11 = resistor module, 22 kΩ, 10 pin
U6 = CA3140AE
U7 = CA3160AE
U8 = CDP1854ACE
U12 = CD4066BE
U13 = 4013 Fairchild
U14 = 4702 Fairchild
U15-U18 = MWS5114E
U19 = 4069 Fairchild
U20, U21 = CDP1866CE
U22 = CDP1858CE
U23 = CD40106BE
U24, U25 = CDP1856CE
U26 = CDP1853CE
U27 = CD4071BE
U28 = CD4023BE
U29 = CD4011BE
U30 = CDP1805CE
U31, U32 = CD4050BE
U33 = resistor module, 22 kΩ, 6 pin

XU9, XU10 = 24-pin socket

Y1 = 4.9152-MHz crystal



CDP18S608

RCA Microboard Computer

The RCA Microboard Computer CDP18S608 is a versatile computer system on a single 4.5 x 7.5 inch card. The card contains a CDP1805CE CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 to 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S608 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and special requirements of his specific application. The CDP18S608 is plug-in compatible with the RCA MSI Industrial Chassis Series. For more detailed information on these Chassis, refer to **RCA Microboard Industrial Chassis Series Brochure,** MB-8.

Component Features

Central Processing Unit. The central processor for the CDP18S608 Microboard Computer is the 8-bit CMOS RCA Microprocessor CDP1805CE. The CDP1805CE has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Current required — 7 to 27 mA (typ.)†**
- **High noise immunity**
- **2-MHz crystal clock**
- **Compatible with 1800-Series Development Systems**
- **Stand-alone capability**
- **1 kilobyte of read/write memory**
- **Sockets for 4/8 kilobytes of ROM/PROM**
- **Power-on reset**
- **Counter-timer**
- **1800-Series Microprocessor architecture with enhanced instruction set**
- **Flexible memory and I/O expansion**
- **20 programmable parallel I/O lines**
- **4 flag inputs**
- **Q serial data output**
- **RS232C or 20-mA serial I/O**
- **65,536-byte memory space**
- **44-pin system interface**
- **Temperature range: -40° C to +85° C**
- **Small board size: 4.5 x 7.5 inches**

†Depending whether 20-mA serial interface is used.

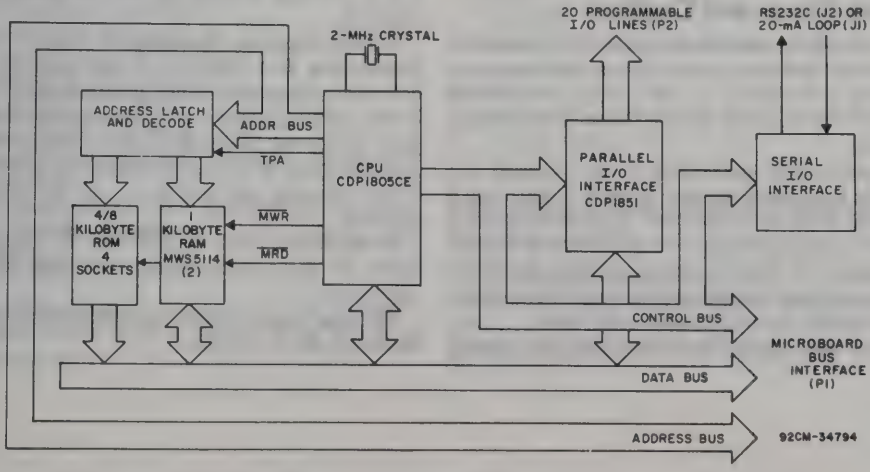


Fig. 1 — Block diagram of RCA Microboard Computer CDP18S608.

CDP18S608

storage and as memory pointers for subroutines, I/O, stacks and the like. One register each is designated for DMA and Interrupt pointers. The CDP1805CE provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

The CDP1805CE features 113 instructions, 22 more than its predecessor CDP1802. These additional instructions include several powerful instructions such as call and return, 16-bit register operations, and interrupt controls. The on-chip counter-timer with its control instructions provides a versatile tool for a variety of timing and counter applications. The counter-timer feature is described more fully below.

Memory. By means of two MWS5114 RAM's, the CDP18S608 provides 1 kilobyte of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S608 provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software.

Counter-Timer and Controls

The CDP1805CE provides an on-chip 8-bit presettable timer-counter. Software control of the counter allows the clock input to be TPA ÷ 32, EF1, EF2, TPA•EF1, or TPA•EF2, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 2 consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a load instruction to the counter, the counter

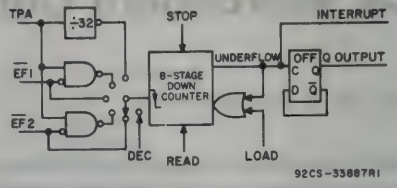


Fig. 2 — Timer/Counter diagram for CDP1805CE.

and its buffer register are loaded, and any previous interrupts cleared. If in an active state the counter must be stopped with a STPC instruction prior to issuing a LDC command. Read operations do not affect the counter.

The counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the EF1 terminal. The high-to-low transition decrements the counter.

2. Event Counter 2: Input to counter is connected to the EF2 terminal. The high-to-low transition decrements the counter.

3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC instruction.

4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

5. Pulse Duration Measurement 2: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF2}$ terminal is low. On the transition of $\overline{EF2}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) command clears the counter mode and stops counting.

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In addition to the five programmable modes, the **Decrement Counter Instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the Event Counter mode, the instruction should be used only after the mode has been cleared by a Stop Counter Instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This action is independent of the Counter mode and the Interrupt Enable flip-flops.

Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

Application

The Microboard Computer CDP18S608 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board. It may be conveniently operated in conjunction with other Microboard System components in the MSI Series of Industrial Chassis.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

Specifications

Microprocessor

CMOS 8-Bit CDP1805CE with
- Call and return instructions
- On-chip timer-counter
- 16 registers each 16-bits wide
- 16-bit register operations.

Memory Capacity

On-board RAM: 1 kilobyte.

On-board ROM/EPROM: 4 sockets for up to 8 kilobytes.

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map

On-board RAM: Low 1-kilobyte block in any 4-kilobyte block.

On-board ROM/EPROM: Depending on type and quantity of ROM's, and 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity

Parallel: 20 lines each programmable as input, output, or bidirectional.

Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.

Counter: 8-bit programmable timer-counter with 5 programmable modes.

Operating Temperature Range

-40°C to +85°C.

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm).

Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

With CMOS ROM's, with RS232C: +5 V at 32 mA, typical operating on-board RAM; 7 mA, off-board RAM.

With CMOS ROM's and 20-mA loop: +5 V at 52 mA, typical operating on-board RAM; 27 mA, off-board RAM.

Operational voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
-5 to -15 V at 8 mA, typical

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pin.

Clock

CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the Microboard Computer CDP18S608 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data

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sheet for the CDP1805CE (File No. 1309). These signals are summarized in Table XI which gives a list of the pins and the signals for the RCA Universal Backplane Connector (P1).

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high, $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S608 uses EF1 and EF2, conditioned by the secondary I/O address, to test the READY state of I/O ports A and B. The serial data interface input is presented directly on EF4 or EF3 chosen by link LK36. I/O devices using the INT line may make use of the EF lines to identify the device. They may also be used to indicate priority or status. The counter-timer may use EF1 or EF2 as an input under software control.

$\overline{INT}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

$\overline{DMAI}$, $\overline{DMAO}$ — Taken directly to the CPU pins and not utilized by the CDP18S608, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S608 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{MWR}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{MRD}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030A is impossible unless MRD is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions or by the counter output when enabled by the ETQ $(6809)_{16}$ instruction. The CDP18S608 may use Q as a serial data output to the RS232C and 20-mA data terminal drivers. It is also available for use through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A 2-MHz square-wave clock provided for general use. It is derived from the crystal-controlled oscillator in the CPU.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ — Two control inputs to the CPU which determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Not allowed
L	H	Reset
H	L	Pause
H	H	Run

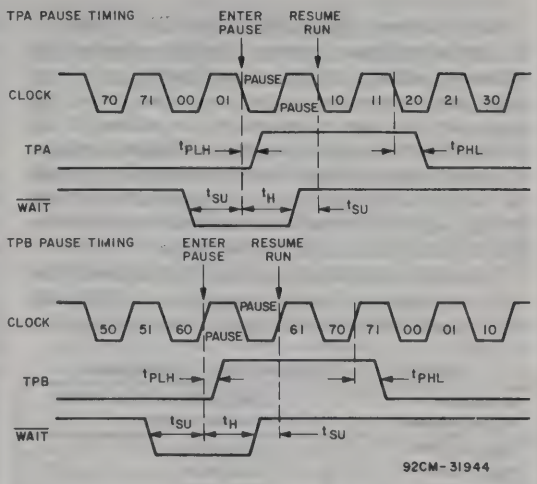
The functions of the modes are defined as follows:

RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 3).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.



NOTE:
PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 3 — Pause mode timing waveforms.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 3). When run is initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S608 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

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RAM Address. The RAM on the CDP18S608 is 1 kilobyte of contiguous memory. The high-order four bits of memory address are latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy 1 kilobyte starting at any even 4-kilobyte block in the memory space. Because the 4-kilobyte decoder enables the data buffers U5 and U8, the whole 4-kilobyte block selected for RAM is removed from the available memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

Table I — 4-Kilobyte Link Connections

4-Kilobyte Address Space	LINK LK10, LK11, or LK22 Pin Connections
0000 - 0FFF	1:16, 5:12
1000 - 1FFF	1:16, 6:11
2000 - 2FFF	1:16, 7:10
3000 - 3FFF	1:16, 8:9
4000 - 4FFF	2:15, 5:12
5000 - 5FFF	2:15, 6:11
6000 - 6FFF	2:15, 7:10
7000 - 7FFF	2:15, 8:9
8000 - 8FFF	3:14, 5:12
9000 - 9FFF	3:14, 6:11
A000 - AFFF	3:14, 7:10
B000 - BFFF	3:14, 8:9
C000 - CFFF	4:13, 5:12
D000 - DFFF	4:13, 6:11
E000 - EFFF	4:13, 7:10
F000 - FFFF	4:13, 8:9

LINK 11 is associated with the 1-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.

ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

Two types of links are provided and must be made up by the user to suit the particular ROM configuration selected. The first link type is for accommodating the type of ROM selected (CDP1834, 2708, 2758, or 2716). The second link type is for selecting the memory address space to be occupied by the ROM.

Link LK4 is an 18-pin dual-in-line arrangement with preprinted links to accommodate the 2716 ROM's. Table II gives the connections required for each ROM type.

Links LK10 and LK22 are 16-pin dual-in-line arrangements with no preprinted links. A DIP switch may be installed if frequent address changes are expected. Link LK10 provides the high-order four address bits decoded so that two links or jumpers place sockets XU24 and XU25 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK22 does the same for sockets XU26 and XU27. See Table I for address map and link connections.

To avoid having floating inputs to the gates, both links LK10 and LK22 should always have two jumpers. For example, if sockets XU26 and XU27 are used, LK22 may be jumpered the same as LK10. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

In instances where the ROM sockets are not fully occupied, it may be desirable to jumper links LK10 or LK22, or both, identically with LK11 so that the unused ROM space overlays the RAM space. Although the 1-kilobyte RAM usurps the whole of its 4-kilobyte assignment on LK11, the remaining 3 kilobytes may be filled by (1) leaving socket XU25 empty; (2) populating sockets XU24, XU26, and XU27 with 1 kilobyte devices; and (3) jumpering LK10, LK11, and LK22 identically. If there is to be no ROM on this board, this linking will prevent the unused sockets from being assigned to memory space perhaps needed by other system boards.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK10 and LK22 should be jumpered identically in accordance with Table I. Then, the ROM's should be installed in sockets XU25, XU27, XU24, and XU26, in order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK10 and LK22 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then, socket XU25 is the low 2 kilobytes and socket XU24 is the high 2 kilobytes of the 4-kilobyte block as set in LK10. Similarly, socket XU27 is the low 2 kilobytes and socket XU26 is the high 2 kilobytes of the 4-kilobyte block set in LK22.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with two-kilobyte ROM's type 2716. If all links are set up for the 2-kilobyte ROM's as shown in Table II for LK4, and LK10 and LK22 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM

in socket XU25 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU24, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU24 or socket XU25 while the other is occupied by a 1-kilobyte ROM. Socket XU27 (low 2 kilobytes) and socket XU26 (high 2 kilobytes) may be used in the same manner.

Table II — ROM Type Selection Links

Link LK4 Pins	ROM Type			
	CDP1834	2708	2758	2716*
1:18	X	OPEN	SHORTED	SHORTED
2:17	X	SHORTED	OPEN	OPEN
3:16	SHORTED	SHORTED	SHORTED	OPEN
4:15	OPEN	OPEN	OPEN	SHORTED
5:14	OPEN	OPEN	OPEN	SHORTED
6:13	SHORTED	SHORTED	SHORTED	OPEN
7:12	X	SHORTED	OPEN	OPEN
8:11	X	OPEN	OPEN	SHORTED
9:10	X	OPEN	SHORTED	OPEN

*X = don't care; Link LK4 is prewired to accept 2716.

I/O Operation

Serial I/O Interface. Serial data output is generated by the Q line from the CPU. Thus, software using the SET Q and RESET Q instructions generates data rate and format. Serial data input is presented to either EF3 or EF4, selectable by links as shown in Table III. The software uses the test branch instructions to decode incoming data.

Table III — Link Table for Serial Data In

Link LK36	Function
7:10	Data to EF3
8:9	Data to EF4

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2, respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire in the C5 holes. RS232C data terminals require that +12 volts be available on pin 20 of the backplane and −5 volts be available on pin 11.

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S608 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The CDP18S608 uses bit three as the group select; that is, the group number $(08)_{16}$ or $(0000\ 1000)_2$ is transmitted by the 61 output instruction to select the programmable I/O on board.

In general, although Interrupt is not gated by group select, External Flags are gated by the appropriate group select. The serial interface on the CDP18S608, however, uses either EF3 or EF4 with no gating by group number. Therefore, when the serial interface is wired for use, EF3 or EF4, whichever was chosen, is not generally available for other devices.

Parallel I/O Interface. The parallel I/O interface consists of 20 lines provided on connector P2. These 20 lines are generated by the CDP1851 Programmable I/O Interface and may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides the Q line, EF1 through EF4, CLEAR, three different voltages, and a logic ground.

For more detailed information on the Programmable

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I/O Interface CDP1851, refer to the data sheet for that device (File No. 1056).

The CDP1851 is assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data = 08 is required before read, write, or control I/O may be performed.

Signal ARDY conditioned by the group select generates EF1; BRDY and group select generates EF2. Link LK41, pins A and B may be jumpered if interrupt-driven software is to be used. Then, INTA or INTB generates INT unconditionally.

Once the group select is accomplished, N1 and N2 are used to address the CDP1851. The following read and write instructions are used to access data, status, and command registers.

62 or 63 — Write to control register
64 or 65 — Write to Port A data register (if A is an output)
66 or 67 — Write to Port B data register (if B is an output)
6A or 6B — Read status register
6C or 6D — Read Port A data register (if A is an input)
6E or 6F — Read Port B data register (if B is an input)

Using the READY Lines for Data Synchronization. The Port A and Port B RDY lines are presented to the CPU EF1 and EF2 lines when the group select is set. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU. Note that there is a logic reversal: when RDY is true, the EF is false. Because of the logic reversal and because the event of interest is RDY going false, the EF true test is used. A test for ARDY might use the B1 instruction (34) which would take the branch if ARDY were false.

When a port designated as on **output** port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true), and load the next output byte. When a port is designated as an **input** port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and then reads the input byte. **In this case, a dummy read after reset is necessary to raise the first RDY.**

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the INTERRUPT Line for Data Synchronization. If link LK41, A:B is jumpered, INTA or INTB generates INT to the CPU. INT is not conditioned by the group select. INT is set by the remote device sending STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table IV summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the group select 08_{16}, and then, either testing the RDY lines or reading the status byte. The low-order two bits of the status byte are: bit 0 = INTB; bit 1 = INTA.

Bidirectional Mode. Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, ARDY and ASTB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and BSTB becomes A OUTPUT STB. Each of the eight lines AD0—AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that output data is gated into AD0—AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode. Both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port

Table IV — READY and INTERRUPT Actions for Input and Output Modes.

		Output Port	Input Port
READY	Set By	Loading Data	Reading Data
	Reset by	STB leading edge	STB leading edge
INTERRUPT	Set by	STB trailing edge	STB trailing edge
	Reset by	Loading Data	Reading Data

A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O Interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the RCA Development Systems CDP18S005 or CDP18S007

Replacement of the CDS CPU Module CDP18S102 with the RCA Microboard Computer CDP18S608 requires some link changes on the CDP18S608 and wiring changes on the CDS backplane. These changes are:

LK43 — Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D. See Table V.

Table V-Changes on Link LK43 for Installation of CDP18S608 in Development Systems CDP18S005 and CDP18S007.

LK43	A:B	C:D	A:D	B:C
Microboard	*Closed	*Closed	Open	Open
CDS	Open	Open	Closed	Closed

*Preprinted links

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK36 — Serial Data In to external flag lines. In the CDS II, if the Terminal Interface Module CDP18S507 is not retained, connect pins 8:9 for EF4 to make the CDP18S608 the operator's terminal interface. If the CDP18S507 is retained, EF3 may be used for another serial interface purpose by connecting pins 7:10. In the CDS III, the UART module in location 14 is the operator's terminal interface and pins 7:10 and 8:9 may be left open.

LK36 — RNU to start ROM's at address 8000. Cut the wire jumper in pins 5:12. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed. This wire should be removed when the CPU Module CDP18S102 is re-installed. See Table VI.

LK10, 11, and 22 — Set up as previously described for the memory address desired, taking care that the CDS memories are not assigned to overlap the assignment of the CDP18S608 Microboard Computer.

Table VII summarizes the required CDS backplane wiring changes.

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Table VI — Changes on Link LK36 for Installation of CDP18S608 in Development Systems CDP18S005 and CDP18S007.

LK36	RNU 5:12	RNU 6:11	EF3 7:10	EF4 8:9
Microboard	¢Closed	Open	Open	¢Closed
CDS	Open	Closed	Open	Closed@

¢Wire jumpers installed
@Assumes the CDP18S608 serial interface is to be the operator terminal interface.

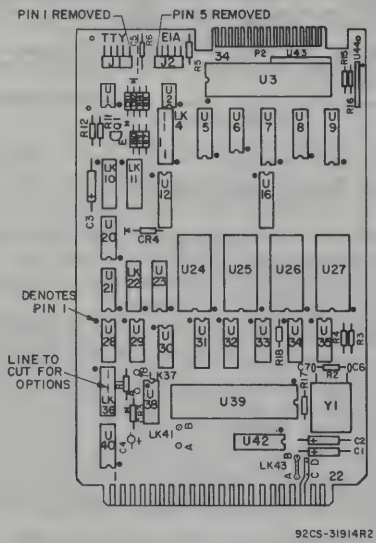

Fig. 4 — Layout diagram of RCA Microboard Computer CDP18S608.

Parts List

C1, C2, C3 = 15 μF, 20 V
C4 = 1.5 μF, 35 V
C6=39 pF
C7=10 pF

CR1, CR2, CR3, CR4 = 1N270
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP86016-1, keying plug — AMP 87077-1, or equivalent)

P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalents
Q1 = 2N5139

Table VII — Summary of Backplane Wiring Additions Needed When the CDP18S608 is Installed in the Development Systems CDP18S005 and CDP18S007.

From		To		
Slot	Pin	Slot	Pin	Function
12	X	13	20	-12 V
12	11	14	11	-5 V
12	12	10	D	RNU-P †

†This connection should be removed when the CDP18S102 is reinstalled.

R1 = 100 kΩ, ¼ W, 5%
R2 = 22 MΩ, ¼ W, 5%
R3, R4 = 22 kΩ, ¼ W, 5%
R5 = 3 kΩ, ¼ W, 5%
R6, R14 = 1 kΩ, ¼ W, 5%
R7 = 11 kΩ, ¼ W, 5%
R8 = 4.3 kΩ, ¼ W, 5%
R9 = 130 kΩ, ¼ W, 5%
R10 = 10 kΩ, ¼ W, 5%
R11 = 2.7 kΩ, ¼ W, 5%
R12 = 100 Ω, ¼ W, 5%
R15-R18 = 22 kΩ, ¼ W, 5%

U1 = CA3160
U2 = CA3140
U3 = CDP1851CE
U5, U8 = CDP1856CE
U6 = CD4069BE
U7 = CDP1867CE
U9 = CDP1866CE
U12, U16 = MWS5114
U20, U38 = resistor module, 22 kΩ, 14 pin
U21 = CD4001BE
U23 = CDP1858CE
U28, U29 = CD4012BE
U30 = CD4016BE
U31, U32 = CD4050BE
U33 = CD4025BE
U34 = CD4013BE
U35 = CD4023UBE
U39 = CDP1805CE
U40 = CD4093BE
U42 = resistor module, 22 kΩ, 16 pin
U43 = resistor module SIP, 22 kΩ, 10-pin
U44 = resistor, module SIP, 8-pin

XU3, XU39 = 40-pin socket
XU24-XU27 = 24-pin socket
Y1 = 2.00-MHz crystal

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Table VIII — List of Links and Their Functions

LK4	ROM Type Selection
*1:18	ROM Type 2758, 2716
2:17	ROM Type 2708
3:16	ROM Type 2758, 2708, or CDP1834
*4:15	ROM Type 2716
*5:14	ROM Type 2716
6:13	ROM Type 2758, 2708, or CDP1834
7:12	ROM Type 2708
*8:11	ROM Type 2716
9:10	ROM Type 2758
LK10	**ROM Decoding for XU24 and XU25**
*1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
5:12	$\overline{A13}$•$\overline{A12}$
*6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12
LK11	**RAM Decoding**
1:16	$\overline{A15}$•$\overline{A14}$
*2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
*5:12	$\overline{A13}$•A12
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12

LK22	ROM Decoding for XU26 and XU27
*1:16	$\overline{A15}$•$\overline{A14}$
2:15	$\overline{A15}$•A14
3:14	A15•$\overline{A14}$
4:13	A15•A14
*5:12	$\overline{A13}$•$\overline{A12}$
6:11	$\overline{A13}$•A12
7:10	A13•$\overline{A12}$
8:9	A13•A12
LK36	
*1:16	Not applicable to CDP1805CE
*2:15	CLEAR-N
3:14	Not applicable to CDP1805CE
4:13	WAIT-N
¢5:12	RNU-P from P1-3
6:11	RNU-P from P1-12 (CDS installation only)
7:10	EF3 for serial interface in
¢8:9	EF4 for serial interface in
LK37	
*A:B	+ 5 V V_{DD} to CDP1805CE
LK41	
A:B	Interrupt from PIO
LK43	
*A:B	Microboard system installation (EF4-N)
*C:D	Microboard system installation (+12 V)
A:D	CDS installation (+12 V)
B:C	CDS installation (EF4-N)

*Preprinted links
¢Wire jumpers installed

Table IX — Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+ 5V
31	EF2-N	32	− 5V/ − 15V
33	EF1-N	34	+ 12V/ + 15V

Table X — Serial Interfaces (J1) and (J2)

Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

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Table XI — Pin Terminals and Signals for the RCA Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Control
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Control
M	A0-P	Out	Multiplexed Address Bus	11	−5 V/−15 V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V	In	+5 volts dc	21	+5 V	In	+5 volts dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

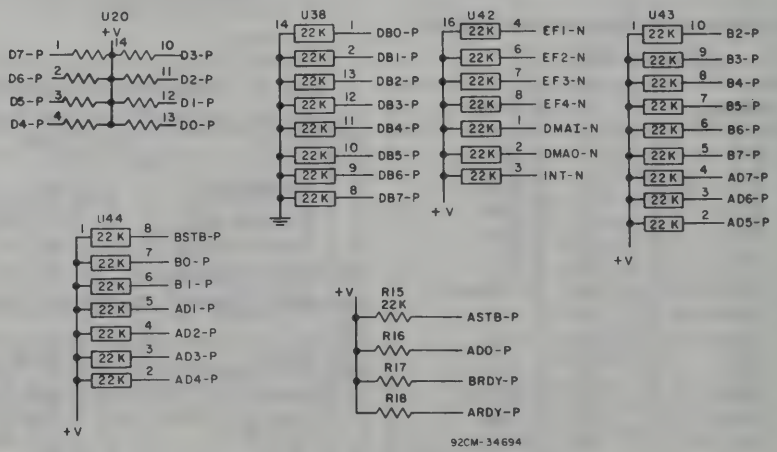

Fig. 5 — Pull-down and pull-up resistors.

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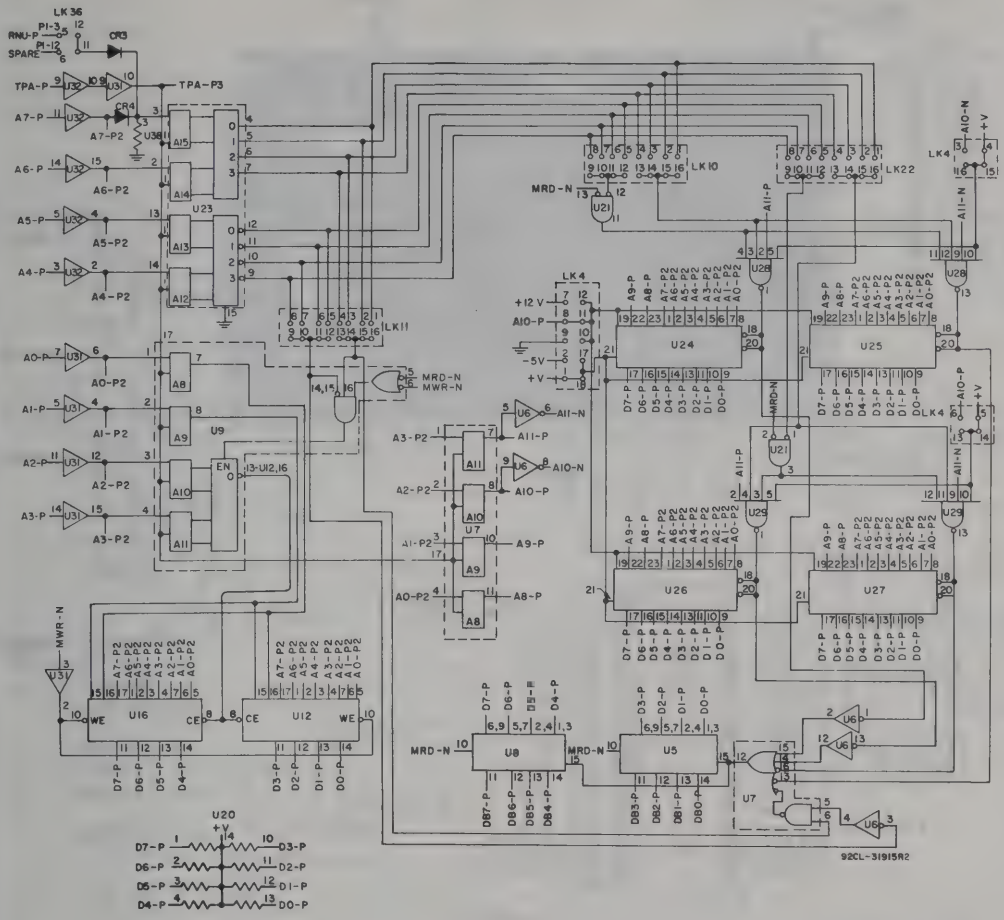

Fig. 6 — Logic diagram of Microboard Computer CDP18S608 — memory portion.

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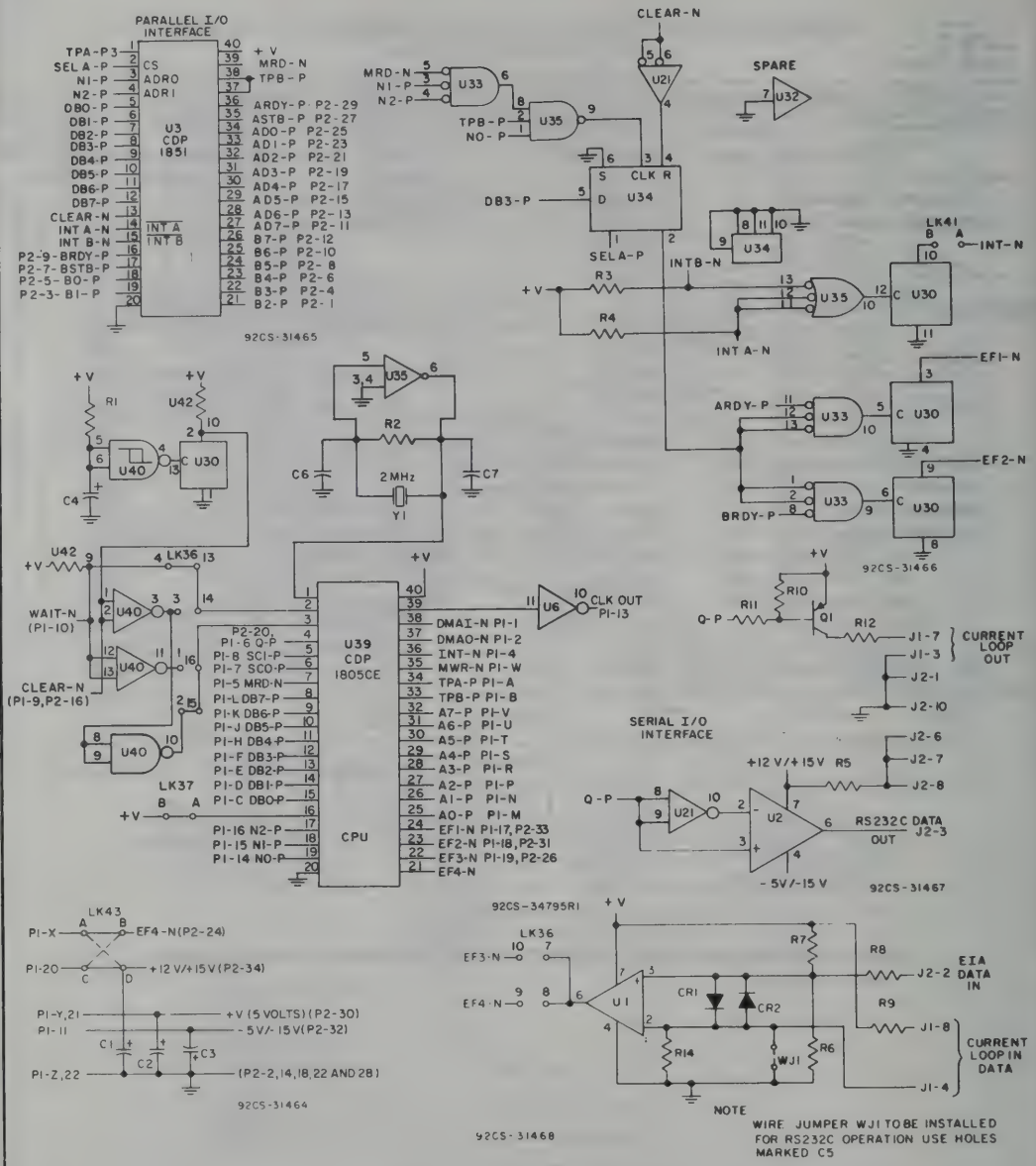

Fig. 7 — Logic diagram of Microboard Computer CDP18S608 — CPU and interface portion.

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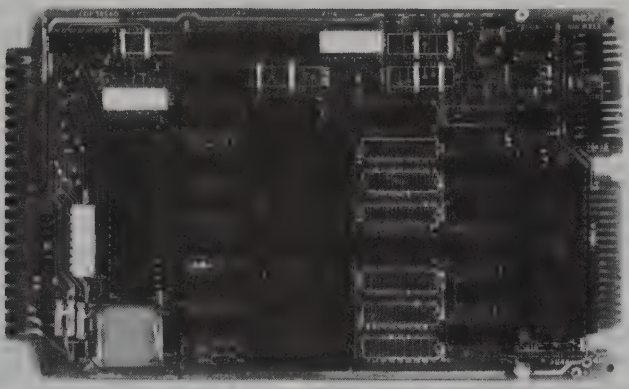


CDP18S609
RCA Microboard Computer

The RCA Microboard Computer CDP18S609 is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card. The card contains a CDP1805CE CPU with an on-chip counter-timer consisting of a presettable 8-bit down counter and a conditional divide-by-32 prescaler, a crystal-controlled clock, read-write memory, parallel I/O ports, programmable timer, power-on reset, and a breadboard for user-added features and interfaces. An on-board socket is provided for read-only memory enabling the user to select up to 4 kilobytes of mask-programmable ROM or EPROM depending on the applications. Because of the CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S609 Microboard Computer is designed to provide at low cost the key hardware for various microcomputer applications thereby enabling the designer to concentrate on the software and the special requirements of his specific application. The CDP18S609 is plug-in compatible with the RCA MSI Industrial Series Chassis. For detailed information on these Chassis, refer to **RCA Microboard Industrial Chassis Series Brochure,** MB-8.

Component Features

Central Processing Unit. The central processor for the CDP18S609 Microboard Computer is the 8-bit CMOS RCA Microprocessor CDP1805CE. The CDP1805CE

Features

- **Two Timers**
  - **Counter-timer on CDP1805CE**
  - **On-board programmable wide-range timer or retriggerable one-shot**
- **Low cost** • **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Current required: 4 mA (typ.)†**
- **High noise immunity** • **Power-on reset**
- **Crystal-clock CPU frequency of 2.097152 MHz**
- **Compatible with 1800-Series Development Systems**
- **Stand-alone capability** • **65,536-byte memory space**
- **1024 bytes of read/write memory**
- **Socket for up to 4 kilobytes of ROM/PROM**
- **1800-Series Microprocessor architecture with enhanced instruction set**
- **Flexible memory and I/O expansion**
- **8 parallel input and 8 parallel output lines**
- **4 flag inputs; Q output**
- **44-pin system interface**
- **Expandable by use of the RCA Microboard Universal Backplane**
- **Powered through either expansion or I/O connector**
- **Temperature range: −40° C to +85° C**
- **Small board size: 4.5 x 7.5 inches**
- **User area for breadboarding**

†With CMOS ROM

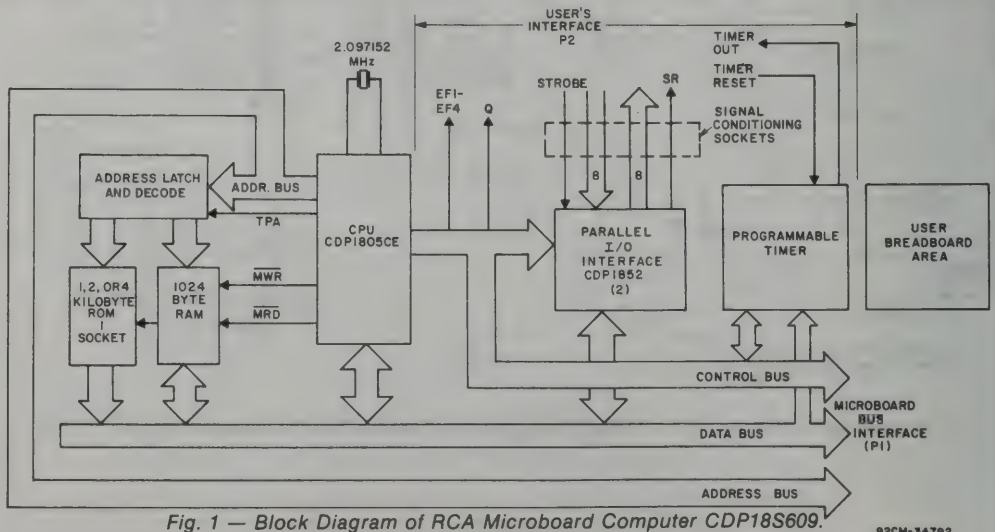


Fig. 1 — Block Diagram of RCA Microboard Computer CDP18S609.

has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1805CE provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

The CDP1805CE features 113 instructions, 22 more than its predecessor CDP1802. These additional instructions include several powerful instructions such as call and return, 16-bit register operations, and interrupt controls. The on-chip counter-timer with its control instructions provides a versatile tool for a variety of timing and counter applications. The counter-timer feature is described more fully below.

Counter-Timer and Controls

The CDP1805CE provides an on-chip 8-bit presettable timer-counter. Software control of the counter allows the clock input to be TPA ÷ 32, EF1, EF2, TPA•EF1, or TPA•EF2, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 2 consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a load instruction to the counter, the counter and its buffer register are loaded, and any previous interrupts cleared. If in an active state the counter must be stopped with a STPC instruction prior to issuing a LDC command. Read operations do not affect the counter.

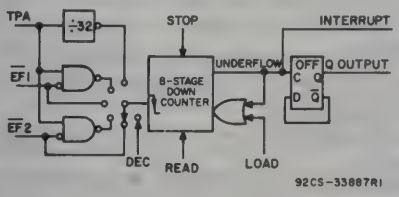


Fig. 2 — Timer/Counter diagram for CDP1805CE.

The counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the EF1 terminal. The high-to-low transition decrements the counter.

2. Event Counter 2: Input to counter is connected to the EF2 terminal. The high-to-low transition decrements the counter.

3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC instruction.

4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

5. Pulse Duration Measurement 2: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF2}$ terminal is low. On the transition of $\overline{EF2}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) command clears the counter mode and stops counting.

In addition to the five programmable modes, the **Decrement Counter Instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the Event Counter mode, the instruction should be used only after the mode has been cleared by a Stop Counter Instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This action is independent of the Counter mode and the Interrupt Enable flip-flops.

Memory. The CDP18S609 provides 1024 bytes of CMOS read-write memory. In addition, a socket is provided for one, two, or 4 kilobytes of nonvolatile read-only memory. RCA CDP1832 or CDP1834 mask-pro-

CDP18S609

grammed CMOS ROM's or 2758, 2716, or 2732 EPROM's may be used in this socket. The memory type selected may be placed independently in the 65,536-byte memory space.

I/O. By means of two parallel I/O ports, type CDP1852, the CDP18S609 provides eight input and eight output lines. Each port has a handshaking line to indicate whether a byte has been written to or read from a port. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. The user's edge connector provides, in addition to the two 8-line input and output ports, access to four flags, Q, timer output and control, and system clear.

Programmable Timer. The CDP18S609 provides a programmable timer independent of the on-chip timer-counter described below. This timer provides a means for generating periodic interrupts, square-wave output, or a programmable, retriggerable one-shot for either interrupt or external use. The start and retrigger signal may be generated by either software or external signal through the P2 connector. Detailed description of the timer is given in the section IO/Operation.

Application

The Microboard Computer CDP18S609 may stand alone and be operated as a complete system. It may be conveniently operated in conjunction with other Microboard Systems Components in the MSI Series of Industrial Chassis. The user breadboard area provides over four square inches of space for custom designs in addition to DIP locations for signal conditioning the I/O ports. Power may be supplied through the Microboard Bus Interface connector or through the I/O connector.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

When the CDP18S609 Microboard Computer is used with the Microboard Control and Display Module CDP18S640A, some debugging capability is available even in such a two-card minimum system. By means of the control switches provided with the CDP18S640A (RESET, RUN PROGRAM, RUN UTILITY, and STEP/CONT) and the six-digit hexadecimal display, the operator can observe the address and data sequences of both the fetch and execute cycles.

Specifications

Microprocessor
- CMOS 8-Bit CDP1805CE with
  - Call and return instructions
  - On-chip counter-timer
  - 16 registers each 16-bits wide
  - 16-bit register operations.

Memory Capacity
- On-board RAM: 1024 bytes.
- On-board ROM/EPROM: 1 socket for up to 4 kilobytes.
- Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map
- On-board RAM: 1024 bytes assignable to any 1-kilobyte block.
- Links are factory installed for RAM at address 4000_{16}.
- On-board ROM and EPROM:
- For CDP1832, 512 bytes assignable to any 1-kilobyte block.
- ROM will "wrap" in low and high half of assigned space.
- For CDP1834 or 2758, 1 kilobyte on any 1-kilobyte boundary. Links are preprinted for ROM 2716 at address 0000.
- For 2716, 2 kilobytes on any 2-kilobyte boundary.
- For 2732, 4 kilobytes on any 4-kilobyte boundary.

I/O Capacity
- Parallel: 8 input lines and 8 output lines with handshaking for each port.
- Counter: 8-bit counter-timer with 5 programmable modes.

Timer
- A programmable one- to-24 stage counter, having a period of 7.6 μs to 64 seconds which may be used as a retriggerable one-shot or a square-wave generator, with a programmable pause feature. Programmed or external start/stop.

Operating Temperature Range
- −40°C to +85°C

Dimensions
- 4.5 inches x 7.5 inches (114.3 x 190.5 mm)
- Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
- With CMOS ROM's: +5 V at 4 mA, typical operating.

Connectors
- System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Clock

CPU and Timer crystal-controlled 2.097152-MHz oscillator.

Microboard Bus Interface Signals (Connector P1)

The following signals, are generated or received by the Microboard Computer CDP18S609 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1805CE (File No. 1309) and to the **User Manual for the CDP1802 Microprocessor,** MPM-201. These signals are summarized in Table VII which gives a list of the pins and signals for the RCA Universal Backplane Connector (P1).

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from I/O to memory; when low, from memory to I/O. Available to user for I/O expansion at connector P1 (P1-14, P1-15, P1-16).

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$ External Flags — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The service request line from the input port is gated to EF3 by the group select signal through an open drain device.

$\overline{\text{INT}}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

The service request line from the input port can be connected through link LK36, pins 2:3 to the interrupt input. The timer can be connected through link LK36, pins 1:4 to the interrupt input. These two interrupts are distinguished by testing EF2 for timer and EF3 for input port. Of course, the proper group select must be set. (See section on I/O addressing.)

All connections to INT and the external flags should be through an open drain, open collector, or other high-impedance device, so that other boards may wire "OR" into these lines.

The conventional implementation of INTERRUPT I/O is to have each interrupting device identify itself by means of flag (EF1, EF2, EF3, or EF4) gated by its group select. In this way, the software may identify an interrupting device by polling the assigned group numbers, establishing priority by the order of polling.

$\overline{\text{DMAI}}$, $\overline{\text{DMAO}}$ — Taken directly to the CPU pins and not utilized by the CDP18S609, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

$\overline{\text{TPA}}$, $\overline{\text{TPB}}$ — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB

CDP18S609

trailing edge is used to latch output data from the data bus.

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S609 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$ — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge, when data lines are stable.

$\overline{\text{MRD}}$ — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030A is impossible unless MRD is properly used to condition data output.

Q — A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions or by the counter output when enabled by the ETQ $(6809)_{16}$ instruction. It is available for use through the Microboard Bus (P1) and Parallel I/O (P2) connectors and may be used to implement a serial output port. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT — A 2.097152-MHz square-wave clock signal derived from the CDP1805CE crystal-controlled oscillator.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ — Two control inputs to the CPU that determine the mode of operation.

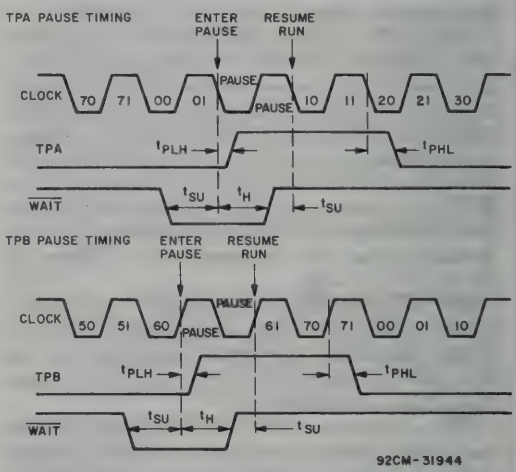
$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	Mode
L	L	Not Allowed
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 3).



NOTE:
PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 3 — Pause mode timing waveforms.

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement

the counter.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 3). When run is initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to the CDP18S609 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000. When the CDP18S609 is used in a stand-alone mode with a utility program located at 8000_{16}, an RNU-P signal must be supplied to connector P1-3 and Pins 7:10 must be connected on link LK6. When CDP18S609 is used with Control and Display Module CDP18S640A1 only pins 7:10 on link LK6 need be connected.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard DIP dimensions.

RAM Address — The 1-kilobyte RAM may be placed in any 1-kilobyte location within the 64-kilobyte memory space. Bits A4, A5, A6, and A7 are latched, at TPA trailing edge, in the CDP1858 (U17) becoming A12, A13, A14 and A15 of the high-order address byte. Bits A3 and A2 are latched in the CDP1867 (U16) becoming A10 and A11 of the high-order address.

Bits A15 and A14 are decoded into one of the 4 lines to link LK24, and A13 and A12 into 4 additional lines to LK24. One link for each pair of bits combined by gates in U11 and U12 provides a 4-kilobyte decode. Bits A10 and A11 inputs to the same gates provide the required 1-kilobyte decode which drives the RAM chips and the memory buffer drivers.

See Table I for detailed linking instructions.

ROM Address — One 24-pin socket is provided to accommodate various ROM types. Link LK31 is used to select the ROM type, links LK30, LK33 and LK25 are used to place the ROM in any place in memory space. ROM types which may be used are 2732 (4 kilobytes), 2716 (2 kilobytes), 2758 (1 kilobyte), CDP1834 (1 kilobyte), and CDP1832 (512 bytes; will wrap within a 1-kilobyte address space).

Link LK25 is used to establish the 4-kilobyte space, just as link LK24 does for the RAM. For 4-kilobyte ROM's the LK25 is sufficient. For 2-kilobyte ROM's the CDP1866 (U32) latches bit A11 and link LK30 selects the polarity for the ROM chip enable. For 1-kilobyte ROM's, the CDP1866 (U32) latches and decodes bits A10 and A11 for four lines to link LK30 where one line is chosen as Chip Enable.

See Tables II through IV for linkage for any ROM type.

I/O Operation

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus the number of addresses provided is 15-binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S609 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be

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exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

Input Port

The input port has, in addition to the eight data lines, a strobe (STB) line input which will latch the data into the port at its trailing edge. The port is a feed-through latch, so that when a strobe is not desired, the STB line may be left open or at a high logic level, allowing the data to feed through during the read instruction. If the STB is used, its trailing edge will generate a service request signal which is gated to EF3 by the proper I/O group select. The service request may be linked to the interrupt line if desired. The service request is cleared by reading the port or by power on or system clear.

The input port is pre-linked to I/O group $(08)_{16}$ and is read by an INP 2 $(6A)_{16}$ instruction.

Output Port

The output port has, in addition to its eight data lines, a

Table I — Memory Map and Link Connections for RAM

LK 24		LK4	Address
1-16	*5-12	2-7* and 4-5*	0000-03FF
		1-8 and 4-5	0400-07FF
		2-7 and 3-6	0800-0BFF
		1-8 and 3-6	0C00-0FFF
	6-11	2-7* and 4-5*	1000-13FF
		1-8 and 4-5	1400-17FF
		2-7 and 3-6	1800-1BFF
		1-8 and 3-6	1C00-1FFF
	7-10	2-7* and 4-5*	2000-23FF
		1-8 and 4-5	2400-27FF
		2-7 and 3-6	2800-2BFF
		1-8 and 3-6	2C00-2FFF
	8-9	2-7* and 4-5*	3000-33FF
		1-8 and 4-5	3400-37FF
		2-7 and 3-6	3800-3BFF
		1-8 and 3-6	3C00-3FFF
*2.15	*5-12	2-7* and 4-5*	4000-43FF
		1-8 and 4-5	4400-47FF
		2-7 and 3-6	4800-4BFF
		1-8 and 3-6	4C00-4FFF
	6-11	2-7* and 4-5*	5000-53FF
		1-8 and 4-5	5400-57FF
		2-7 and 3-6	5800-5BFF
		1-8 and 3-6	5C00-5FFF
	7-10	2-7* and 4-5*	6000-63FF
		1-8 and 4-5	6400-67FF
		2-7 and 3-6	6800-6BFF
		1-8 and 3-6	6C00-6FFF
	8-9	2-7* and 4-5*	7000-73FF
		1-8 and 4-5	7400-77FF
		2-7 and 3-6	7800-7BFF
		1-8 and 3-6	7C00-7FFF

LK24		LK4	Address
3-14	*5-12	2-7* and 4-5*	8000-83FF
		1-8 and 4-5	8400-87FF
		2-7 and 3-6	8800-8BFF
		1-8 and 3-6	8C00-8FFF
	6-11	2-7* and 4-5*	9000-93FF
		1-8 and 4-5	9400-97FF
		2-7 and 3-6	9800-9BFF
		1-8 and 3-6	9C00-9FFF
	7-10	2-7* and 4-5*	A000-A3FF
		1-8 and 4-5	A400-A7FF
		2-7 and 3-6	A800-ABFF
		1-8 and 3-6	AC00-AFFF
	8-9	2-7* and 4-5*	B000-B3FF
		1-8 and 4-5	B400-B7FF
		2-7 and 3-6	B800-BBFF
		1-8 and 3-6	BC00-BFFF
4-13	*5-12	2-7* and 4-5*	C000-C3FF
		1-8 and 4-5	C400-C7FF
		2-7 and 3-6	C800-CBFF
		1-8 and 3-6	CC00-CFFF
	6-11	2-7* and 4-5*	D000-D3FF
		1-8 and 4-5	D400-D7FF
		2-7 and 3-6	D800-DBFF
		1-8 and 3-6	DC00-DFFF
	7-10	2-7* and 4-5*	E000-E3FF
		1-8 and 4-5	E400-E7FF
		2-7 and 3-6	E800-EBFF
		1-8 and 3-6	EC00-EFFF
	8-9	2-7* and 4-5*	F000-F3FF
		1-8 and 4-5	F400-F7FF
		2-7 and 3-6	F800-FBFF
		1-8 and 3-6	FC00-FFFF

*Factory-installed link connections

Table II — Memory Map and Link Connections for ROM Types CPD1834 and 2758

LK31		LK33	LK25		LK30		Address
For 2758 1-10 and 4-7	For 1834 "DON'T CARE"	1-8 and 3-6	*1-16	*5-12	6-9	*1-14	0000-03FF
						2-13	0400-07FF
						3-12	0800-0BFF
						4-11	0C00-0FFF
				6-11		*1-14	1000-13FF
						2-13	1400-17FF
						3-12	1800-1BFF
						4-11	1C00-1FFF
				7-10		*1-14	2000-23FF
						2-13	2400-27FF
						3-12	2800-2BFF
						4-11	2C00-2FFF
				8-9		*1-14	3000-33FF
						2-13	3400-37FF
						3-12	3800-3BFF
						4-11	3C00-3FFF
			2-15	*5-12		*1-14	4000-43FF
						2-13	4400-47FF
						3-12	4800-4BFF
						4-11	4C00-4FFF
				6-11		*1-14	5000-53FF
						2-13	5400-57FF
						3-12	5800-5BFF
						4-11	5C00-5FFF
				7-10		*1-14	6000-63FF
						2-13	6400-67FF
						3-12	6800-6BFF
						4-11	6C00-6FFF
				8-9		*1-14	7000-73FF
						2-13	7400-77FF
						3-12	7800-7BFF
						4-11	7C00-7FFF
			3-14	*5-12		*1-14	8000-83FF
						2-13	8400-87FF
						3-12	8800-8BFF
						4-11	8C00-8FFF
				6-11		*1-14	9000-93FF
						2-13	9400-97FF
						3-12	9800-9BFF
						4-11	9C00-9FFF
				7-10		*1-14	A000-A3FF
						2-13	A400-A7FF
						3-12	A800-ABFF
						4-11	AC00-AFFF
				8-9		*1-14	BC00-B3FF
						2-13	B400-B7FF
						3-12	B800-BFFF
						4-11	BC00-BFFF

*Preprinted link connections.

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Table II — Memory Map and Link Connections for ROM Types CPD1834 and 2758 — Cont'd.

LK31		LK33	LK25		LK30		Address
For 2758 1-10 and 4-7	For 1834 "DON'T CARE"	1-8 and 3-6	4-13	*5-12	6-9	*1-14	C000-C3FF
						2-13	C400-C7FF
						3-12	C800-CBFF
						4-11	CC00-CFFF
				6-11		*1-14	D000-D3FF
						2-13	D400-D7FF
						3-12	D800-DBFF
						4-11	DC00-DFFF
				7-10		*1-14	E000-E3FF
						2-13	E400-E7FF
						3-12	E800-EBFF
						4-11	EC00-EFFF
				8-9		*1-14	F000-F3FF
						2-13	F400-F7FF
						3-12	F800-FBFF
						4-11	FC00-FFFF

*Preprinted link connections.

service request (SR) out. This SR goes high after data has been latched into the port and low at the following TPB. The SR pulse may be used to indicate the arrival of a new data byte, or ignored where not required. SR will be initially low, due to power on or system reset.

The output port is pre-linked to I/O group $(08)_{16}$ and is loaded by an OUT 2 $(62)_{16}$ instruction.

On-Board Timer

The on-board timer consists of a divide-by-eight prescaler CD4018BE driven by the 2.097152 MHz clock. The prescaler output goes to the CD4536BE (U13) counter which is a 24-stage binary counter with control inputs. The output of the CD4536BE counter drives a "D"-type flip-flop which in turn is gated to EF2 by the group select and also may be linked to the interrupt through link LK36 pins 1 and 4. The CD4536BE timer output is also provided on the user connector P2 pin 9.

Loading the control register resets the "D"-type flip-flop which generates EF2 flag and interrupt signal INT, so that interrupt or branch service should re-load the control register in order to remove the INT and flag EF2.

The timer is programmed by a control byte transmitted by an OUT 3 $(63)_{16}$ instruction, with I/O group $(08)_{16}$ selected.

The timer control register provides the following control functions (See Fig. 4 Programmable-Timer-Control Word Definition).

Bits 0 through 3 — The low-order four bits select the timer output to be one of the 16 high-order bits of the counter.

Bit 4 — Causes the low-order eight stages of the counter to be by-passed, in effect reducing it from a 24-bit to a 16-bit counter.

Bit 5 — Sets all stages of the counter, including the output.

Bit 6 — Resets all stages of the counter, including the output.

Bit 7 — Pause. While bit 7 is true, counting is suspended without disturbing the current value. When bit 7

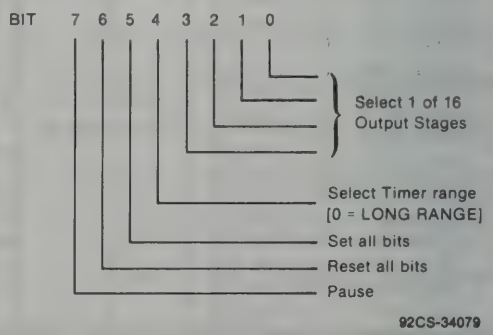

Fig. 4 — Programmable-timer-control word definition.

is cleared, counting resumes.

Square-Wave Generation — A square wave may be generated by setting bits 0 through 4 to the period desired with bits 5, 6 and 7 zeros. If interrupt is linked, the interrupt period will be a full period of the square wave as will EF2. Reset (bit 6 or pin P2-14) or Set (bit 5) may be used to stop at any time and restart in a known state (all zeros or all ones). (Note that after a Reset, the first interrupt is a full period but after a Set, the first interrupt is a half period, then a full period thereafter.) Pause (bit 7) may be used at any time to leave the counter in its present state until bit 7 is cleared, then resume.

One-Shot Method — Software release of Reset (bit 6) or hardware release of Reset (P2-14) starts the count at zero and when the stage selected by bits 0 through 4 is clocked true TIMER OUT-P goes high. When the stage is clocked false, TIMER OUT-P goes low and INT and EF2 are enabled. Either hardware or software can then do a reset to end the one-shot cycle. See Figs. 5a and 5b. If Set (bit 5) is used instead of Reset the cycle is the same except that it starts with TIMER-OUT-P going high and INT and EF2 are set after a half period. Pause (bit 7) may be

Table III — Memory Map and Link Connections for ROM Type 2716

LK31	LK25		LK33	LK30		Address
*2-9 and 4-7	*1-16	*5-12	*2-7 and 4-5	6-9	*1-14	0000-07FF
					2-13	0800-0FFF
		6-11			*1-14	1000-17FF
					2-13	1800-1FFF
		7-10			*1-14	2000-27FF
					2-13	2800-2FFF
		8-9			*1-14	3000-37FF
					2-13	3800-3FFF
	2-15	*5-12			*1-14	4000-47FF
					2-13	4800-4FFF
		6-11			*1-14	5000-57FF
					2-13	5800-5FFF
		7-10			*1-14	6000-67FF
					2-13	6800-6FFF
		8-9			*1-14	7000-77FF
					2-13	7800-7FFF
	*1-16	*5-12			*1-14	8000-87FF
					2-13	8800-8FFF
		6-11			*1-14	9000-97FF
					2-13	9800-9FFF
		7-10			*1-14	A000-A7FF
					2-13	A800-AFFF
		8-9			*1-14	B000-B7FF
					2-13	B800-BFFF
	2-15	*5-12			*1-14	C000-C7FF
					2-13	C800-CFFF
		6-11			*1-14	D000-D7FF
					2-13	D800-D7FF
		7-10			*1-14	E000-E7FF
					2-13	E800-EFFF
		8-9			*1-14	F000-F7FF
					2-13	F800-FFFF

*Preprinted link connections.

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Table IV — Memory Map and Link Connections for ROM Type 2732

LK30	LK33	LK31	LK25		Address
5-10 and 7-8	"DON'T CARE"	2-9 and 5-6	*1-16	*5-12	0000-0FFF
				6-11	1000-1FFF
				7-10	2000-2FFF
				8-9	3000-3FFF
			2-15	*5-12	4000-4FFF
				6-11	5000-5FFF
				7-10	6000-6FFF
				8-9	7000-7FFF
			3-14	*5-12	8000-8FFF
				6-11	9000-9FFF
				7-10	A000-AFFF
				8-9	B000-BFFF
			4-13	*5-12	C000-CFFF
				6-11	D000-DFFF
				7-10	E000-EFFF
				8-9	F000-FFFF

*Preprinted link connections.

used at any time to stop counting without resetting.

A retrigger function can be done before time out by asserting Reset or Set by either hardware or software. See Fig. 5b.

Another one-shot method uses an RC time constant to limit the duration of the TIMER-OUT signal. Replacing R6 with a capacitor and adding R5 causes the TIMER-OUT signal to be reset after the end of the RC time period. INT and EF2 are generated at the trailing edge of TIMER OUT. Unless Reset or Set are asserted, the counter continues to count its full period. The width of the positive timer output using this monostable option is poorly regulated. R5 should be greater than 2kΩ, R5=10kΩ and C4=1000 pF will give about 3 μs. (See Fig. 8.)

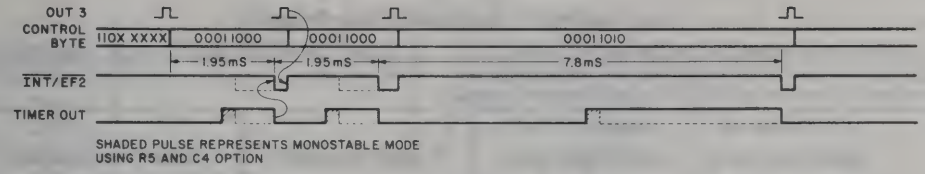
Machine Cycle Timing — The timer and the CPU share the 2.097152 MHz clock. Therefore, a definite relationship may be established between the counter and the CPU/software timing. Both the CPU TP generator and the counter pre-scaler are eight-state devices, so that the timer is incremented once per machine cycle, unless WAIT states are encountered, in which case the timer continues in real time while the CPU pauses.

In order to establish a known relationship between timer and CPU, the RESET and PAUSE bits in the control word are used together. When the two bits are cleared during the TPB of the execute cycle of the OUT3, the CD4018BE pre-scaler will generate the first increment to the timer three clock periods later and thereafter every eight clock periods. Because of the variance of propagation delays, a minus zero plus one clock period (2.097152 MHz), uncertainty exists in the phase relationship of the counter input and the machine cycles.

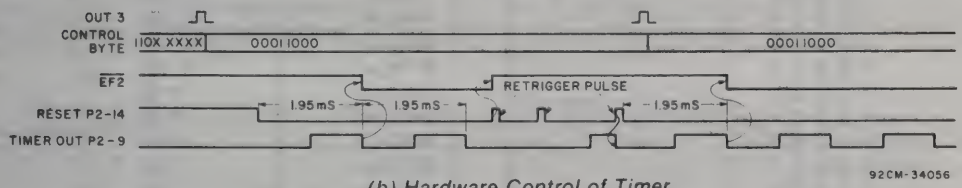
The timing then is such that the timer increment occurs after TPA of each machine cycle, and before TPB. EF2 is sampled during TPA of the execute cycle of the branch instruction inside the CPU, and INT will be taken after any execute cycle unless a DMA cycle is pending. One can thus calculate how many machine cycles are available for software action before the interrupt occurs or EF2 may be detected.

For long counts, an uncertainty of plus one or two machine cycles should be added, since the ripple time of the counter is long, up to 30 ns per stage. For worst case, one cycle per 10 stages of counter should be added for ripple time.

Use of the PAUSE bit alone allows a time out feature. This time can be an integral number of machine cycles. The counter is started by use of both the RESET and PAUSE bits; both set until the starting 63 command resets them. If the RESET bit alone or the external RESET is used to start, the PAUSE mode may have an uncertainty of plus 8 clock bits (3.8 μs).



(a) Software Generation of Variable Waveform



(b) Hardware Control of Timer

Fig. 5 — Timer waveforms of RCA Microboard Computer CDP18S609.

Breadboarding Area

The breadboard area is a 16 x 26 matrix of 0.035-inch plated-through holes on 0.10-inch centers. A total of seven holes are missing at corners, leaving 409 holes for mounting components.

To aid the user, some signals needed for Input-Output circuits are brought near to the breadboard area and provided with plated holes for solder attachment.

DB0-P through DB7-P are next to the breadboard area and marked by silkscreen.

N=7-P, N=6-P, N=5-P and N=4-P are next to U7 and marked by silkscreen. These signals are generated by the CDP1853 (U7) and are conditioned by the Group Select 08. Thus these signals provide the complete two-level I/O decoding and their timing is from the trailing edge of TPA to the trailing edge of TPB.

The data lines of the input and output ports are available on links LK2 and LK1, respectively.

+5 volts may be found adjacent to pin 24 of U5, and ground adjacent to pin 11 of link LK1.

Power-On Reset

An RC integrator (R1 and C1 in the control circuit logic diagram) provides a true CLEAR signal for approximately 100 milliseconds when the +5-volt supply is turned on. This signal drives the CLEAR input to the CPU, the parallel I/O interface, and the I/O group select latch. After the CLEAR signal, the I/O group select is reset, the output port and its SR is reset, and the input port goes to a high-impedance state with SR reset. The CPU initializes and starts processing at location 0000 provided the WAIT line is not asserted.

External circuits may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C1 will disable it and an external CLEAR must be provided.

Installation in the RCA Development Systems CDP18S005 and CDP18S007

Replacement of CDS CPU Module CDP18S102 or CDP18S102V1 with the RCA Microboard Computer CDP18S609 requires some link changes on the CDP18S609. These changes are:

LK34 — Cut A:B and C:D and install B:C. Install A:D only if a connection to the plus auxiliary voltage is needed on P2 or the breadboard area.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

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Table V — Setting the Timer Period

Bits 0 through 4 of the control byte determine the period generated by the Timer in all modes. Two ranges are available, determined by Bit 4. When Bit 4 is true, the range is 7.63 μs to 250 ms. When Bit 4 is false, the range is 1.95 ms to 64 s as shown.

LOW-RANGE CONTROL BITS 4 3 2 1 0	HIGH-RANGE CONTROL BITS 4 3 2 1 0	TIMER PERIOD	TIMER FREQUENCY Hz
1 0 0 0 0		7.629 μs	131,072
1 0 0 0 1		15.26 μs	65,536
1 0 0 1 0		30.52 μs	32,768
1 0 0 1 1		61.04 μs	16,384
1 0 1 0 0		122.1 μs	8192
1 0 1 0 1		244.1 μs	4096
1 0 1 1 0		488.3 μs	2048
1 0 1 1 1		976.6 μs	1024
1 1 0 0 0	0 0 0 0 0	1.953 ms	512
1 1 0 0 1	0 0 0 0 1	3.906 ms	256
1 1 0 1 0	0 0 0 1 0	7.813 ms	128
1 1 0 1 1	0 0 0 1 1	15.63 ms	64
1 1 1 0 0	0 0 1 0 0	31.25 ms	32
1 1 1 0 1	0 0 1 0 1	62.5 ms	16
1 1 1 1 0	0 0 1 1 0	125 ms	8
1 1 1 1 1	0 0 1 1 1	250 ms	4
	0 1 0 0 0	500 ms	2
	0 1 0 0 1	1.0 s	1
	0 1 0 1 0	2.0 s	0.5
	0 1 0 1 1	4.0 s	0.25
	0 1 1 0 0	8.0 s	0.125
	0 1 1 0 1	16.0 s	0.0625
	0 1 1 1 0	32.0 s	0.03125
	0 1 1 1 1	64.0 s	0.015625

LK35 — RNU to start ROM's at address 8000_{16}. Connect a wire jumper between 1 and 4 on link LK35, and remove the wire jumper between 2 and 3. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000_{16} after the RESET, RUN U switches are pressed. The wire jumper to the CDS backplane should be removed before the CDP18S102 is reinstalled.

Memory Address Links. The desired memory addresses should be set up according to the memory maps of Tables I through IV. Care should be taken that the CDS memories are not assigned to overlap the assignment of the CDP18S609 Microboard Computer.

Connector Matching Cables Available Separately

CPD18S517 — I/O Interface Cable

Fits connector P2; 36 inches long; 34-pin flat ribbon cable; output end unterminated.

CDP18S609

Table VI — List of Links and Their Functions

LK1 OUTPUT PORT		
†2:19	DO3-P	LINKS MAY BE CUT TO INSERT RESISTOR NETWORKS OR POWER DRIVERS, SUCH AS SN75498
†3:18	DO2-P	
†4:17	DO1-P	
†5:16	DO0-P	
†6:15	SR-P	
†7:14	DO7-P	
†8:13	DO6-P	
†9:12	DO5-P	
†10:11	DO4-P	

LK2 INPUT PORT		
†1:18	DI4-P	LINKS MAY BE CUT TO INSERT RESISTOR NETWORKS OR OTHER SIGNAL CONDITIONER
†2:17	DI5-P	
†3:16	DI6-P	
†4:15	DI7-P	
†5:14	DI0-P	
†6:13	DI1-P	
†7:12	DI2-P	
†8:11	DI3-P	
†9:10	STB-P	

LK4 RAM DECODING	
1:8	A10
*2:7	$\overline{A10}$
3:6	A11
*4:5	$\overline{A11}$

LK24 RAM DECODING	
1:16	$\overline{A15}.\overline{A14}$
*2:15	$\overline{A15}.A14$
3:14	$A15.\overline{A14}$
4:13	$A15.A14$
*5:12	$\overline{A13}.\overline{A12}$
6:11	$\overline{A13}.A12$
7:10	$A13.\overline{A12}$
8:9	$A13.A12$

LK25 ROM DECODING	
*1:16	$\overline{A15}.\overline{A14}$
2:15	$\overline{A15}.A14$
3:14	$A15.\overline{A14}$
4:13	$A15.A14$
*5:12	$\overline{A13}.\overline{A12}$
6:11	$\overline{A13}.A12$
7:10	$A13.\overline{A12}$
8:9	$A13.A12$

LK30 ROM DECODING	
†1:14	1 kilobyte — $\overline{A11}$-$\overline{A10}$, 2 kilobytes — $\overline{A11}$
2:13	1 kilobyte — $\overline{A11}$-$\overline{A10}$, 2 kilobytes — A11
3:12	1 kilobyte — A11-$\overline{A10}$
4:11	1 kilobyte — A11-A10
5:10	4 kilobytes
†6:9	1 kilobyte, 2 kilobytes
7:8	4 kilobytes

LK31 ROM TYPE SELECTION	
1:10	ROM Type 2758
*2:9	ROM Type 2716 or 2732
3:8	NOT USED
*4:7	ROM Type 2758 or 2716
5:6	ROM Type 2732

LK33 ROM DECODING	
1:8	1 kilobyte
*2:7	2 kilobytes
3:6	1 kilobyte
*4:5	2 kilobytes

LK34 CDS INSTALLATION	
*A:B	
*C:D	

LK35 RNU	
1:4	CDS
*2:3	MICROBOARD

*Factory-installed link connections
†Preprinted links

CDP18S609

INSTRUCTION **BITS**

61

7	6	5	4	3	2	1	0
80	40	20	10	08	04	02	01
GROUP NUMBERS 01, 02, 04, 08 OR 10, 20, . . . E0, F0.							

I/O GROUP SELECT

62

7	6	5	4	3	2	1	0

OUTPUT PORT (GROUP 08)

63

7	6	5	4	3	2	1	0
PAUSE	RESET	SET	$\overline{8}$	8	4	2	1
CONTROL			N				

Note bit 4 inversion

PROGRAMMABLE TIMER FREQUENCY = 262, 144 $\div 2^{N+1}$ Hz

64 65 66 67 Unused

69

7	6	5	4	3	2	1	0
80	40	20	10	08	04	02	01

RESERVED FOR READ I/O GROUP STATUS

6A

7	6	5	4	3	2	1	0

INPUT PORT (GROUP 08)

6B 6C 6D 6E 6F Unused

Fig. 6 — Programmers I/O Reference for RCA Microboard Computer CDP18S609.

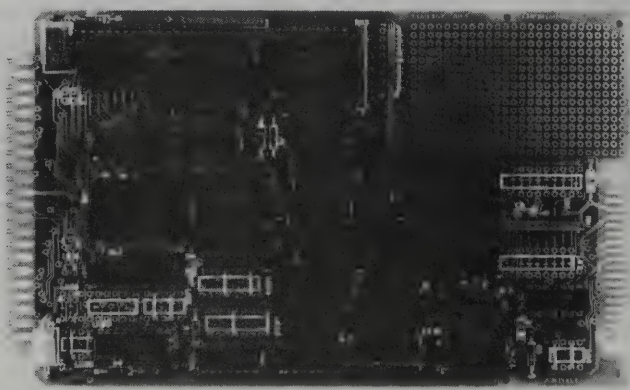


Table VII — Pin Terminals and Signals for the RCA Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

92CS-34444

Table VIII — Microboard Computer CDP18S609 Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	DI2-P	2	GND
3	DI1-P	4	DI3-P
5	DI0-P	6	DI4-P
7	STB-P	8	DI5-P
9	TIMER OUT-P	10	DI6-P
11	DO7-P	12	DI7-P
13	DO6-P	14	TIMER RESET-P
15	DO5-P	16	CLEAR-N
17	DO4-P	18	GND
19	DO3-P	20	Q-P
21	DO2-P	22	SPARE
23	DO1-P	24	EF4-N
25	DO0-P	26	EF3-N
27	SPARE	28	GND
29	SR-P	30	+5 V
31	EF2-N	32	+5 V/−15 V
33	EF1-N	34	+12 V/+15 V

CDP18S609

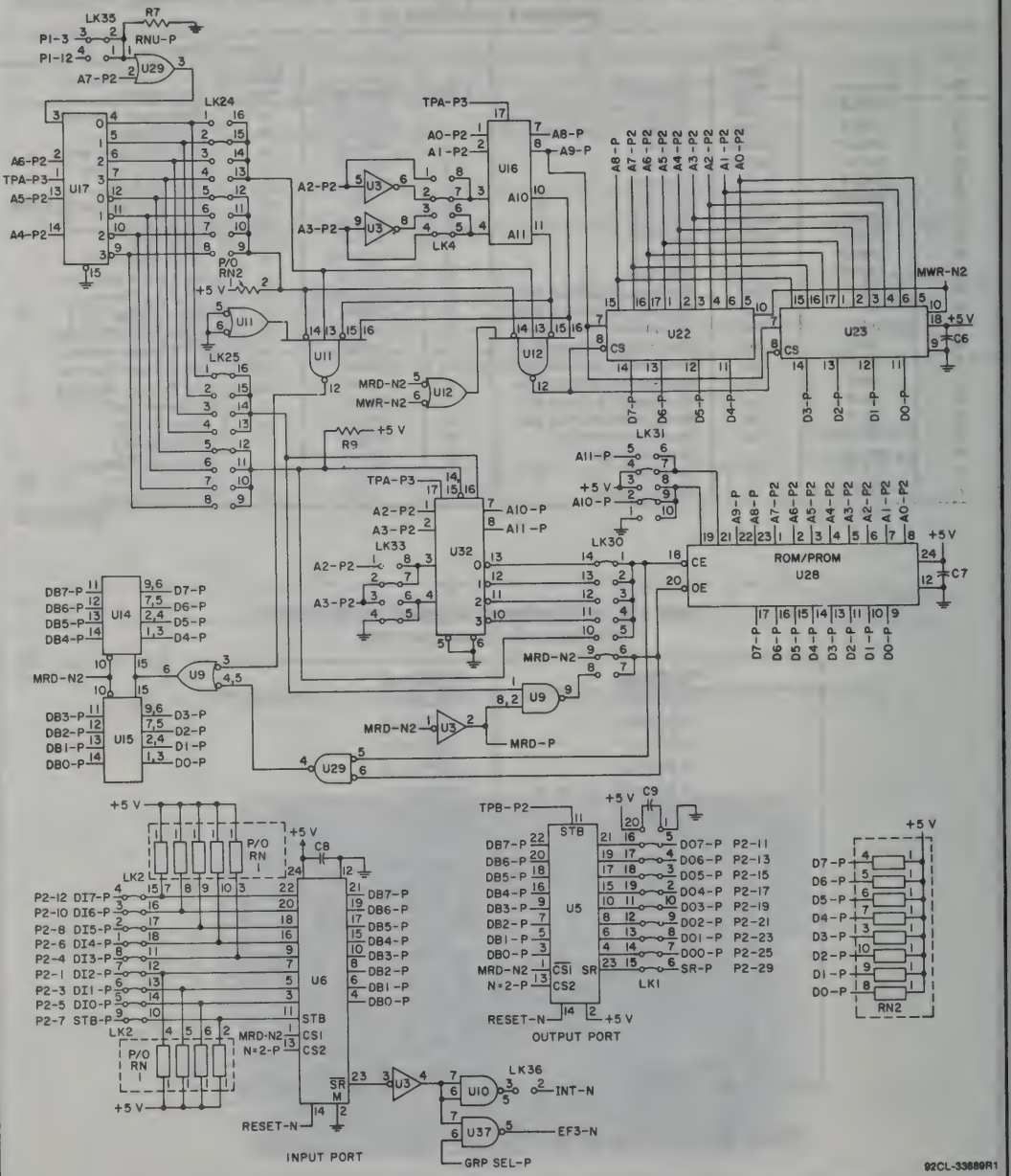


Fig. 7 — Logic Diagram of Microboard Computer CDP18S609 — Memory Portion.

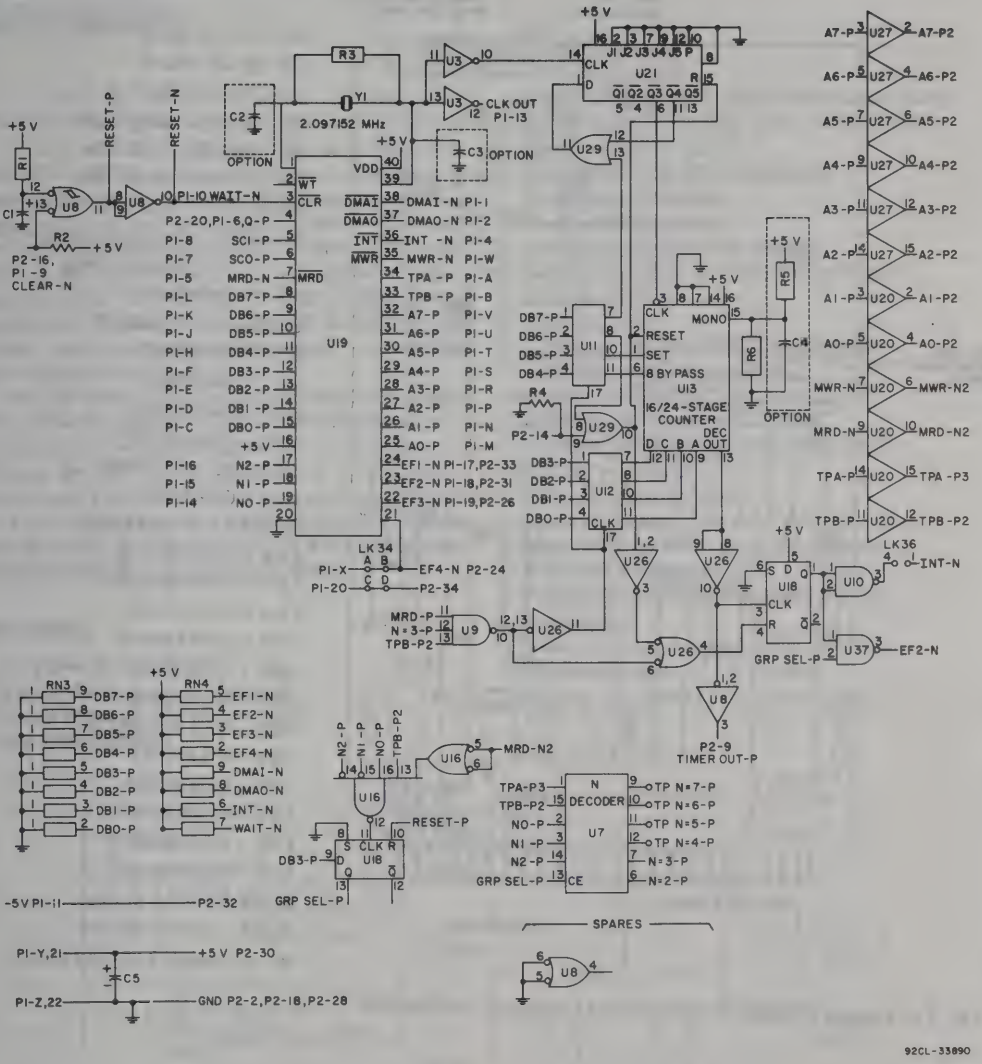


Fig. 8 — Logic Diagram of Microboard Computer CDP18S609 — CPU, Oscillator, and Buffer Portion.

CDP18S609

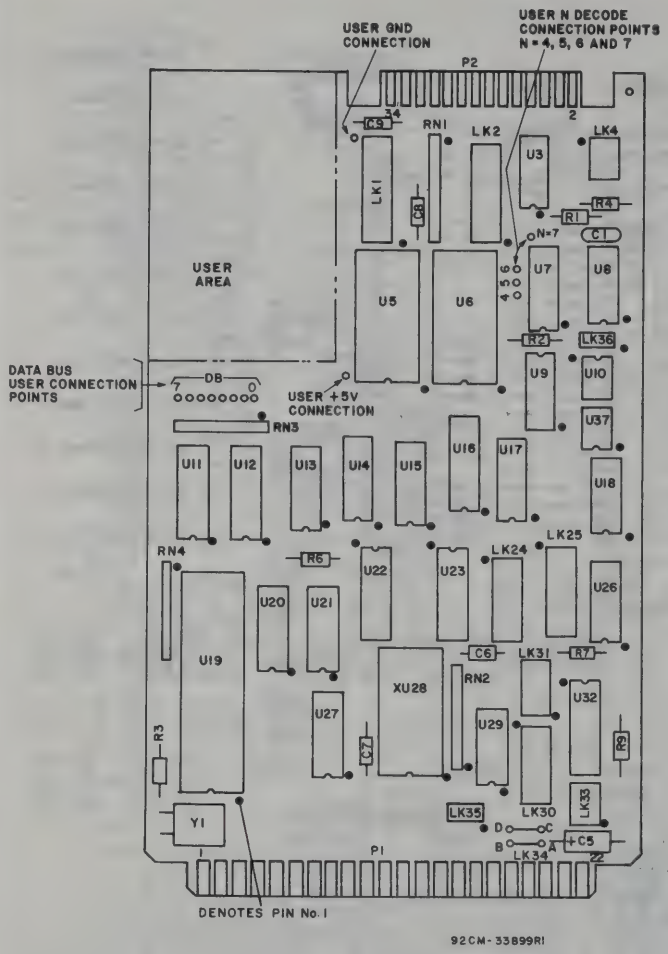


Fig. 9 —Layout Diagram of Microboard Computer CDP18S609.

PARTS LIST

C1 = 1.5 uF, 25 V
C5 =22 uF, 100 V
C6-C9 = 0.1 uF, 15 V
R1 = 100 kΩ, 1/4 W, 5%
R2 = 22 kΩ, 1/4 W, 5%
R3 = 22 MΩ, 1/4 W, 5%
R4,R6,R7,R9 = 22 kΩ, 1/4 W, 5%
RN1-RN4 = Resistor Module SIP, 22kΩ, 10-Pin
U3 = CD4069UBE
U5, U6 = CDP1852CE
U7 = CDP1853CE
U8 = CD4093BE
U9 =CD4023UBE
U10 = CD40107BE
U11, U12 = CDP1867CE
U13 = CD4536BE
U14, U15, = CD1856CE
U16 = CDP1867CE
U17 = CDP1858CE
U18 = CD4013BE
U19 = CDP1805CE
U20 = CD4050BE
U21 = CD4018BE
U22, U23 = MWS5114
U26 = CD4011BE
U27 = CD4050BE
U29 = CD4071BE
U32 = CDP1866CE
U37 = CD40107BE
XU19 = 40-Pin Socket
XU28 = 24-Pin Socket
Y1 = Crystal, 2.097152 MHz

CDP18S610

RCA Microboard Computer

The RCA Microboard Computer CDP18S610 is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card. The card contains a CDP1805CE CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a UART serial communications interface, power-on-reset, and expansion interface. Two on-board sockets are provided for read-only memory enabling the user to select 2 or 4 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of the CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S610 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and the special requirements of his specific applications. The CDP18S610 is plug-in compatible with the RCA MSI Industrial Chassis Series. For detailed information on these chassis, refer to **RCA Microboard Industrial Chassis Series Brochure**, MB-8.

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Current required: 8 to 28 mA (typ.)***
- **High noise immunity**
- **UART-driven serial I/O port with handshaking**
- **Crystal clock—selectable rates: 2.4576, 1.2288, 0.6144 or 0.3072 MHz**
- **Compatible with RCA 1800-Series Development Systems**
- **Stand-alone capability**
- **2 kilobytes of read/write memory**
- **Sockets for 2/4 kilobytes of ROM/PROM**
- **Counter-timer**
- **Power-on reset**
- **COSMAC Microprocessor architecture with enhanced instruction set**
- **Flexible memory and I/O expansion**
- **4 flag inputs; Q serial data output**
- **14 selectable baud rates: 50 to 19200 baud**
- **RS232C serial I/O**
- **65,536-byte memory space**
- **44-pin system interface**
- **Expandable by use of RCA Microboard Universal Backplane**
- **Powered through either expansion or I/O connector**
- **Wide temperature range: -40° C to 85° C**
- **Small board size: 4.5 x 7.5 inches**

*Depending whether 20-mA serial interface is used.

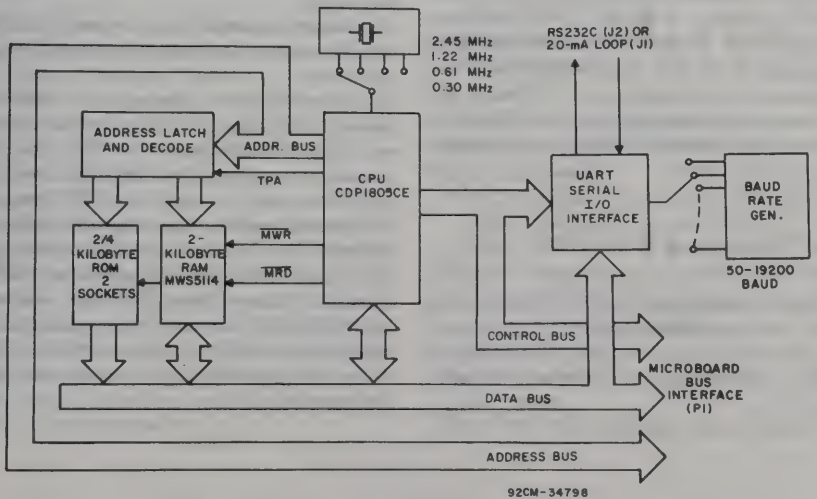


Fig. 1 - Block diagram of RCA Microboard Computer CDP18S610.

CDP18S610

Component Features

Central Processing Unit. The central processor for the CDP18S610 Microboard Computer is the RCA 8-bit CMOS Microprocessor CDP1805CE. The CDP1805CE has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks and the like. One register each is designated for DMA and interrupt pointers. The CDP1805CE provides a serial data-out connection, Q, and four external flag input pins, EF1 through EF4, whose logic levels may be tested with conditional branch instructions.

The CDP1805CE features 113 instructions, 22 more than its predecessor CDP1802. These additional instructions include several powerful instructions such as call and return, 16-bit register operations, and interrupt controls. The on-chip counter-timer with its control instructions provides a versatile tool for a variety of timing and counter applications. The counter-timer feature is described more fully below.

Memory. By means of four MWS5114 RAM's, the CDP18S610 provides 2 kilobytes of CMOS read-write memory. In addition, two sockets are provided for two or four kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM or 2758 or 2716-type EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on boundaries in accordance with the memory maps given in Tables I through IV.

I/O. A serial communications interface, having an EIA RS232C capability, is driven by an on-board UART, the CDP1854A. Handshaking lines are provided, as well as selectable baud rates. Right-angle headers are provided for the serial communications interface.

The data format is determined by software. There are 14 baud rates available, from 50 to 19200 bauds, selectable by a four-rocker DIP switch.

Counter-Timer and Controls

The CDP1805CE provides an on-chip 8-bit presettable timer-counter. Software control of the counter allows the clock input to be TPA + 32, EF1, EF2, TPA · EF1, or TPA · EF2, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 2 consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

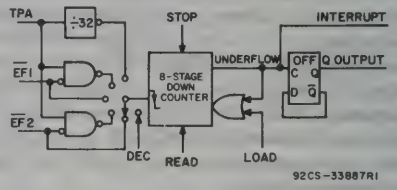


Fig. 2 - Timer/Counter diagram for CDP1805CE.

During a load instruction to the counter, the counter and its buffer register are loaded, and any previous interrupts cleared. If in an active state the counter must be stopped with a STPC instruction prior to issuing a LDC command. Read operations do not affect the counter.

The counter has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the EF1 terminal. The high-to-low transition decrements the counter.

2. Event Counter 2: Input to counter is connected to the EF2 terminal. The high-to-low transition decrements the counter.

3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC instruction.

4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

5. Pulse Duration Measurement 2: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF2}$ terminal is low. On the transition of $\overline{EF2}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but the counter will continue.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) command clears the counter mode and stops counting.

In addition to the five programmable modes, the **Decrement Counter Instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the Event Counter mode, the instruction should be used only after the mode has been cleared by a Stop Counter Instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This action is independent of the Counter mode and the Interrupt Enable flip-flops.

Application

The CDP18S610 may be conveniently operated in conjunction with other Microboard Systems Components in the MSI Series of Industrial Chassis.

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

When the CDP18S610 Microboard Computer is used with the Microboard Control and Display Module CDP18S640A1, some debugging capability is available even in such a two-card minimum system. By means of the control switches provided with the CDP18S640A1 (RESET, RUN PROGRAM, RUN UTILITY, AND STEP/CONT) and the six-digit hexadecimal display, the operator can observe the address and data sequences of both the fetch and execute cycles.

Specifications

Microprocessor

CMOS 8-bit CDP1805CE with
- On-chip timer-counter
- 16 registers each 16 bits wide
- 16-bit register operations
- Call and return instructions

Memory Capacity

On-board RAM: 2 kilobytes

On-board ROM/EPROM: 2 sockets for up to 4 kilobytes

Off-board Expansion: Any user-specified combination of RAM, ROM, and EPROM, up to a total of 65,536 bytes on-board and off-board

Memory Address Map

(See Tables I through IV)

On-board RAM: 2 kilobytes contiguous on any 2 kilobyte boundary: Links are preprinted for RAM at address 8800_{16}

On-board ROM and EPROM: For CDP1834 and 2758, 2 kilobytes contiguous on any 2-kilobyte boundary

For 2716, 4 kilobytes contiguous on any 4-kilobyte boundary. Links are preprinted for ROM types CDP1834 and 2758 and for address start at 8000.

I/O Capacity

Serial: UART-controlled input and output lines. EIA RS232C interface. User-programmed data format. 14 selectable baud rates, 50 to 19200 baud. CTS and RTS control lines.

Counter: 8-bit programmable counter-timer with 5 programmable modes.

Operating Temperature Range

−40°C to 85°C

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements

With CMOS ROM's and RS232C: +5 V at 32 mA, typical operating on-board RAM, 8 mA offboard RAM

Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers

Serial I/O: One right-angle header, 10 pins

CDP18S610

Clock

CPU and Interface: crystal-controlled oscillator; selectable frequencies: 2.4576, 1.2288, 0.6144, and 0.3072 MHz. A preprinted link selects 2.4576 MHz as the CPU clock frequency.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the RCA Microboard Computer CDP18S610 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1805CE (File No. 1309) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201. These signals are summarized in Table VIII which gives a list of the pins and the signals for the RCA Universal Backplane Connector (P1).

DB7 through DB0—Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2—Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the MRD line. When high MRD indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$—Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The UART Serial Data In (SDI) line is gated to EF4 by the UART Group Select through a pre-printed link. EF1 or EF2 may be used by the counter-timer under software control.

$\overline{INT}$—Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{INT}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter. The interrupt line from the UART can be presented directly to this input via link LK1.

$\overline{DMA1}$, $\overline{DMA0}$—Taken directly to the CPU pins and not utilized by the CDP18S610, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0—State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB—Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0—Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S610 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{MWR}$—A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{MRD}$—A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers

in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030A is impossible unless MRD is properly used to condition data output.

Q—A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions or by the counter output when enabled by the ETQ $(6809)_{16}$ instruction. It is available for use through the Microboard Bus (P1) connector. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT—A square-wave clock signal derived from an external crystal-controlled oscillator. One of four clock frequencies can be selected, 2.4576, 1.2288, 0.6144, or 0.3072 MHz. This signal is made available on connectors P1 and P2 by a preprinted link across pins 8 and 5 of link LK8. A preprinted link across pins 7 and 8 of link LK3 selects 2.4576 MHz as the CPU clock frequency.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$—Two control inputs to the CPU that determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Not Allowed
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

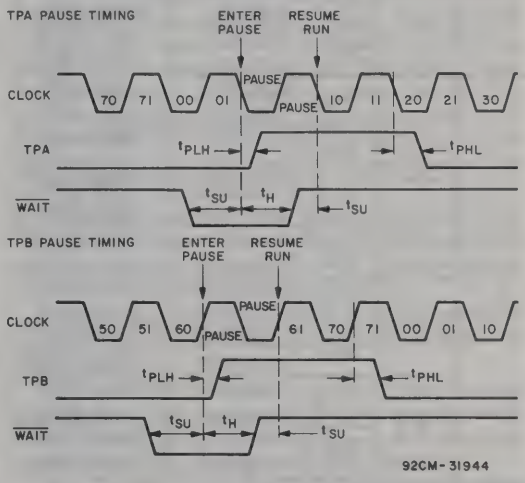
RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P → T, and then registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 3).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 3). When run is initiated from the Reset operation, the first machine cycle following Reset



NOTE:
PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 3 - Pause mode timing waveforms.

is always the initialization cycle. The initialization cycle is then followed by a DMA(S2) cycle or fetch (S0) from location 0000 in memory.

RNU - Run Utility Software: A signal supplied to the CDP18S610 to force the most significant address bit true. As a result, the program start is at memory location 8000 instead of 0000. When the CDP18S610 is used in a stand-alone mode and a utility program is included at 8000, an RNU-P signal must be supplied to connector P1-3, and pins 12:1 must be connected on link LK8. When the

CDP18S610

Table I - Memory Map and Link Connections for RAM

	LK5	LK4	RAM	Address
1:16	*5:12	7:10	U16/U18 U15/U17	0000-03FF 0400-07FF
		*8:9	U16/U18 U15/U17	0800-0BFF 0C00-0FFF
	6:11	7:10	U16/U18 U15/U17	1000-13FF 1400-17FF
		*8:9	U16/U18 U15/U17	1800-1BFF 1C00-1FFF
	7:10	7:10	U16/U18 U15/U17	2000-23FF 2400-27FF
		*8:9	U16/U18 U15/U17	2800-2BFF 2C00-2FFF
	8:9	7:10	U16/U18 U15/U17	3000-33FF 3400-37FF
		*8:9	U16/U18 U15/U17	3800-3BFF 3C00-3FFF
2:15	*5:12	7:10	U16/U18 U15/U17	4000-43FF 4400-47FF
		*8:9	U16/Y18 U15/U17	4800-4BFF 4C00-4FFF
	6:11	7:10	U16/U18 U15/U17	5000-53FF 5400-57FF
		*8:9	U16/U18 U15/U17	5800-5BFF 5C00-5FFF
	7:10	7:10	U16/U18 U15/U17	6000-63FF 6400-67FF
		*8:9	U16/U18 U15/U17	6800-6BFF 6C00-6FFF
	8:9	7:10	U16/U18 U15/U17	7000-73FF 7400-77FF
		*8:9	U16/U18 U15/U17	7800-7BFF 7C00-7FFF
*3:14	*5:12	7:10	U16/U18 U15/U17	8000-83FF 8400-87FF
		*8:9	U16/U18 U15/U17	8800-8BFF 8C00-8FFF
	6:11	7:10	U16/U18 U15/U17	9000-93FF 9400-97FF
		*8:9	U16/U18 U15/U17	9800-9BFF 9C00-9FFF
	7:10	7:10	U16/U18 U15/U17	A000-A3FF A400-A7FF
		*8:9	U16/U18 U15/U17	A800-ABFF AC00-AFFF
	8:9	7:10	U16/U18 U15/U17	B000-B3FF B400-B7FF
		*8:9	U16/U18 U15/U17	B800-BBFF BC00-BFFF
4:13	*5:12	7:10	U16/U18 U15/U17	C000-C3FF C400-C7FF
		*8:9	U16/Y18 U15/U17	C800-CBFF CC00-CFFF
	6:11	7:10	U16/U18 U15/U17	D000-D3FF D400-D7FF
		*8:9	U16/U18 U15/U17	D800-DBFF DC00-DFFF
	7:10	7:10	U16/U18 U15/U17	E000-E3FF E400-E7FF
		*8:9	U16/U18 U15/U17	E800-EBFF EC00-EFFF
	8:9	7:10	U16/U18 U15/U17	F000-F3FF F400-F7FF
		*8:9	U16/U18 U15/U17	F800-FBFF FC00-FFFF

*Preprinted link connections.

CDP18S610 is used with Control and Display Module CDP18S640A1, the preprinted link LK8 pins 12:1, provides the RNU to the on-board memory decoder. Since the ROM sockets are pre-linked to start at 8000, there would be a conflict with the ROM on the CDP18S640A1, unless the linking is changed to place the on-board RAM and ROM elsewhere in memory space. See Tables I through IV.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described in Tables I through IV. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address: The CDP18S610 Microboard Computer has two kilobytes of contiguous memory which can occupy any 2-kilobyte block in memory space on 2-kilobyte boundaries. The high-order byte of the memory address is latched and decoded. Bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two wire jumpers on link LK5. One jumper on link LK4 will

enable the next level of decoding; selecting either A11 or A11 inverted enables the RAM decoder U21. If the latched bit A11 is not inverted, the low half of a 4-kilobyte block is enabled. Bit A10 will next select 1-kilobyte segments within the 2-kilobyte block.

To set up the RAM address, it is necessary to install two jumpers in link LK5 and one in link LK4 as given in the memory map of Table I. As an alternative, DIP switches may be installed if frequent link changes are anticipated.

To avoid having floating inputs to CMOS gates, links LK5 and LK4 must always have jumpers installed.

ROM Address: Two 24-pin sockets (XU9 and XU10) are provided for user-programmed ROM's. Three ROM types are suitable: CDP1834 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes). The address decoding technique prevents "wrap-around" in memory space for any memory type.

Table II shows the LK3 and LK4 link connections needed for the ROM selected. Tables III and IV give the additional link connections needed and the memory address information.

Table II - Connections for Link LK3 and LK4 for ROM

Link	CDP1834 or 2758	2716
LK4 1:16*	C	O
LK4 2:15	O	C
LK4 4:13	O	C
LK4 5:12*	X	O
LK4 6:11	X	O
LK3 1:14*	C	O
LK3 2:13	O	C

O=Open; C=Closed; X=See Table III. *Preprinted link connections

For testing or debugging, all ROM space can be inhibited by connecting A and B on link LK7.

When ROM's CDP1834 or 2758 are used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. One jumper on link LK4 enables the next level of decoding; selecting either A11 or A11 inverted enables ROM decoder U20.

If bit A11 is not inverted, the low half of the 2-kilobyte block is selected. If bit A11 is inverted by U19, the high half of the block is enabled. Another jumper on link LK4 connects bit A10 to the decoder selecting one of the two 1-kilobyte blocks. For the CDP1834 and 2758, input pin 19 of the ROM is grounded. Note that to avoid floating inputs, links LK6 and LK4 must have jumpers installed.

When ROM 2716 is used, memory address bits A15, A14, A13, and A12 select one of 16 4-kilobyte blocks by means of two jumpers on link LK6. With another jumper connecting pins 2:15 on link LK4, bit A11 now selects 2-kilobyte segments within a 4-kilobyte block. Link LK3 is used to connect address bit A10 to pin 19 of the 2716 ROM.

Note that with type 2716 also, jumpers must always be present to avoid floating inputs to CMOS gates. Note that the CDP18S610 is initially configured for ROM types CDP1834 and 2758 at address 8000.

Input/Output Interfacing

Serial I/O Interfacing: Serial output data is generated by the UART. In Microboard systems including the Control and Display Module CDP18S640A1, the utility software UT61 sets the data format. This format is one start bit, eight data bits (no parity), and two stop bits. The utility also determines when to read data from the UART and when to write to it by reading its status word. The user, of course, has the option in a stand-alone system of writing his own UART routine.

The UART interrupt line is wired to link LK1 where the user may jumper it either to the CPU's interrupt input or to one of the flag lines (EF3) or both. See the data sheet for UART CDP1854A (File No. 1193).

Because the SDI line is connected to EF4 by means of a preprinted link, a break condition may be conveniently detected.

Any one of the 14 baud rates available from the baud rate generator can be selected through a four-bit binary code determined by the setting of a four-rocker DIP switch. The switch settings are given in Table V.

Two-Level I/O Interfacing: During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard System the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded

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Table III – Additional Link Connections and Memory Addresses for ROM Types CDP1834 and 2758

LK6		LK4	ROM	Address
1:16	*5:12	*5:12	U9	0000-03FF
			U10	0400-07FF
		6:11	U9	0800-0BFF
			U10	0C00-0FFF
	6:11	*5:12	U9	1000-13FF
			U10	1400-17FF
		6:11	U9	1800-1BFF
			U10	1C00-1FFF
	7:10	*5:12	U9	2000-23FF
			U10	2400-27FF
		6:11	U9	2800-2BFF
			U10	2C00-2FFF
	8:9	*5:12	U9	3000-33FF
			U10	3400-37FF
		6:11	U9	3800-3BFF
			U10	3C00-3FFF
2:15	*5:12	*5:12	U9	4000-43FF
			U10	4400-47FF
		6:11	U9	4800-4BFF
			U10	4C00-4FFF
	6:11	*5:12	U9	5000-53FF
			U10	5400-57FF
		6:11	U9	5800-5BFF
			U10	5C00-5FFF
	7:10	*5:12	U9	6000-63FF
			U10	6400-67FF
		6:11	U9	6800-6BFF
			U10	6C00-6FFF
	8:9	*5:12	U9	7000-73FF
			U10	7400-77FF
		6:11	U9	7800-7BFF
			U10	7C00-7FFF

LK6		LK4	ROM	Address
*3:14	*5:12	*5:12	U9	8000-83FF
			U10	8400-87FF
		6:11	U9	8800-8BFF
			U10	8C00-8FFF
	6:11	*5:12	U9	9000-93FF
			U10	9400-97FF
		6:11	U9	9800-9BFF
			U10	9C00-9FFF
	7:10	*5:12	U9	A000-A3FF
			U10	A400-A7FF
		6:11	U9	A800-ABFF
			U10	AC00-AFFF
	8:9	*5:12	U9	B000-B3FF
			U10	B400-B7FF
		6:11	U9	B800-BBFF
			U10	BC00-BFFF
4:13	*5:12	*5:12	U9	C000-C3FF
			U10	C400-C7FF
		6:11	U9	C800-CBFF
			U10	CC00-CFFF
	6:11	*5:12	U9	D000-D3FF
			U10	D400-D7FF
		6:11	U9	D800-DBFF
			U10	DC00-DFFF
	7:10	*5:12	U9	E000-E3FF
			U10	E400-E7FF
		6:11	U9	E800-EBFF
			U10	EC00-EFFF
	8:9	*5.12	U9	F000-F3FF
			U10	F400-F7FF
		6:11	U9	F800-FBFF
			U10	FC00-FFFF

*Preprinted link connections.

by any Microboard in the system having an I/O function. Any I/O function is assigned to a group number and only responds when its group number and its appropriate N register code are transmitted.

- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S610 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The user may place the UART in one of two I/O groups by the position of a jumper wire on link LK1. If

Table IV - Additional Link Connections and Memory Addresses for ROM Type 2716

	LK6	ROM	Address
*1:16	*5:12	U9	0000-07FF
		U10	0800-0FFF
	6:11	U9	1000-17FF
		U10	1800-1FFF
	7:10	U9	2000-27FF
		U10	2800-2FFF
	8:9	U9	3000-37FF
		U10	3800-3FFF
2:15	*5:12	U9	4000-47FF
		U10	4800-4FFF
	6:11	U9	5000-57FF
		U10	5800-5FFF
	7:10	U9	6000-67FF
		U10	6800-6FFF
	8:9	U9	7000-77FF
		U10	7800-7FFF
3:14	*5:12	U9	8000-87FF
		U10	8800-8FFF
	6:11	U9	9000-97FF
		U10	9800-9FFF
	7:10	U9	A000-A7FF
		U10	A800-AFFF
	8:9	U9	B000-B7FF
		U10	B800-BFFF
4:13	*5:12	U9	C000-C7FF
		U10	C800-CFFF
	6:11	U9	D000-D7FF
		U10	D800-DFFF
	7:10	U9	E000-E7FF
		U10	E800-EFFF
	8:9	U9	F000-F7FF
		U10	F800-FFFF

*Preprinted link connections.

Table V - Baud Rate Selection Chart

Switch S1				Output Rate
4	3	2	1	Baud*
C	C	C	C	19200
C	C	O	C	50
C	C	O	O	75
C	O	C	C	134.5
C	O	C	O	200
C	O	O	C	600
C	O	O	O	2400
O	C	C	C	9600
O	C	C	O	4800
O	C	O	C	1800
O	C	O	O	1200
O	O	C	C	2400
O	O	C	O	300
O	O	O	C	150
O	O	O	O	110

*Actual input to UART is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.
O=Open; C=Closed.

data bit DB0 is used as a group select, the group number $(0000\ 0001)_2$ is transmitted by the 61 output instruction to select the UART. The CDP18S610 comes with the link preprinted for group 1. The user also has the option of using data bit DB1 or group number $(0000\ 0010)_2$ for selecting the UART. When the UART is selected, the I/O instructions 62, 63, 6A, and 6B are reserved for use in utility programs UT61 for operating the UART. When the CDP18S610 is used with Microboard Control and Display Module CDP18S640A1, which contains the utility program UT61, the UART must be linked for group 1, and the RAM and ROM on the CDP18S610 must be placed at a new location to avoid the UT61 and RAM on the CDP18S640A1.

Table VI - UART Linking Arrangements

UART Group Select
Group 1 (01_{16}): LK1 2:9 Closed; LK1 1:10 Open Group 2 (02_{16}): LK1 2:9 Open; LK1 1:10 Closed
SDI to EF4-N
LK1 6:5 Closed
UART INT-N to CPU INT-N and EF3
LK1 3:8 Closed; LK1 4:7 Closed

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Table VII - List of Links and Their Functions

LK1	
1:10	Select UART - Group 02_{16}
*2:9	Select UART - Group 01_{16}
3:8	UART Interrupt Line to CPU Interrupt
*4:7	UART Interrupt Line to EF3
*5:6	Serial Data-In Line to EF4
LK2	
*A:B	EIA Receiver Operation
LK3	
*1:14	ROM CDP1834/2758 Operation
2:13	ROM 2716 Operation
3:12	1.2288 MHz CPU Frequency
4:11	0.6144 MHz CPU Frequency
5:10	0.3072 MHz CPU Frequency
§6:9	4.9152 MHz CPU Frequency
*7:8	2.4576 MHz CPU Frequency
LK4	
*1:16	ROM Decoding
2:15	ROM Decoding
3:14	Permanent Connection
4:13	ROM Decoding
*5:12	ROM Decoding
6:11	ROM Decoding
7:10	RAM Decoding
*8:9	RAM Decoding

LK5		LK6	
1:16	RAM Decoding	1:16	ROM Decoding
2:15	RAM Decoding	2:15	ROM Decoding
*3:14	RAM Decoding	*3:14	ROM Decoding
4:13	RAM Decoding	4:13	ROM Decoding
*5:12	RAM Decoding	*5:12	ROM Decoding
6:11	RAM Decoding	6:11	ROM Decoding
7:10	RAM Decoding	7:10	ROM Decoding
8:9	RAM Decoding	8:9	ROM Decoding

LK7	
A:B	Inhibit ROM
LK8	
*1:12	RUN U
2:11	RUN U if installed in CDP18S005 or CDP18S007
3:10	Not Used
4:9	Not Used
*5:8	Clock Frequency Out
*6:7	+5 V to CDP1805CE V_{DD}
LK9	
*A:B	EF4 to Backplane
*C:D	+12 V/+15 V
LK11	
A:B	PWR-ON RESET
LK12	
*1:5	$\overline{\text{CLEAR}}$
*2:3	$\overline{\text{WAIT}}$
5:6	Not Used
2.4	Not Used

*Preprinted links.
§Not applicable to CDP18S610.

Power-On Reset

An RC integrator (R2 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U23) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU. The CPU initializes and starts processing at location 0000 provided the WAIT line is not asserted.

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 using transmission gates, three-state, or open-collector devices.

To enable the power-on reset, install a jumper in LK11, A:B.

Installation in the COSMAC Development Systems CDP18S005 (II) and CDP18S007 (III)

Replacement of the CDS CPU Module CDP18S102 or CDP18S102V1 with the RCA COSMAC Microboard Computer CDP18S610 requires some link changes on the CDP18S610. These changes are:

LK9—Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter), do not install A:D.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut link LK1 so that when it is re-installed, no conflict

results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK8—RNU to start ROM's at address 8000. If there is ROM at 8000 containing a utility program, connect a wire jumper between 11 and 2 on link LK8 and cut link between 12 and 1 on link LK8. Then, add a wire to the CDS backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after the RESET RUN U switches are pressed.

Power—Add a wire from location 12 pin 11 to location 14 pin 11 to provide −5 volts. This connection is needed only for the RS232C serial interface, if required.

Memory Address Links—The desired memory addresses should be set up according to the memory maps of Tables I through IV. Care should be taken that the CDS memories are not assigned to overlap the assignment of the CDP18S610 Microboard Computer.

Table VIII - Pin Terminals and Signals for the RCA Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

92CS-34444

Table IX - Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

Connector Matching Cable - Available Separately

CDP18S516 - EIA Terminal Interface Cable

Fits connector J2; 15 feet long; has 25-pin delta and mating male connectors for EIA RS232C Terminal.

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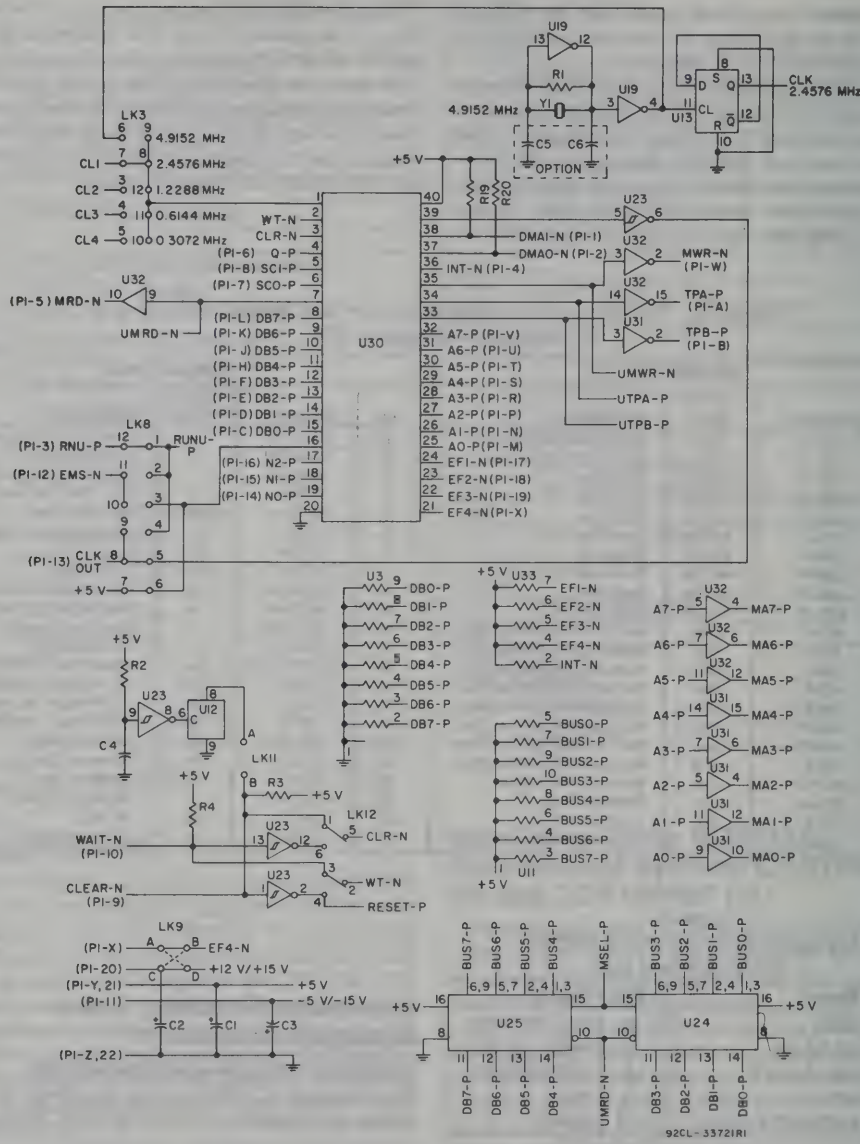

Fig. 4 - Microboard Computer CDP18S610 logic and circuit diagram - microprocessor and clock portion.

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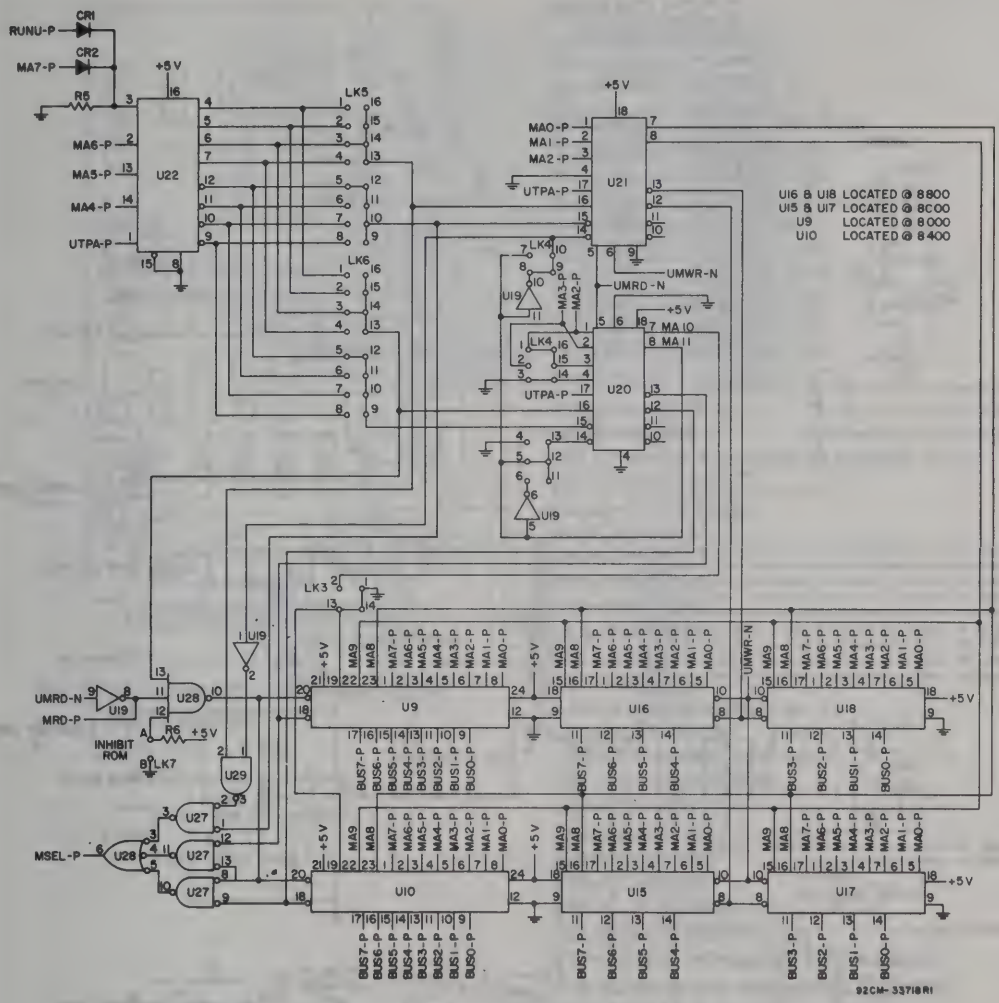


Fig. 5 - Microboard Computer CDP18S610 logic and circuit diagram - memory portion.

CDP18S610

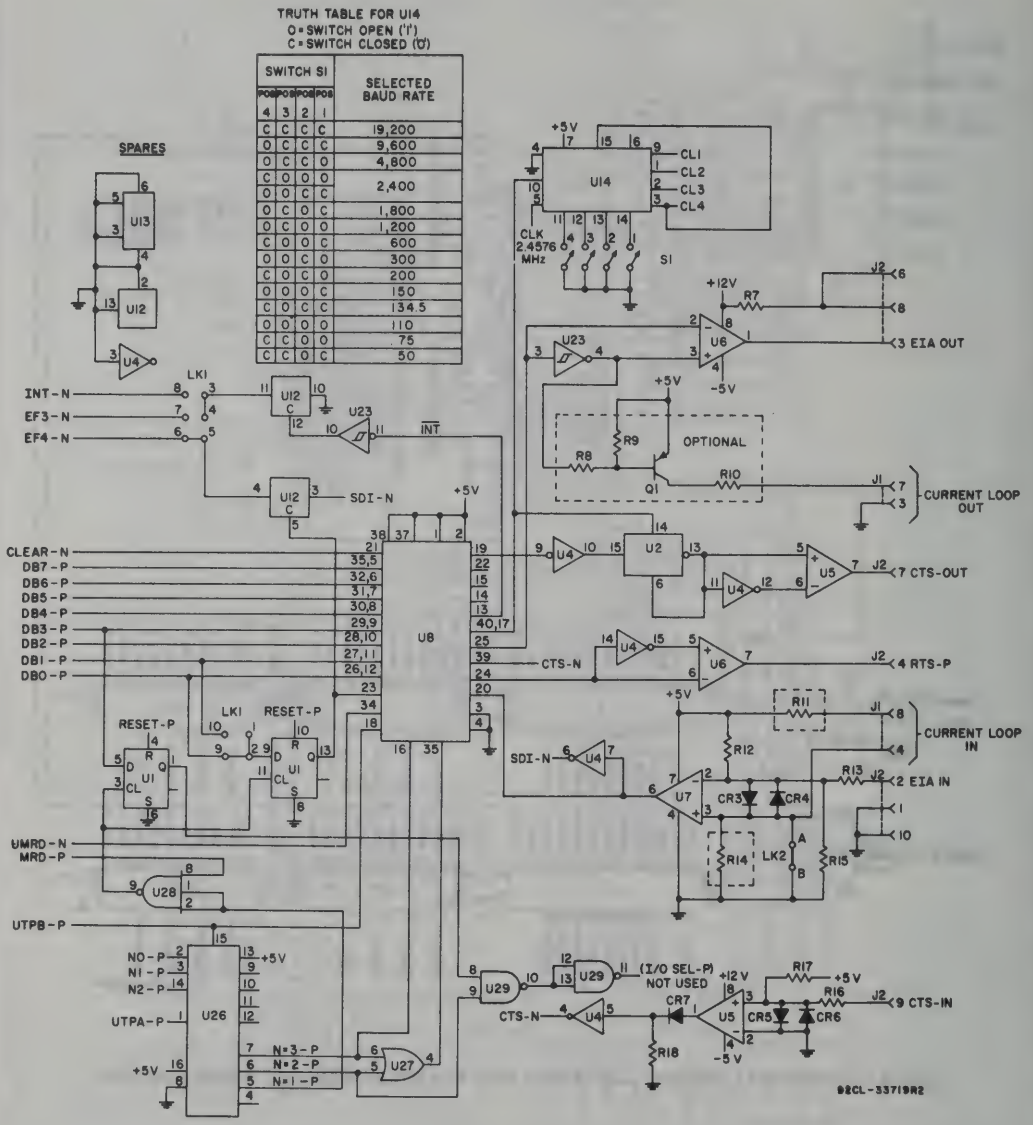


Fig. 6 - Microboard Computer CDP18S610 logic and circuit diagram - I/O portion.

CDP18S610

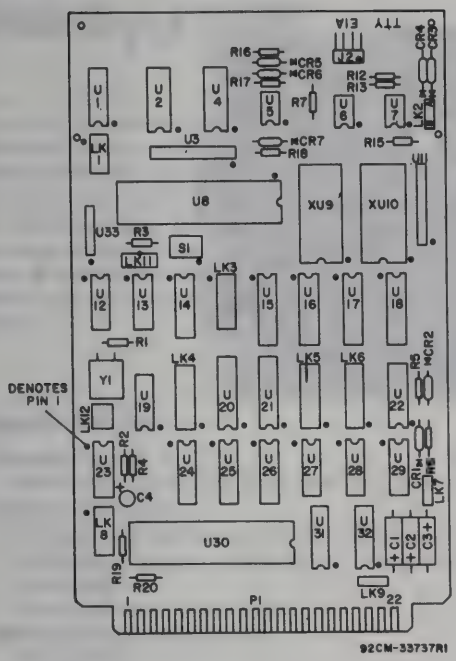
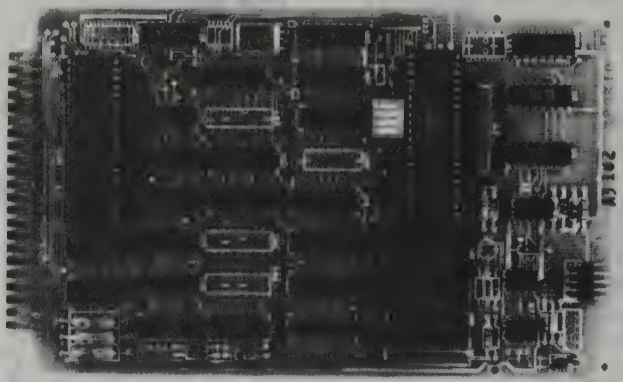


Fig. 7 - Microboard Computer CDP18S610 layout diagram.

Parts List

C1-C3=15 μF, 50 V
C4=1.5 μF, 25 V
CR1-CR7=1N270
J2=connector, right angle, 10 pin
R1=22 megohms, 0.25 W, 5%
R2=100 kilohms, 0.25 W, 5%
R3-R6,R19,R20=22 kilohms, 0.25 W, 5%
R7=3 kilohms, 0.25 W, 5%
R12=11 kilohms, 0.25 W, 5%
R13,R16=4.3 kilohms, 0.25 W, 5%
R15=1000 ohms, 0.25 W, 5%
R17=47 kilohms, 0.25 W, 5%
R18=10 kilohms, 0.25 W, 5%
S1=4-rocker DIP switch
U1=CD4013BE
U2=CD4017BE
U3,U11=resistor network, 22 kilohms, 10 pin
U4=CD4049UBE
U5,U6=CA3240AE
U7=CA3160AE
U8=CDP1854CE
U12=CD4066BE
U13=F34013PC
U14=F34702PC
U15-U18=MWS5114
U19=F34069PC
U20,U21=CDP1866CE
U22=CDP1858CE
U23=CD40106BE
U24,U25=CDP1856CE
U26=CDP1853CE
U27=CD4071BE
U28=CD4023BE
U29=CD4011BE
U30=CDP1805CE
U31,U32=CD4050BE
U33=resistor network, 22 kilohms, 6 pin
XU9,XU10=24-pin, low-profile, IC socket
Y1=4.9152 MHz, crystal

CDP18S610



CDP18S620

RCA COSMAC Microboard 4-Kilobyte RAM

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 is a static read-write memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 4-kilobyte block in the 64-kilobyte memory space. A four-rocker DIP switch is provided to set the binary value of the specific 4-kilobyte block to be occupied.

Specifications

Memory Capacity
4096 bytes (32 CMOS static RAM's 256 x 4).

Memory Addressing
Occupies any contiguous 4-kilobyte block on any 4-kilobyte boundary within the 64-kilobyte address space.
Switch-selectable block address.

Operating Temperature Range
0°C to 70°C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm).
Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
+5 volts at 4 milliamperes typical operating.

Connector
System interface: Edge fingers, 44 pins on 0.156-inch centers.

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with COSMAC Development Systems
- Compatible with Micromonitor CDP18S030 expansion connector
- High noise immunity
- Flexible address assignment
- Fully buffered
- Simple system interface
- Temperature range - 0°C to 70°C
- Expandable by use of COSMAC Microboard Universal Backplane

Bus Interface Signals (Connector P1)

The RCA Microboard 4-Kilobyte RAM makes use of the following Microboard bus interface signals.

A7 through A0 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM chip for the low-address byte, which becomes stable after TPA.

Bits 3 through 0 are latched in a CDP1858 4-bit Latch with Decode at TPA trailing edge. Bits 0 and 1 are decoded into four chip-enable lines called CE0-P through CE3-P. Bits 2 and 3 are decoded into four chip-enable lines called RE0-N

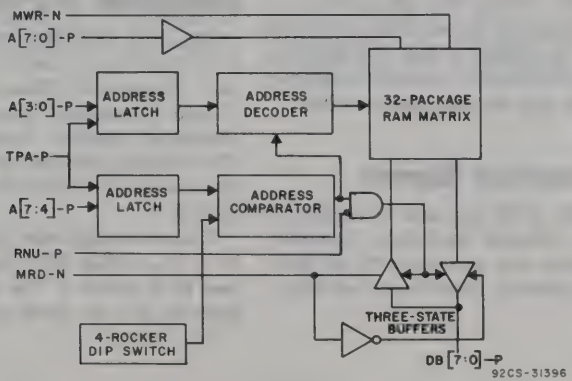


Fig. 1 - Block diagram of RCA COSMAC Microboard 4-Kilobyte RAM.

CDP18S620

through RE3-N. These eight lines are wired to CE2 and $\overline{CE1}$, respectively, on the RAM chips in a matrix form, and any combination of bits 3 through 0 will uniquely select the proper two RAM chips.

Bits 7 through 4 are latched into a CDP1867 4-bit Latch on the TPA trailing edge. These bits are compared with the setting of the four DIP switch rockers. When they are equal, an enable is generated which enables the CDP1858 decoder for bits 3 through 0 mentioned above and the data bus three-state buffers.

DB7 through DB0 - These **Data Bus** lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a match between the four high-address bits and the four DIP switch rockers. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted **to** the Microboard interface bus; when MRD is false, data bits are transmitted **from** the Microboard interface bus.

$\overline{MRD}$ - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the output control on each RAM chip.

$\overline{MWR}$ - Memory Write. This signal is buffered and wired to each RAM chip. It is the write command.

TPA - Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1858 and CDP1867 latches. Latching takes place at the TPA trailing edge.

RNU - Run Utility. This signal, through link LK2, inhibits the board ENABLE signal, thereby eliminating memory access. The link need not be installed if not required. Its purpose is to inhibit the board when its address is **0000** (DIP switches open) and a RUN UTILITY switch is causing the system to start at address 8000 instead of 0000.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal	Pin	Signal
A	TPA-P *	1	DMAI-N
B	TPB-P	2	DMAO-N
C	DB0-P *	3	RNU-P *
D	DB1-P *	4	INT-N
E	DB2-P *	5	MRD-N *
F	DB3-P *	6	Q-P
H	DB4-P *	7	SC0-P
J	DB5-P *	8	SC1-P
K	DB6-P *	9	CLEAR-N
L	DB7-P *	10	WAIT-N
M	A0-P *	11	−5 V/−15 V
N	A1-P *	12	SPARE
P	A2-P *	13	CLOCK OUT
R	A3-P *	14	N0-P
S	A4-P *	15	N1-P
T	A5-P *	16	N2-P
U	A6-P *	17	EF1-N
V	A7-P *	18	EF2-N
W	MWR-N*	19	EF3-N
X	EF4-N	20	+12 V/+15 V
Y	+5 V *	21	+5 V *
Z	GND *	22	GND *

*Signals used on RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

Installation in a Microboard System

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). No link changes are required. If the system has a RUN UTILITY switch and the DIP switch rockers are all open, the user should make certain that link LK2 pins A and B are shorted.

The desired high-order four address bits should be set in the four-rocker DIP switch (UA9). The least significant bit is rocker 1. The open position of the rocker generates a 0; the closed position generates a 1.

Installation in the COSMAC Development System CDP18S005

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 may be installed in the CDS II in any memory slot 1 through 8. No Bank Select wiring is required on the backplane. The binary address of the desired 4-kilobyte block should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect A and B of link LK1.

For the RNU signal, the user should make certain that A and B of link LK2 are connected, if the board is to reside at address 0000. On the CDS II backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

Installation in the Micromonitor CDP18S030

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. The binary number of the desired 4-kilobyte block address should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1). Link LK1 must be arranged as follows:

A to B - SHORTED
C to D - OPEN (Cut preprinted LINK)
E to F - SHORTED

When the CDP18S620 is used in this manner, it will respond only to the block address set into the DIP switch rockers. The memory disable output from the Micromonitor CDP18S030 will be inactive only when the system under test generates a memory address that agrees with the value set into the DIP switch rockers even though the EXM bit is true. This arrangement allows for the substitution of a given 4-kilobyte block of user memory and enables the remainder of user memory space to operate normally.

Physical Address Map

The physical address map given in Table II may be used to identify the board location of a memory device as a function of its address. Because the device organization is 256 x 4, two devices are involved with any byte of data. Table II provides the two device locations for each address, one containing the high-order half byte and the other the low-order half byte.

Table II - Physical Address Map of 32-Package RAM Matrix

	Memory Location	
Hex Address	High Half-Byte	Low Half-Byte
X0XX	UD1	UE1
X1XX	UD2	UE2
X2XX	UD3	UE3
X3XX	UD4	UE4
X4XX	UD5	UE5
X5XX	UD6	UE6
X6XX	UD7	UE7
X7XX	UD8	UE8
X8XX	UB1	UC1
X9XX	UB2	UC2
XAXX	UB3	UC3
XBXX	UB4	UC4
XCXX	UB5	UC5
XDXX	UB6	UC6
XEXX	UB7	UC7
XFXX	UB8	UC8

X = DON'T CARE, except that the most significant hex digit matches the DIP switch setting. If it does not, the board is not being addressed.

CDP18S620

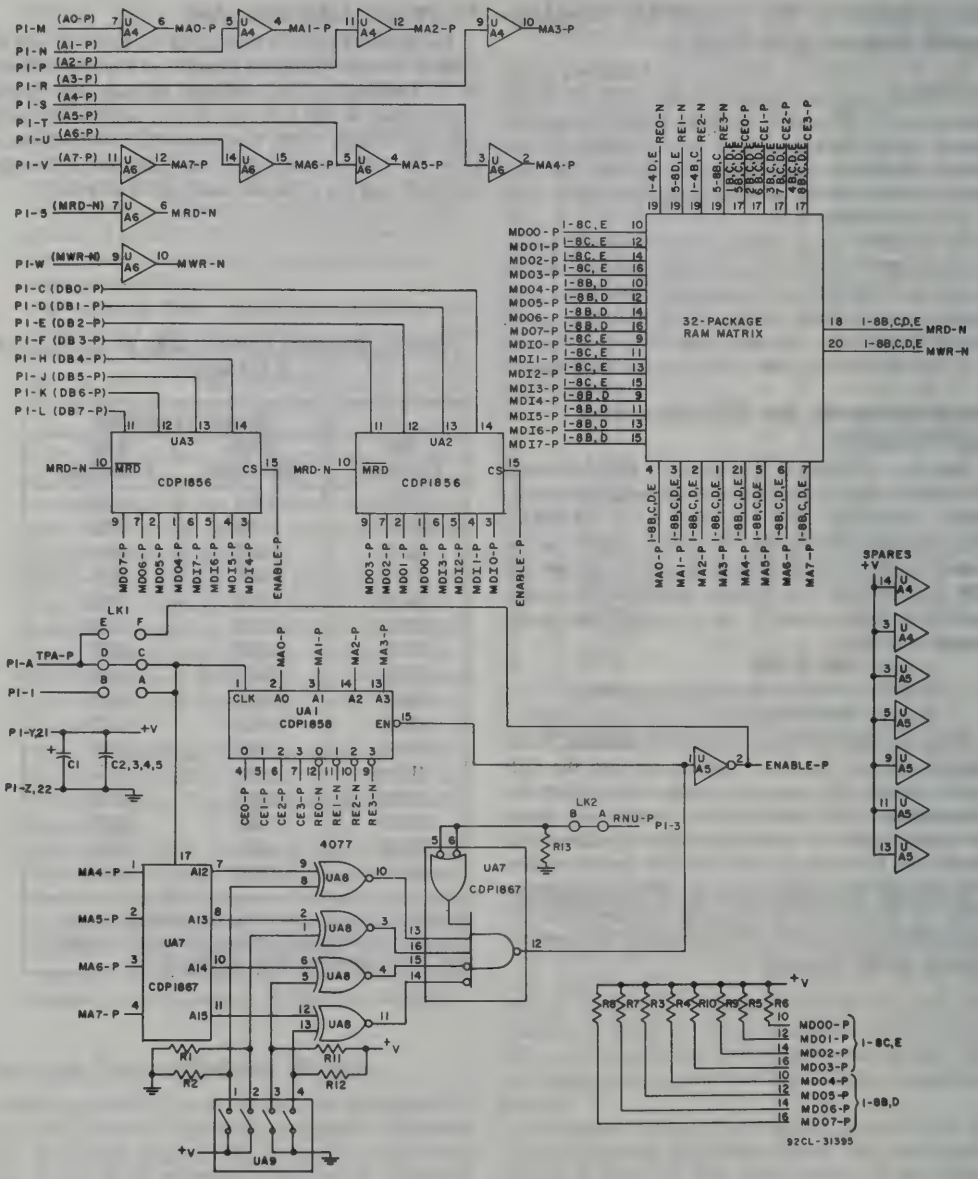


Fig. 2 - Logic diagram for RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

CDP18S620

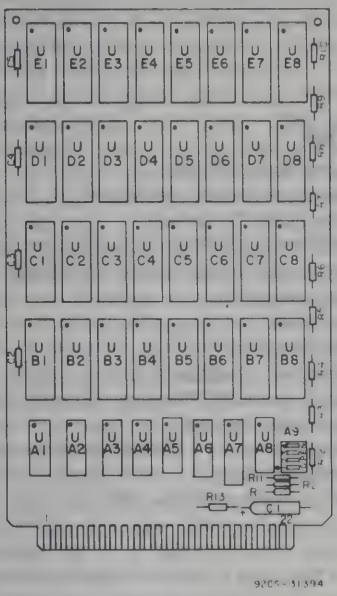
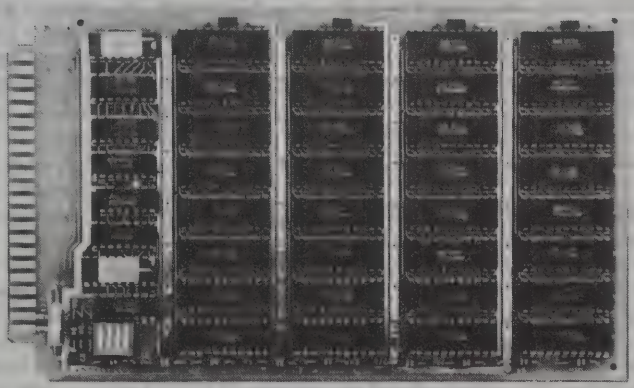


Fig. 3 - Layout diagram of RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

Parts List

C1 = 15 μF, 20 V
C2 – C5 = 0.1 μF, 50 V
R1 – R13 = 22 kilohms, 0.25 W
UA1 = CDP1858CE
UA2, UA3 = CDP1856CE
UA4, UA6 = CD4050BE
UA5 = CD4069BE
UA7 = CDP1867CE
UA8 = CD4077BE
UA9 = 4-rocker DIP switch
UB1-UB8, UC1-UC8, UD1-UD8, UE1-UE8 } CDP1822E or MWS5101EL-3



CDP18S621
RCA COSMAC Microboard 16-Kilobyte RAM

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 is a static read-write memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 16-kilobyte block in the 64-kilobyte memory space. A two-rocker DIP switch is provided to set the binary value of the specific 16-kilobyte block to be occupied.

Specifications

Memory Capacity

16192 bytes (32 CMOS static RAM's 1048 x 4; MWS5114)

Memory Addressing

Occupies any contiguous 16-kilobyte block on any 16-kilobyte boundary within the 64-kilobyte address space.

Switch-selectable block address.

Operating Temperature Range

0°C to 70°C

Dimensions

4.5 inches x 7.5 inches (114.3 mm x 190.5 mm). Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

+5 volts at 6 milliamperes typical, operating at 2-MHz system clock.

Connector

System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small size (4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- Compatible with Micromonitor CDP18S030 expansion connector
- Fully buffered
- High noise immunity
- Flexible address assignment
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range - 0°C to 70°C

Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard 16-Kilobyte RAM makes use of the following Microboard bus interface signals.

A7 through A0 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM chip for the low-address byte, which becomes stable after TPA.

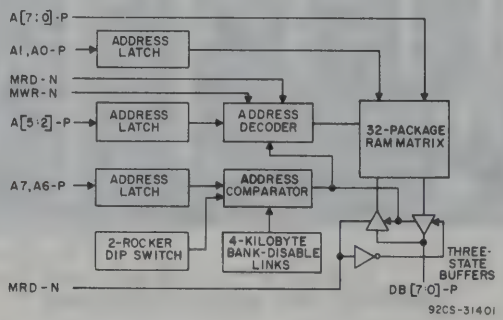


Fig. 1 - Block diagram of RCA COSMAC Microboard 16-Kilobyte RAM.

Bits 1 and 0 are latched in a CDP1866 (U1B) latch-decoder at TPA trailing edge. The output of these latches are wired to each memory chip, providing A9 and A8 for on-chip decoding.

Bits 3 and 2 are latched into four CDP1866 latch-decoders (U1B, U2B, U6B, U7B) in parallel, forming A11 and A10, and decoded into four sets of four chip-enable lines. These lines are wired to four 4-kilobyte blocks of memory chips as chip-enables.

Bits 5 and 4 are latched into a CDP1866 (U2B), forming A13 and A12, and are used to condition the four decoders so that only one 4-kilobyte block is addressed at any time.

Bits 7 and 6 are latched into a CDP1866 (U6B) forming A15 and A14. These bits are compared with the setting of the 2 DIP switch rockers. When there is a match, the four decoders and the data buffers are enabled.

DB7 through DB0 - These Data Bus lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a match between the two high-address bits and the two DIP switch rockers. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted to the Microboard interface bus; when MRD is false, data bits are transmitted from the Microboard interface bus.

$\overline{\text{MRD}}$ - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the chip-select decoders.

$\overline{\text{MWR}}$ - Memory Write. This signal is buffered. It conditions each RAM chip and the chip-select decoders. It is the write command.

TPA - Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866 latches. Latching takes place at the TPA trailing edge.

RNU - Run Utility. This signal, through link LK2A, pins 4 and 13, inhibits the board ENABLE signal, thereby eliminating memory access. The link may be cut if not required. Its purpose is to inhibit the board when its address is 0000 (DIP switches open) and a RUN UTILITY switch is causing the system to start at address 8000 instead of 0000.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal	Pin	Signal
A	TPA-P *	1	DMAI-N
B	TPB-P	2	DMAO-N
C	DB0-P *	3	RNU-P *
D	DB1-P *	4	INT-N
E	DB2-P *	5	MRD-N *
F	DB3-P *	6	Q-P
H	DB4-P *	7	SC0-P
J	DB5-P *	8	SC1-P
K	DB6-P *	9	CLEAR-N
L	DB7-P *	10	WAIT-N
M	A0-P *	11	−5 V/−15 V
N	A1-P *	12	SPARE
P	A2-P *	13	CLOCK OUT
R	A3-P *	14	N0-P
S	A4-P *	15	N1-P
T	A5-P *	16	N2-P
U	A6-P *	17	EF1-N
V	A7-P *	18	EF2-N
W	MWR-N*	19	EF3-N
X	EF4-N	20	+12 V/+15 V
Y	+5 V *	21	+5 V *
Z	GND *	22	GND *

*Signals used on RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621.

Installation in a Microboard System

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). No link changes are required.

The desired high-order two address bits should be set in the two-rocker DIP switch S1. The least significant bit is rocker 1. The open position of the rocker generates a 0; the closed position generates a 1.

CDP18S621

Installation in the COSMAC Development System CDP18S005

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 may be installed in the CDS II in any memory slot 1 through 8. No Bank Select wiring is required on the backplane. The binary address of the 16-kilobyte block should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect pins 1 and 16 of link LK2A.

For the RNU signal, a connection is preprinted between pins 4 and 13 of link LK2A. On the CDS II backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

Installation in the Micromonitor CDP18S030

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. The binary number of the desired 16-kilobyte block address should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1). Connect link LK2A as follows:

1 to 16 - SHORTED
2 to 15 - OPEN (Cut preprinted link)
3 to 14 - SHORTED

When the CDP18S621 is used in this manner, it will respond only to the block address set into the DIP switch rockers. The memory disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the value set into the DIP switch rockers even though the EXM bit is true. This arrangement allows for the substitution of a given 16-kilobyte block of user memory and enables the remainder of user memory space to operate normally.

Installation as a 4-, 8-, or 12-Kilobyte RAM

The CDP18S621 may be configured as a 4-, 8-, or 12-kilobyte RAM when, for example, ROM is substituted for RAM in a developmental cycle. Any 4-kilobyte block may be disabled by the cutting of one link.

The disabling links for each 4-kilobyte block of memory, as defined in the physical address map given in Table II, are as follows

Memory Block To Be Disabled	Pins of Link LK2A To Be Cut
First 4 kilobytes	5 to 12
Second 4 kilobytes	6 to 11
Third 4 kilobytes	7 to 10
Fourth 4 kilobytes	8 to 9

The result of cutting one or more of these links is the creation of 4-kilobyte holes in the 16-kilobyte space normally occupied by the board. Other memories may then occupy these holes without conflict.

Physical Address Map

The physical address map given in Table II may be used to identify the board location of a memory device as a function of its address. Because the device organization is 1024 x 4, two devices are involved with any byte of data. Table II provides the two device locations for each address, one containing the high-order half byte and the other the low-order half byte.

Table II - Physical Address Map of 32-Package RAM Matrix

Binary Value of High Address Byte		Memory Location: High Half-Byte	Memory Location: Low Half-Byte
XX00	00XX	U2E	U2C
XX00	01XX	U2F	U2D
XX00	10XX	U1E	U1C
XX00	11XX	U1F	U1D
XX01	00XX	U4E	U4C
XX01	01XX	U4F	U4D
XX01	10XX	U3E	U3C
XX01	11XX	U3F	U3D
XX10	00XX	U6E	U6C
XX10	01XX	U6F	U6D
XX10	10XX	U5E	U5C
XX10	11XX	U5F	U5D
XX11	00XX	U8E	U8C
XX11	01XX	U8F	U8D
XX11	10XX	U7E	U7C
XX11	11XX	U7F	U7D

X = DON'T CARE, except that the two most significant bits match the DIP switch setting. If they do not, the board is not being addressed.

CDP18S621

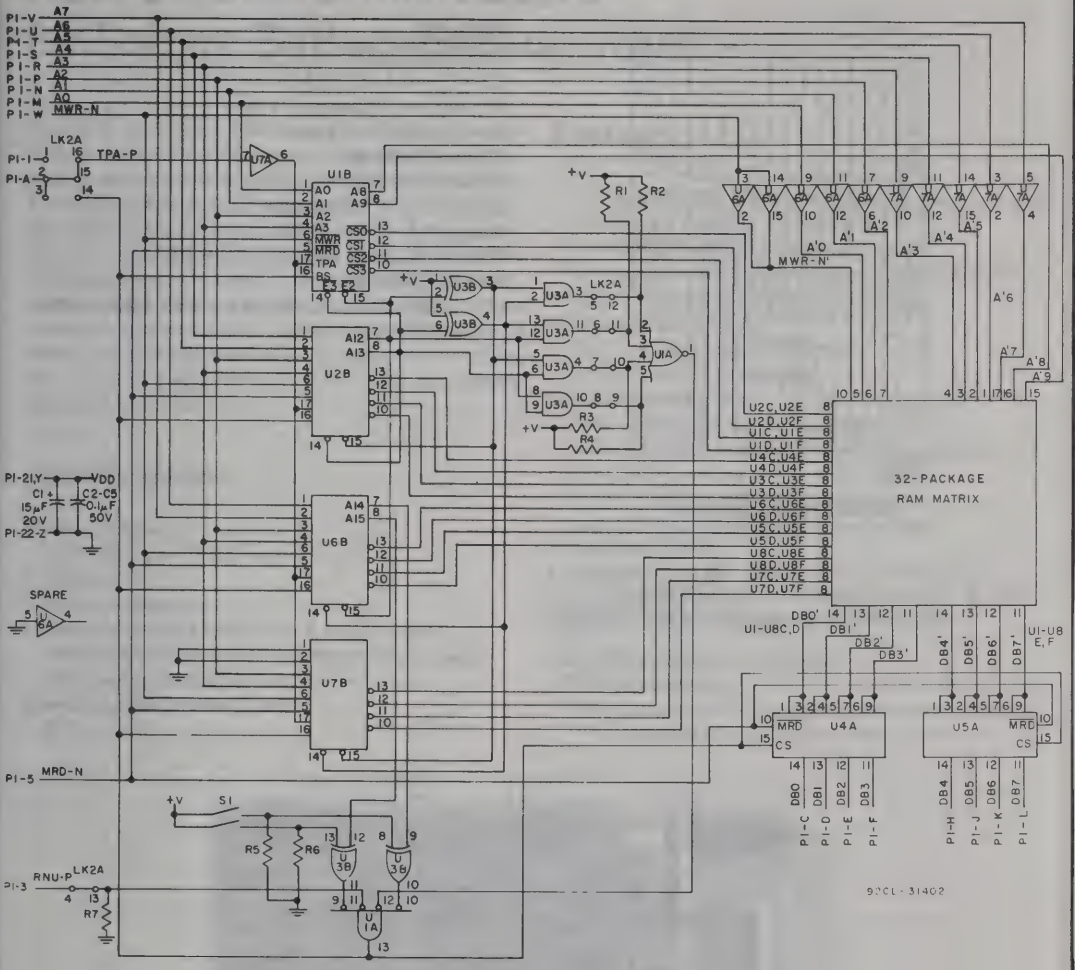
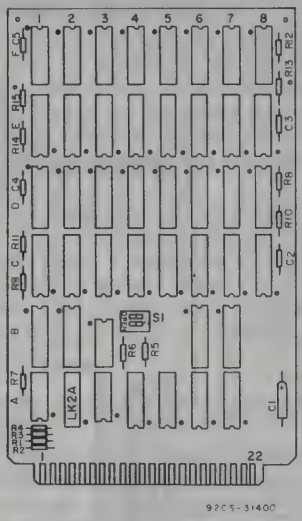


Fig. 2 - Logic diagram for RCA COSMAC Microboard 16-kilobyte RAM CDP18S621.

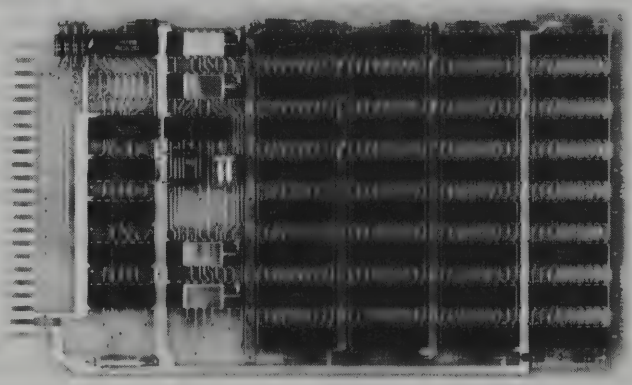
CDP18S621



Parts List

C1 = 15 μF, 20 V
C2 – C5 = 0.1 μF, 50 V
R1 – R15 = 22 kilohms, ¼ W
S1 = 2-rocker DIP switch
U1A = CD4002BE
U3A = CD4081BE
U4A, U5A = CDP1856CE
U6A, U7A = CD4050BE
U1B, U2B, U6B, U7B = CDP1866CE
U3B = CD4070BE
U1C – U8C, U1D – U8D, U1E – U8E, U1F – U8F = MWS5114E-5

Fig. 3 - Layout diagram of RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621.



CDP18S622

RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 is a static read-write memory module with on-board address latches and decoders. The address and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 8-kilobyte block within the 64-kilobyte memory space. A three-rocker DIP switch defines the 8-kilobyte block to be occupied. Three 180-mAh nickel-cadmium batteries provide backup power for data retention when system power is down. The board is also prewired for use with an optional regulated power supply.

Specifications

Memory Capacity
8192 bytes (16 CMOS static RAM's 1024 x 4)

Memory Addressing
Occupies any 8-kilobyte block on 8-kilobyte boundaries within the 64-kilobyte address space. Switch-programmable block addressing.

Operating-Temperature Range
0°C to 70°C

Features:

- Low-power static CMOS (600 μA typ. battery drain)
- Small board size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with COSMAC Development Systems
- Fits Micromonitor (CDP18S030) memory expansion connector
- High noise immunity (1.5 V typ.)
- Flexible address assignment
- Fully buffered
- Power supply option for ac operation
- Battery-backup memory (96-hr. data retention)
- 0 to 70°C operating-temperature range
- 44-pin system interface
- Integral battery option can power entire computer system
- Expandable by use of COSMAC Microboard Universal Backplane
- Memory protect switch

Power Requirements - Standby

Without batteries:	+5 V at 600 μA, typ.
With batteries 10% charged:	+5 V at 145 mA, typ.
With batteries 90% charged:	+5 V at 4.5 mA, typ.

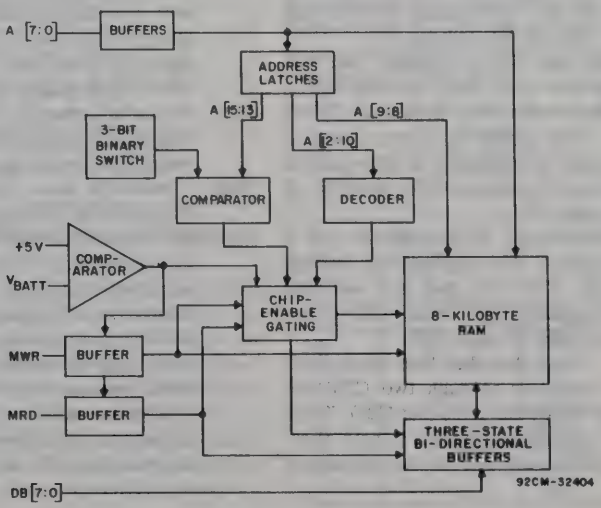


Fig. 1 - RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 block diagram.

CDP18S622

Optional Power Supply - Regulated
Input: 8 to 20 V dc or 12.6 V ac at 1.5 A, max. (diode bridge installed)
Output: Regulated - 4.92 to 5.62 V dc at 500 mA
Battery Supply
3 batteries: 3.6 to 4.35 V at 90 mAh
With optional 4th battery: 4.8 to 5.8 V at 90 mAh
Connector
System interface: Edge fingers, 44 pins on 0.156-inch centers
Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum
Data Retention
With 3 batteries, fully charged: 96 hours, min.

Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM makes use of the following Microboard bus interface signals.

A0 through A7 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM and address decoder. The address decoders latch the high-address byte on the trailing edge of TPA. The low-address byte becomes stable after TPA.

Address Bits A0 and A1 are latched into a CDP1866 (U22 and U23) at the trailing edge of TPA and generate output Address Bits A8 and A9.

Address Bits A2 and A3 are latched into two CDP1866's (U22 and U23). Each of these latches generate four chip-enable lines designated CS1-N through CS8-N. Each enable line is then wired to the appropriate pair of MWS5114 RAM's (1024 x 4). A12 = 1 enables CS5 through CS8, and A12 = 0 enables CS1 through CS4.

Address Bits A4 through A7 are latched into a CDP1867 (U21) latch at TPA trailing edge, forming A12 through A15. A15, A14, and A13 are compared to the setting of the three-rocker DIP switch and used to enable CS1 through CS8.

DB0 through DB7 - These **Data Bus** lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators (U26 and U27). These devices are in a high-impedance state in both directions until an enable is generated by the comparison of A15, A14, and A13 with the setting of the three-rocker DIP switch and POWER ENABLE (PE). The direction is determined by the READ-N signal. When READ-N is true, data bits are transmitted to the Microboard interface bus; when READ-N is false, data bits are transmitted from the Microboard bus.

$\overline{\text{MRD}}$ - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered and gated with PE-N (Power Enable) generating a signal READ-N. READ-N conditions the data bus interface buffers and the chip-enable (CS1-N through CS8-N) decoders.

$\overline{\text{MWR}}$ - Memory Write. When true, MWR dictates a write command. This signal is buffered and gated with PE-N (Power Enable) generating a signal WE-N. This signal enables the chip-enable decoders and conditions all the RAM's into the WRITE mode.

TPA - Timing Pulse A. This signal is buffered and used to latch the high-order address bits into the CDP1867 and CDP1866 latches. Latching takes place at the TPA trailing edge.

PE - Power Enable. The signal PE-N is generated by the CA3078 Micropower Operational Amplifier. The supply voltage for the amplifier is obtained directly from the battery supply, thus enabling proper operation without the application of external power. The battery voltage V_B and the external supply voltage V_{DD} are both sampled through a voltage divider network to the inputs of the CA3078. If a power failure is sensed, the PE-N signal is driven into the off state (high), thus isolating the data bus, chip select, memory write, and memory read functions from the Microboard interface bus while V_B allows data retention in RAM.

POR - Power-On Reset. The signal POR is available, if required by the user, through link LK7 A and B to pin 17 on the Microboard Interface Connector (P1). After power up (V_{DD} on), the signal will momentarily remain high and then stabilize to a low state. The RC integrator (R1 and C4) and the Schmitt trigger (U3) lower the signal approximately 150 milliseconds after power turn on. Systems using the data retention feature must use a POR to avoid random-memory access at power-on time. Microboard computer modules also provide a POR,

generating CLEAR-N at P1-9. Link LK7 A and B should not be used in a Microboard system, only in other applications.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Microboard Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622.

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal
A	TPA-P	*	1	DMAI-N
B	TPB-P		2	DMAO-N
C	DB0-P	*	3	RNU-P
D	DB1-P	*	4	INT-N
E	DB2-P	*	5	MRD-N
F	DB3-P	*	6	Q-P
H	DB4-P	*	7	SC0-P
J	DB5-P	*	8	SC1-P
K	DB6-P	*	9	CLEAR-N
L	DB7-P	*	10	WAIT-N
M	A0-P	*	11	−5 V/−15 V
N	A1-P	*	12	SPARE
P	A2-P	*	13	CLOCK OUT
R	A3-P	*	14	N0-P
S	A4-P	*	15	N1-P
T	A5-P	*	16	N2-P
U	A6-P	*	17	EF1-N†
V	A7-P	*	18	EF2-N
W	MWR-N	*	19	EF3-N
X	EF4-N		20	+12 V/+15 V
Y	+5 V	*	21	+5 V
Z	GND	*	22	GND

*Signals used on RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622.
†Power reset option.

Installation in a Microboard System

The RCA COSMAC 8-Kilobyte Battery-Backup RAM CDP18S622 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). The user must set the position of the three-rocker DIP switch to determine the module address. The rocker labeled 1 is the least significant bit; rocker open = 0; rocker closed = 1. Table II gives the hexadecimal address for the various settings of the three-rocker DIP switch.

Installation in the COSMAC Development System CDP18S005 or CDP18S007

The RCA COSMAC 8-Kilobyte Battery-Backup RAM CDP18S622 may be installed in the CDS in any memory slot 1 through 8. Bank Select wiring is not required on the backplane. The three-rocker DIP switch should be set for the desired address. Refer to Table II for the switch setting. Additional changes are required for the TPA, RNU, and POR (clear) signals to assure proper operation of the CDS.

For the TPA signal, on LK5 of the CDP18S622 disconnect A and B, and connect C and B. As an alternative, on the backplane of the CDS pin 1 can be wired to pin A in the slot selected for the CDP18S622.

For the RNU signal, if the CDP18S622 is to reside at address 0000_{16}, pin 3 of any memory slot 1 through 9 of the CDS should be wired to pin D of slot location 10 of the CDS. This signal, RNU-P, starts utility software at location 8000_{16}. Its function on the CDP18S622 is to inhibit response while the utility program is being initiated.

For the POR signal, add a jumper between A and B of LK7 on the CDP18S622. On the CDS backplane, add a jumper between pin 11 of slot 25 and pin 17 of the slot selected for the CDP18S622. These connections will provide the necessary clear signal to the CPU after power is applied to the CDS. This signal must be provided so that the CPU will not inadvertently power up in the write mode and cause invalid data to be written to a programmed CDP18S622.

Table II—
Memory Addresses for Various Settings of Switch S2.

Switch Setting			Memory Addresses (hex)	
3	2	1	First	Last
0	0	0	0000	1FFF
0	0	1	2000	3FFF
0	1	0	4000	5FFF
0	1	1	6000	7FFF
1	0	0	8000	9FFF
1	0	1	A000	BFFF
1	1	0	C000	DFFF
1	1	1	E000	FFFF

CDP18S622

Installation in the Micromonitor CDP18S030

The RCA COSMAC 8-Kilobyte Battery-Backup RAM CDP18S622 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. For proper operation, LK5 must be modified to provide an "External Memory Deselect-N" signal for the Micromonitor. To make this modification, disconnect A and B on LK5 and connect A to D and B to C.

The memory address of the CDP18S622 can be located in any 8-kilobyte block in the 64-kilobyte memory space.

The memory-disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the setting of the three-rocker DIP switch, even though the EXM bit is true. This arrangement allows for the substitution of 8-kilobyte blocks of user memory within the 64-kilobyte memory space and enables the remainder of user memory space to operate normally.

Optional Power Supply

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 can be operated from a 12.6-volt ac power source by means of the regulated power supply option. The CDP18S622 printed-circuit board is prewired to accept the optional power-supply components listed in Table III. The power supply, a full-wave bridge rectifier with capacitive input filtering, delivers 17.8 volts dc at no load into a three-terminal positive-voltage regulator. The 5.26-volt dc output from the regulator (V_{REG}) is connected to link LK2.

To install the components listed in Table III, the user should refer to the Microboard layout diagram and the logic diagrams. The 12.6 volts (1 ampere) ac is applied to J1 and J2. The connections for link LK2 are given in Table IV for the four power-supply options.

Battery-Backup Memory Function

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 is supplied with three 180-mAh nickel-cadmium batteries capable of providing power to the control logic and RAM's during system power failures or other normal power-down situations. For operation of the CDP18S622 under battery power, the batteries must be charged for a period of 24 hours prior to use. With fully charged batteries, the data-retention capability is 96 hours under battery power. To disable the battery-backup feature of the CDP18S622, set switch S1 (Batt. Hold) to the off position. This switch disconnects the battery voltage ground connection.

Memory Protect Function

Switch S3 has been provided to prevent changing of the memory contents. When this switch is on, the signal WE is inhibited and, therefore, no writing can take place. No error indication is generated. In the memory-protected state, the CDP18S622 may be viewed as a ROM.

Table III - Components Required for Optional Regulated Power Supply

Component	Type	Quantity	Location	Suggested Supplier and Part No.
Capacitor	220 μF, 20 V dc	2	C2, C3	Sprague 137D227C7020F2
Diode	1N4001	4	CR6, CR7 CR8, CR9	RCA D1201F
Diode	1N270	1	CR5	—
Regulator	5 V, 3 pin	1	VR1	Fairchild 7805
Heat sink	—	1	H1	Aavid Eng. 5063B or Thermalloy 6070B
Heat sink compound	as required			
Hardware	screw #6-32, lock washer #6, hex nut #6-32			

Table IV - Connections for Link LK2

Function	Link Connections	
	Remove	Add
A. Power Microboard RAM CDP18S622 only from regulated supply - battery backup for Microboard RAM only	V_{DD} to V_{CC}	V_{REG} to V_{CC}
B. Power entire Microboard system from regulated supply - battery backup for entire system	V_{DD} to V_{CC}	V_{REG} to V_{CC} and V_{DD} to V_B
C. Power entire Microboard system from regulated supply - battery backup for Microboard RAM only	none	V_{REG} to V_{CC}
D. Power Microboard RAM from system V_{DD} - battery backup for entire system	V_{DD} to V_{CC}	V_{DD} to V_B

Optional Four-Battery Configuration

As shown in the layout diagram, the CDP18S622 provides for the addition of a fourth battery. With the additional battery, backup and operating power is available for the complete Microboard system. This feature assures proper Microboard system operation during power supply failures.

To operate a Microboard Computer System with the battery-backup feature, the following steps must be taken. First, check that all devices in the system can be operated at 6.1 volts dc, the normal operating voltage for the system. Then,

1. Remove link V_{DD} to V_{CC} from LK2.
2. Remove link A to B on LK3.
3. Remove system V_{DD} from Microboard Chassis backplane. (V_{DD} will not be used).
4. Install link from V_{DD} to V_B on LK2.
5. Install link from B to C on LK3.
6. Install 180-mAh AAA nickel-cadmium battery in location B4 (Caution: Be sure to observe correct polarity).
7. Connect an external 6.5-volt dc supply to V_{CC} on LK2. (Provides system V_{DD}.)

Physical Address Map (Unmodified Board)

The physical address map given in Table V may be used to identify the board location of any memory component by its logical address.

Applications

The type of application for the CDP18S622 in which the battery-backup feature is used to advantage includes the transfer of software or data from the RCA COSMAC Development System - CDP18S005 or CDP18S007 to a Microboard Computer System or the retention of data when the external power is down-during hardware changes or work stoppages.

Transport of Software or Data. The CDP18S622 can be used very effectively to transfer newly developed software from a development system to a prototyping system and to transfer test programs and data to remote systems when other means such as disk or tape are not available.

To transfer software or data, the CDP18S622 should be installed in the Development System as previously described (page 4) but with the following exceptions:

CDP18S622

Table V—Physical Address Map (Hexadecimal Location) for Unmodified RCA COSMAC Microboard RAM CDP18S622.

SWITCH SETTING →		000	001	010	011	100	101	110	111	HALF BYTE HIGH	HALF BYTE LOW
MEMORY ADDRESS	From	0000	2000	4000	6000	8000	A000	C000	E000	U16	U8
	To	03FF	23FF	43FF	63FF	83FF	A3FF	C3FF	E3FF		
	From	0400	2400	4400	6400	8400	A400	C400	E400	U15	U7
	To	07FF	27FF	47FF	67FF	87FF	A7FF	C7FF	E7FF		
	From	0800	2800	4800	6800	8800	A800	C800	E800	U14	U6
	To	0BFF	2BFF	4BFF	6BFF	8BFF	ABFF	CBFF	EBFF		
	From	0C00	2C00	4C00	6C00	8C00	AC00	CC00	EC00	U13	U5
	To	0FFF	2FFF	4FFF	6FFF	8FFF	AFFF	CFFF	EFFF		
	From	1000	3000	5000	7000	9000	B000	D000	F000	U12	U4
	To	13FF	33FF	53FF	73FF	93FF	B3FF	D3FF	F3FF		
	From	1400	3400	5400	7400	9400	B400	D400	F400	U11	U3
	To	17FF	37FF	57FF	77FF	97FF	B7FF	D7FF	F7FF		
	From	1800	3800	5800	7800	9800	B800	D800	F800	U10	U2
	To	1BFF	3BFF	5BFF	7BFF	9BFF	BBFF	DBFF	FBFF		
	From	1C00	3C00	5C00	7C00	9C00	BC00	DC00	FC00	U9	U1
	To	1FFF	3FFF	5FFF	7FFF	9FFF	BFFF	DFFF	FFFF		

1. Wire the TPA connection (pin 1 to pin A) on the backplane instead of on the CDP18S622.
2. Do not install the POR link.

The software or data should be developed and loaded into the CDP18S622 in the normal manner. Make sure the battery hold switch S1 on the CDP18S622 is in the ON position and the batteries are adequately charged. Then turn off the external power to the Development System. Remove the CDP18S622 and install it into the second system. Power up the system and the memory contents of the CDP18S622 will be available to it.

If the user so desires, the board address assignment may be changed by means of DIP switch S2 before the CDP18S622 is installed in the second system.

Data Retention. The ability to retain data in memory when the external power to a system is turned off during hardware changes or overnight or weekend down periods is a very useful development aid. With the CDP18S622, this data-retention capability can be used at any time. It is only necessary for the user to make sure that the batteries are charged and that the battery switch S1 is in the ON position.

CDP18S622

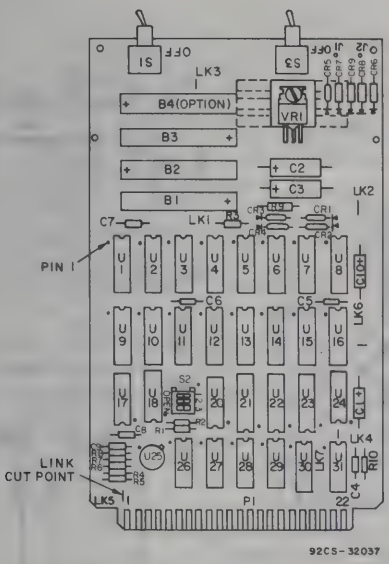
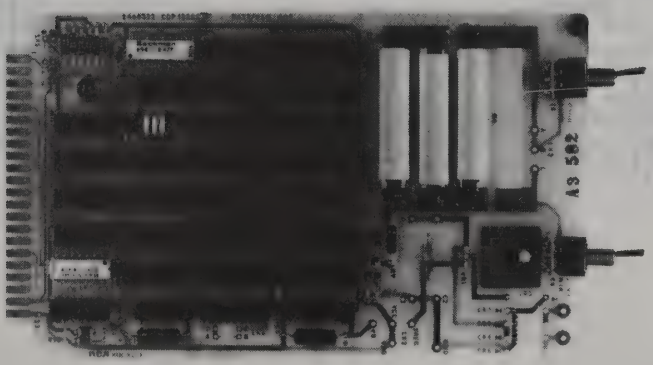


Fig. 2 - Layout diagram for RCA COSMAC Microboard Battery-Backup RAM CDP18S622. B4, VR1, CR5 - CR9, C2 and C3 are optional items not installed on board.

Parts List

B1 – B3 = nickel-cadmium, 180 mAh, AAA
*B4 = nickel-cadmium, 180 mAh, AAA (Panasonic NR-AAA-U)
C1, C10 = 15 μF, 50 V
*C2, C3 = 220 μF, 20 V (Sprague 137D227C7020F2)
C4 = 0.33 μF, 50 V
C5 – C8 = 0.1 μF, 50 V
C9 = 22 pF
CR1 – CR4 = 1N270
*CR5 = 1N270
*CR6 – CR9 = 1N4001 (RCA D1201F)
*H1 = Heat sink (Thermalloy 6070B)
J1, J2 = terminal, optional 12.6 V ac
R1, R2, R3, R6, R7 = 47 kΩ, ¼ W, 5%
R4 = 5.1 MΩ, ¼ W, 5%
R5 = 10.0 MΩ, ¼ W, 5%
R8 = 1.1 MΩ, ¼ W, 5%
R9 = 15 Ω, ½ W
R10 = 100 kΩ, ¼ W, 5%
S1, S3 = SPDT
S2 = 3-rocker DIP
U1 – U16 = MWS5114E
U17, = resistor module
22 kΩ, 16 pin
U18 = CD4001BE
U20 = CD4070BE
U21 = CDP1867CE
U22, U23 = CDP1866CE
U24 = CD4075BE
U25 = CA3078S
U26, U27 = CDP1856CE
U28, U29 = CD4050BE
U30 = resistor module
22 kΩ, 14 pin
U31 = CD4093BE
*VR1 = 5-V voltage regulator
(Fairchild 7805)

*User-supplied components for optional power supply.



CDP18S622

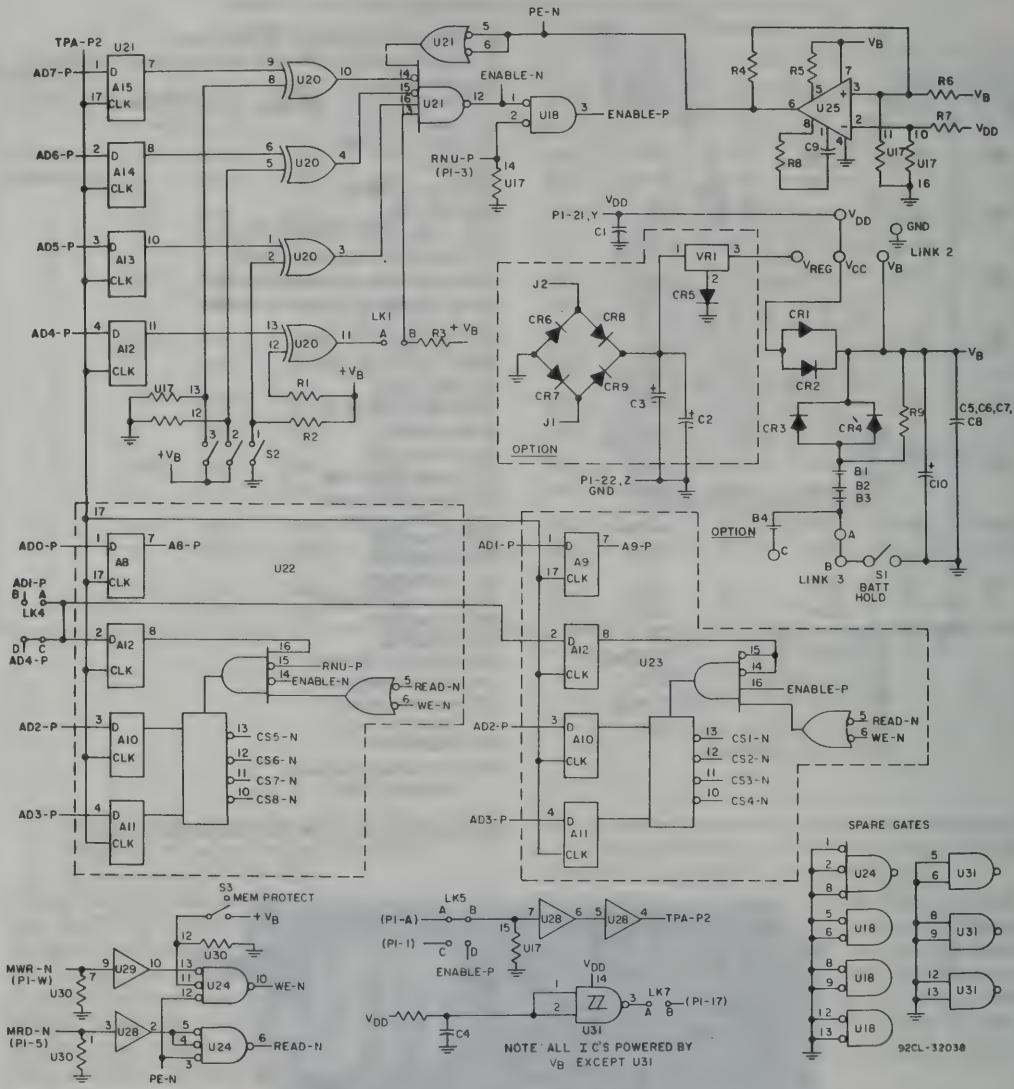


Fig. 3 - Logic diagram for RCA COSMAC Microboard Battery-Backup RAM CDP18S622 - control portion and optional power supply.

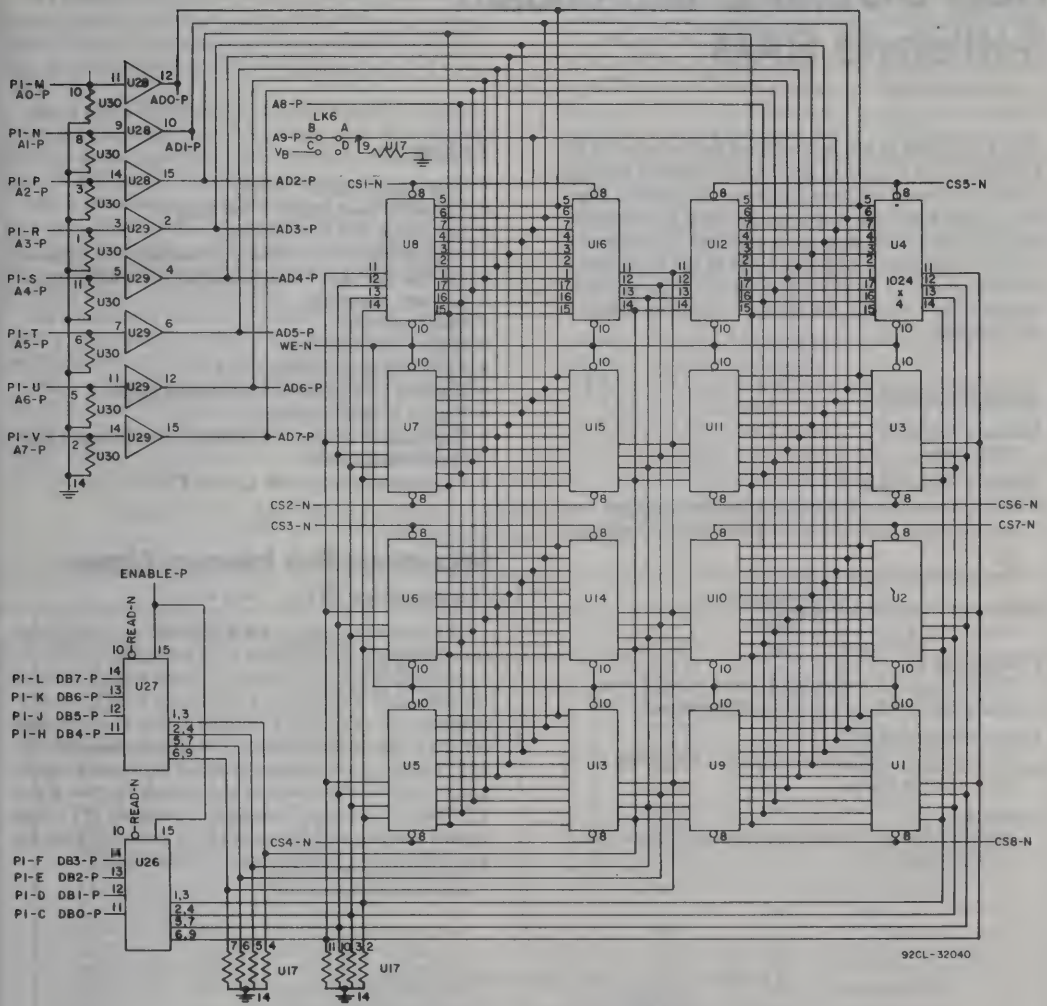


Fig. 4 - Logic diagram for RCA COSMAC Microboard Battery-Backup RAM CDP18S622 - memory and buffer portion.

CDP18S623A

RCA COSMAC Microboard 8-Kilobyte RAM

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A is a static read-write memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 8-kilobyte block in the 64-kilobyte memory space. A 3-rocker DIP switch is provided to set the binary value of the specific 8-kilobyte block to be occupied.

Specifications

Memory Capacity
8192 bytes

Memory Addressing
Occupies any contiguous 8-kilobyte block on any 8-kilobyte boundary within the 64-kilobyte address space.
Switch-selectable address.

Operating Temperature Range
-40 to +85°C

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm).
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
+5 volts at 6 milliamperes typical, operating at 2-MHz system clock.

Connector
System interface: edge fingers, 44 pins (dual 22) on 0.156-inch centers.

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Small size (4.5 x 7.5 inches)**
- **Compatible with COSMAC Development Systems**
- **Compatible with Micromonitor CDP18S030 expansion connector**
- **Fully buffered**
- **High noise immunity**
- **Flexible address assignment**
- **Member of extensive Microboard family**
- **Simple system interface**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Temperature range -40 to +85°C**

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard CPS18S623A.

For additional information on these signals, refer to the published data for the CDP1802A COSMAC Microprocessor (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.** These signals are summarized in Table I which gives a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on RCA COSMAC Microboard, CDP18S623A.

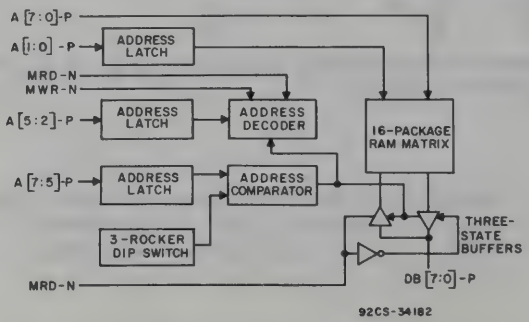


Fig. 1 - Block diagram of RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A.

CDP18S623A

A7 through A0 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM chip for the low-address byte, which becomes stable after TPA.

Bits 0 and 1 are latched in CDP1866CE (U1B and U2B) latch-decoders at TPA trailing edge. The output of these latches are wired to each memory chip, providing A8 and A9 for on-chip decoding.

Bits 2 and 3 are latched into two CDP1866CE latch-decoders (U1B, U6B) in parallel, forming A10 and A11, and decoded into two sets of four chip-enable lines. These lines are wired to two 4-kilobyte blocks of memory chips as chip-enables.

Bit 4 is latched into a CDP1866CE (U2B), forming A12, and is used to condition the two decoders so that only one 4-kilobyte block is addressed at any time.

Bits 5, 6, and 7 are latched into a CDP1866CE (U6B, U1B) forming A13, A14, and A15. These bits are compared with the setting of the 3 DIP switch rockers. When there is a match, the decoders and the data buffers are enabled.

DB7 through DB0 -These Data Bus lines are bidirectional and are interfaced through two CDP1866CE 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a match between the 3 high-address bits and the 3 DIP switch rockers. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted *to* the Microboard interface bus; when MRD is false, data bits are transmitted *from* the Microboard interface bus.

$\overline{\text{MRD}}$ - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the chip-select decoders.

$\overline{\text{MWR}}$ - Memory Write. This signal is buffered. It conditions each RAM chip and the chip-select decoders. It is the write command.

TPA - Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866CE latches. Latching takes place at the TPA trailing edge.

RNU - Run Utility. This signal, through link LK2A, pins 4 and 13, inhibits the board ENABLE signal,

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P *	In/Out	Data Bus	3	RNU-P *	—	Run Utility Request
D	DB1-P *	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P *	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N *	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

92CS-34443

*Signals used on RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A.

CDP18S623A

thereby eliminating memory access. The link may be cut if not required. Its purpose is to inhibit the board when its address is 0000 (DIP switches open) and a RUN UTILITY switch is causing the system to start at address 8000 instead of 0000.

Installation in a Microboard System

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A may be installed in any position in the five-card Microboard Chassis (CDP18S675), in the 22-card Microboard Chassis (CDP18S670), or in the Card Nest for the Microboard Computer Development Systems CDP18S693 and CDP18S694. No link changes are required.

The desired high-order three address bits should be set in the 3-rocker DIP switch S1. The least significant bit is rocker 1. The open position of the rocker generates a 0; the closed position generates a 1.

Installation in the COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III)

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A may be installed in the CDS II and CDS III in any memory slot 1 through 8. No Bank Select wiring is required on the backplane. The binary address of the 8-kilobyte block should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect pins 1 and 16 of link LK2A.

For the RNU signal, a connection is preprinted between pins 4 and 13 of link LK2A. On the CDS II backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

Installation in the Micromonitor CDP18S030

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. The binary number of the desired 8-kilobyte block address should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1). Connect link LK2A as shown in Table II.

Table II - Link LK2A Connections

Link LK2A	CDP18S623A Microboard	CDSII, CDSIII	CDP18S030 Micromonitor
1:16	Open	Short	Short
2:15	Short	Open	Open
3:14	Open	Open	Short
4:13	Optional	Optional	Open

When the CDP18S623A is used in this manner, it will respond only to the block address set into the DIP switch rockers. The memory disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the value set into the DIP switch rockers even though the EXM bit is true. This arrangement allows for the substitution of a given 8-kilobyte block of user memory and enables the remainder of user memory space to operate normally.

Physical Address Map

The physical address map given in Table III may be used to identify the board location of a memory device as a function of its address. Because the device organization is 1024 x 4, two devices are involved with any byte of data. Table III provides the two device locations for each address, one containing the high-order half byte and the other the low-order half byte. For example, if the hex address 8240 contains an error in the 2^2 bit, then the first line indicates that the device in question is in location U2C.

Table III - Physical Address Map of 16-Package RAM Matrix

Hex Address		Memory Location High Half-Byte	Memory Location Low Half-Byte
(0,2,4,6,8,A,C,E) (0-3)	XX	U2E	U2C
(0,2,4,6,8,A,C,E) (4-7)	XX	U2F	U2D
(0,2,4,6,8,A,C,E) (8-B)	XX	U1E	U1C
(0,2,4,6,8,A,C,E) (C-F)	XX	U1F	U1D
(1,3,5,7,9,B,D,F) (0-3)	XX	U6E	U6C
(1,3,5,7,9,B,D,F) (4-7)	XX	U6F	U6D
(1,3,5,7,9,B,D,F) (8-B)	XX	U5E	U5C
(1,3,5,7,9,B,D,F) (C-F)	XX	U5F	U5D

X = DON'T CARE

CDP18S623A

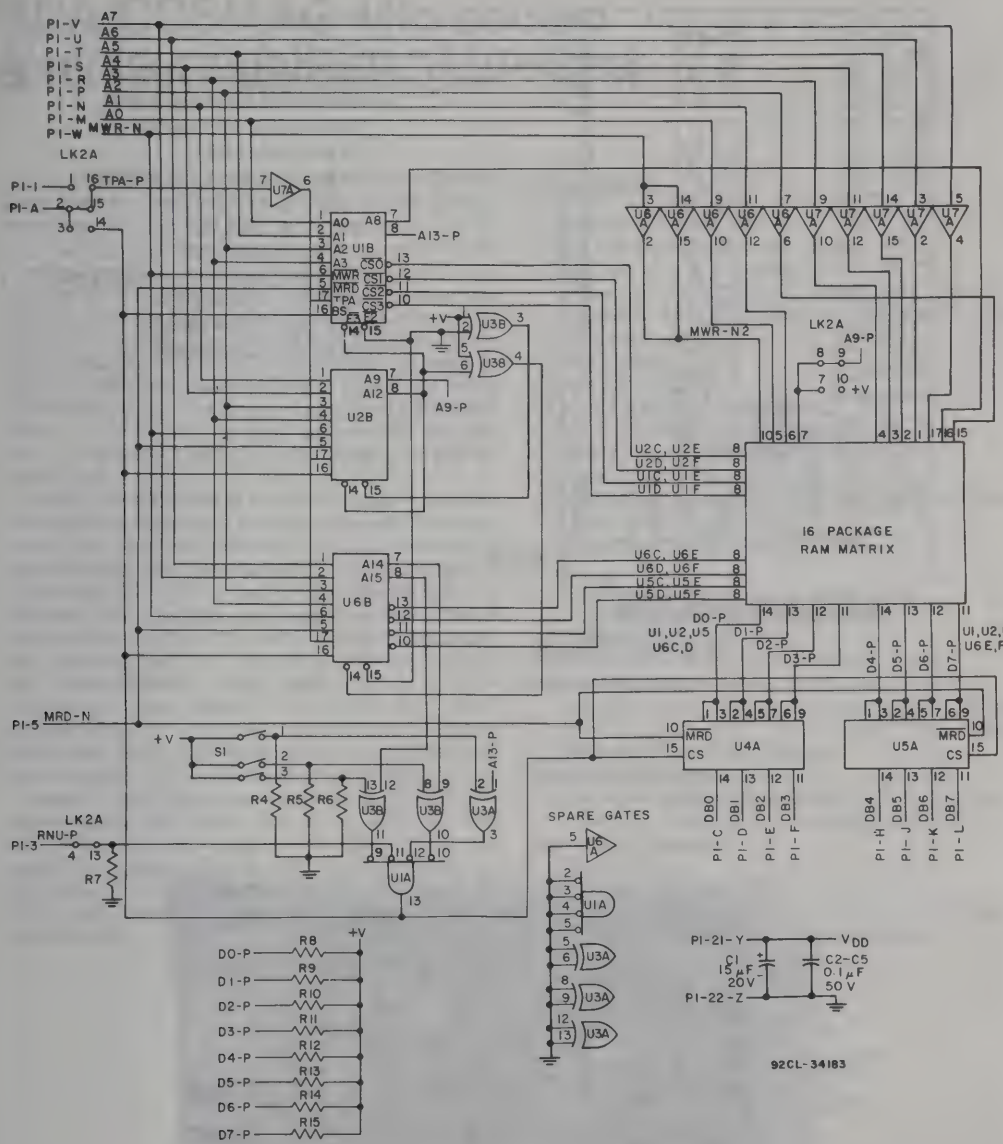


Fig. 2 - Logic diagram for RCA COSMAC Microboard 8-kilobyte RAM CDP18S623A.

CDP18S623A

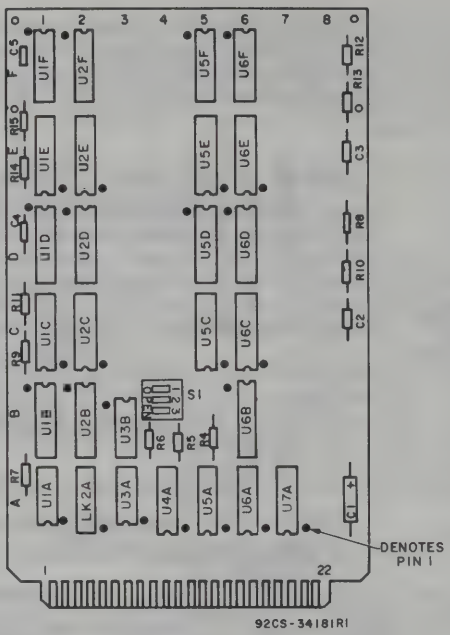
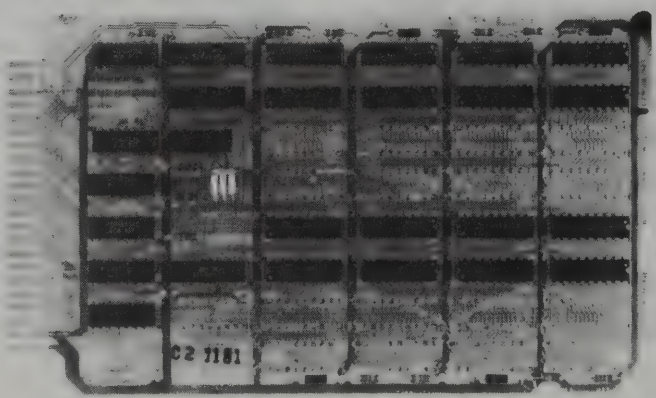


Fig. 3 - Layout diagram of RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623A.

Parts List

C1 = 15 uF, 20 V
C2-C5=0.1 uF, 50 V
R4-R15=22 kilohms, 1/4 W
S1=3-rocker DIP switch
U1A=CD4002BE
U1B,U2B,U6B=CDP1866CE
U1C,U1D,U1E,U1F
U2C,U2D,U2E,U2F
U5C,U5D,U5E,U5F
U6C,U6D,U6E,U6F=MWS5114E
U3A,U3B,=CD4070BE
U4A,U5A,=CDP1856CE
U6A,U7A=CD4050BE



CDP18S625

RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM

The RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 is a dual 4/8/16-kilobyte ROM/PROM memory module having on-board address latches and decoders. The eight 24-pin sockets provided permit the easy interchangeability of user-supplied ROM's, PROM's, or EPROM's. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The CDP18S625 provides for two independent blocks of memory each expandable from 1 to 16 kilobytes in 1-kilobyte increments within the 64-kilobyte memory space. Two sets of bank-select switches and two sets of links are provided for easy selection of ROM, PROM, or EPROM type and address range.

Because the CDP18S625 has two 4-position banks (A and B) for the memories, it can accommodate four different types of ROM/EPROM's and can operate up to three different types simultaneously. Bank A consists of U22, U26, U23, and U27 and is controlled by link LK9 and switch S1. See layout and logic diagrams. Bank B consists of U24, U28, U25, and U29 and is controlled by link LK13 and switch S2. Each bank must be populated with ROM/PROM's of the same size, 1, 2, or 4 kilobytes. One bank, however, can have ROM/PROM's of a size and type different from those in the other bank. Each bank can be independently addressed to different addresses and boundaries.

Memory types that can be used include the CDP1834 mask-programmed ROM and 2732, 2758, or 2716 EPROM's. The latter types can be programmed very rapidly in a suitable Microboard Computer System or a COSMAC Development System by means of the CDP18S480 PROM Programmer (See Product Description PD22A).

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small size (4.5 × 7.5 inches)
- Compatible with COSMAC Development Systems
- Compatible with Micromonitor CDP18S030 expansion connector
- Fully buffered
- High noise immunity
- Flexible address assignment
- Two independent memory banks
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range — 0°C to 70°C

Specifications

Memory Capacity

Two groups of four sockets accepting CDP1834 ROM or 2732, 2758, or 2716 EPROM; 1 to 32 kilobytes of read-only memory.

Memory Addressing

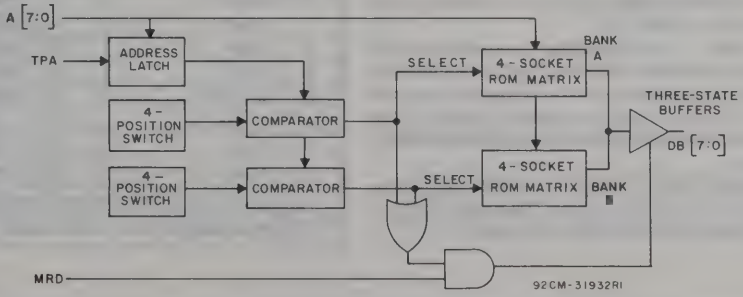
Switch-selectable block address on 1- to 32-kilobyte boundaries determined by memories selected.

Operating Temperature

0°C to 70°C

Dimensions

4.5 inches × 7.5 inches (114.3 mm × 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum



Block diagram of RCA COSMAC Microboard 8/16/32-Kilobyte ROM CDP18S625

CDP18S625

Power Requirements

+5 volts at 10 milliamperes typical, operating at 2-MHz system clock and using eight CDP1834 CMOS ROM's.

Connector

System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers.

Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 makes use of the following Microboard bus interface signals.

A7 through A0. Memory address bus on which the high- and low-order address bytes are multiplexed. These signals are buffered and then wired to each ROM for the low-address byte, which becomes stable after TPA. At the trailing edge of TPA, these same signals are latched, forming the high-order address bits A15 through A8. These high-order bits are latched and used in various combinations, depending on the ROM type, for generating the proper chip select.

The decoding scheme is as follows. The high-order bits are compared to DIP switch settings to generate a Bank Select signal. Because by choice of ROM type the bank may be 4, 8, or 16 kilobytes, the number of bits and switch positions needed to generate a bank select is 4, 3, or 2, respectively.

The next lower-order two bits, A11 and A10 for a 4-kilobyte bank, A12 and A11 for an 8-kilobyte bank, or A13 and A12 for a 16-kilobyte bank, are decoded into one of four chip select signals. One of these three decoders is selected by DIP switch settings, depending upon ROM type, and the resulting chip selects are wired to the ROM sockets.

In addition, A11 and A10 are gated to the ROM chips when appropriate to the type selected. That is, a 1-kilobyte ROM receives neither, a 2-kilobyte ROM receives A10 but not A11, and a 4-kilobyte ROM receives both A11 and A10.

Tables are provided giving all the switch settings for the various combinations.

DB7 through DB0. These **Data Bus** lines are interfaced through two CDP1856 4-bit Bus Buffer Separators (U31 and U32). These devices are in a high-impedance state in the bus direction until an enable is generated by a match between the high address bits and the DIP switch rockers.

$\overline{\text{MRD}}$ — Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered and conditions the chip-select decoders.

TPA — Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866 latches. Latching takes place at the TPA trailing edge.

RNU — Run Utility. This signal, through LK30 pins 4 and 5, forces A15 to be set at the TPA trailing edge, regardless of the value of A7. This feature is used in manual start controls where it is desired to start processing at address 8000_{16} instead of 0000.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625.

Table I-Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal	
A	TPA-P	*	1	DMAI-N	
B	TPB-P		2	DMAO-N	
C	DB0-P	*	3	RNU-P	*
D	DB1-P	*	4	INT-N	
E	DB2-P	*	5	MRD-N	*
F	DB3-P	*	6	Q-P	
H	DB4-P	*	7	SC0-P	
J	DB5-P	*	8	SC1-P	
K	DB6-P	*	9	CLEAR-N	
L	DB7-P	*	10	WAIT-N	
M	A0-P	*	11	−5 V/−15 V	
N	A1-P	*	12	SPARE	
P	A2-P	*	13	CLOCK OUT	
R	A3-P	*	14	N0-P	
S	A4-P	*	15	N1-P	
T	A5-P	*	16	N2-P	
U	A6-P	*	17	EF1-N	
V	A7-P	*	18	EF2-N	
W	MWR-N		19	EF3-N	
X	EF4-N		20	+12 V/+15 V	
Y	+5 V	*	21	+5 V	*
Z	GND	*	22	GND	*

*Signals used on RCA COSMAC Microboard 8/16/32-Kilobyte RAM CDP18S625.

ROM/PROM Installation

Using the CDP1834 or 2758 1-Kilobyte ROM/PROM. To utilize the CDP1834 mask-programmable ROM or the 2758 EPROM in the CDP18S625, it is necessary to program DIP switch S1 or S2, depending on whether Bank A or Bank B of the Microboard is used, as follows. Switch rockers 5 through 8 must be closed and rockers 1 through 4 are set by the user for one of 16 4-kilobyte address areas as shown in Table II. The setting selected will position the four sockets of Bank A or Bank B for use with four ROM/PROM's. To use fewer than four ROM/PROM's, it may be necessary to cut the link positions associated with the sockets to be disabled as shown in Table III. Cutting these links forces the Chip-Select signal false for the unused socket, thereby freeing the memory space normally occupied by those sockets. This freed memory space may then be assigned to other Microboards in the system. If this unused memory space is not needed elsewhere, the links need not be cut.

Using the 2716 2-Kilobyte EPROM. To utilize four 2716 EPROM's in the CDP18S625, it is necessary to set rockers 4, 3, and 2 of switch S1 or S2 (depending whether Bank A or Bank B is used) to select one of eight 8-kilobyte address areas, as shown in Table IV. If two 2716 EPROM's are used, rocker 7 of the switch should be closed and rocker 1 can then be used to control address locations, as shown in Table V. If one 2716 EPROM is to be used, one link position associated with the unused socket needs to be cut. The user should first select a pair of EPROM socket positions as indicated in Table V and then cut the link position associated with the unused socket of the pair. For example, if socket U23 were to be used for the one 2716 EPROM needed, the user should first select the pair U23 and U27 and set the rockers of switch S1 in accordance with Table V; that is, rockers 1, 5, 6, and 7 are closed, rocker 8 is open, and rockers 2, 3, and 4 may be either open or closed (X = don't care). Then, to deselect U27, link position 4 of LK9 should be cut. This link need not be cut if it is acceptable to the system for the address space occupied by the socket to be unusable.

Using the 2732 4-Kilobyte EPROM. To utilize the 2732 EPROM in the CDP18S625, it is necessary to use rockers 4 and 3 of switch S1 or S2 (depending on whether Bank A or Bank B is used). Table VI shows how to select one of the four 16-kilobyte address areas. Rockers 1, 2, and 5 through 8 are left in the open position. If fewer than four 2732 EPROM's are used, it is advisable to deselect the unused address areas as shown in Table VII. When only one socket is to be used, rockers 5 and 7 can be closed and thus allow the use of rockers 2 and 1 to control which EPROM is selected, as shown in Table VIII.

Table II-Addresses and Corresponding Switch Rocker Positions for Installing the CDP1834 or 2758 ROM/EPROM in the CDP18S625

4-Kilobyte Address	Switch (S1 or S2) Rocker 4 3 2 1	5 6 7 8
0XXX	O O O O	C C C C
1XXX	O O O C	C C C C
2XXX	O O C O	C C C C
3XXX	O O C C	C C C C
4XXX	O C O O	C C C C
5XXX	O C O C	C C C C
6XXX	O C C O	C C C C
7XXX	O C C C	C C C C
8XXX	C O O O	C C C C
9XXX	C O O C	C C C C
AXXX	C O C O	C C C C
BXXX	C O C C	C C C C
CXXX	C C O O	C C C C
DXXX	C C O C	C C C C
EXXX	C C C O	C C C C
FXXX	C C C C	C C C C

Rocker ON = Closed (C); OFF = Open (O)
X = Don't care.

Table III-Relationship of Link LK9 and LK13 Link Positions, Bank, Associated Socket Number, and Chip-Select Signal

Link Position (LK9 or LK13)	Socket/Chip Select Signal Bank A	Bank B
1	U22/CS1	U24/CS5
2	U26/CS2	U28/CS6
3	U23/CS3	U25/CS7
4	U27/CS4	U29/CS8

Installation in a Microboard System

The RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 may be installed in any position in the five-card Microboard Chassis (CDP18S675)

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Table IV-Addresses for Installing the 2716 2-Kilobyte EPROM in the CDP18S625

Link of LK9 or LK13	1	2	3	4	Switch (S1 or S2) Rocker Position 4 3 2	1 5 6 7 8
	Socket Designation					
(LK9) Bank A (LK13) Bank B	U22 U24	U26 U28	U23 U25	U27 U29		
Address Area						
0000- 1FFF	0000 07FF	0800 0FFF	1000 17FF	1800 1FFF	O O O	O C C O O
2000 3FFF	2000 27FF	2800 2FFF	3000 37FF	3800 3FFF	O O C	O C C O O
4000 5FFF	4000 47FF	4800 4FFF	5000 57FF	5800 5FFF	O C O	O C C O O
6000 7FFF	6000 67FF	6800 6FFF	7000 77FF	7800 7FFF	O C C	O C C O O
8000 9FFF	8000 87FF	8800 8FFF	9000 97FF	9800 9FFF	C O O	O C C O O
A000 BFFF	A000 A7FF	A800 AFFF	B000 B7FF	B800 BFFF	C O C	O C C O O
C000 DFFF	C000 C7FF	C800 CFFF	D000 D7FF	D800 DFFF	C C O	O C C O O
E000 FFFF	E000 E7FF	E800 EFFF	F000 F7FF	F800 FFFF	C C C	O C C O O
Rocker ON = Closed (C); OFF = Open (O)						

or in the 25-card Microboard Chassis (CDP18S670). No link changes are required.

The desired high-order address bits should be set in one or both of the two eight-rocker DIP switches S1 and S2. The least significant bit is rocker 1. The open position of the rocker generates a 0, the closed position generates a 1.

Installation in the COSMAC Development Systems

The CDP18S625 may be installed into any of the available memory slots (1 through 8) in the COSMAC Development System (CDS II) CDP18S005 or in the COSMAC DOS Development System (CDS III) CDP18S007 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement.

When a CDP18S625 is installed in a COSMAC Development System, no Bank Select wiring is required on the backplane. The binary address of the address area in which the CDP18S625 ROM is to reside should be set on DIP switches S1 or S2 (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect pins 1 and 8 of link LK30 on the CDP18S625; or, as an alternative, connect pins 1 and A of the backplane connector to be used.

For the RNU signal, a connection is preprinted between pins 4 and 5 of link LK30. On the CDS backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

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Table V-Switch (S1 or S2) Rocker Position Guide for Using One or Two 2716 EPROM's in the CDP18S625

Link of LK9 or LK13	1	2	3	4	Switch (S1 or S2) Rocker Position 4 3 2 1	5 6 7 8
	Socket Designation					
(LK9) Bank A (LK13) Bank B	U22 U24	U26 U28	U23 U25	U27 U29		
Address Area						
0000-0FFF	0000 07FF	0800 0FFF	—	—	OOOO	CCCO
1000 1FFF	—	—	1000 17FF	1800 1FFF	OOOC	CCCO
2000 2FFF	2000 27FF	2800 2FFF	—	—	OOCO	CCCO
3000 3FFF	—	—	3000 37FF	3800 3FFF	OOCC	CCCO
4000 4FFF	4000 47FF	4800 4FFF	—	—	OCOO	CCCO
5000 5FFF	—	—	5000 57FF	5800 5FFF	OCOC	CCCO
6000 6FFF	6000 67FF	6800 6FFF	—	—	OCCO	CCCO
7000 7FFF	—	—	7000 77FF	7800 7FFF	OCCC	CCCO
8000 8FFF	8000 87FF	8800 8FFF	—	—	COOO	CCCO
9000 9FFF	—	—	9000 97FF	9800 9FFF	COOC	CCCO
A000 AFFF	A000 A7FF	A800 AFFF	—	—	COCO	CCCO
B000 BFFF	—	—	B000 B7FF	B800 BFFF	COCC	CCCO
C000 CFFF	C000 C7FF	C800 CFFF	—	—	CCOO	CCCO
D000 DFFF	—	—	D000 D7FF	D800 DFFF	CCOC	CCCO
E000 EFFF	E000 E7FF	E800 EFFF	—	—	CCCO	CCCO
F000 FFFF	—	—	F000 F7FF	F800 FFFF	CCCC	CCCO

Rocker ON = Closed (C); OFF = Open (O)

CDP18S625

Table VI-Addresses for Installing the 2732 4-Kilobyte EPROM in the CDP18S625

Link of LK9 or LK13	1	2	3	4	Switch (S1 or S2) Rocker Position 4 3 2 1 5 6 7 8
	Socket Designation				
(LK9) Bank A (LK13) Bank B	U22 U24	U26 U28	U23 U25	U27 U29	
Address Area					
0000-3FFF	0XXX	1XXX	2XXX	3XXX	O O O O O O O
4000 7FFF	4XXX	5XXX	6XXX	7XXX	O C O O O O O
8000 BFFF	8XXX	9XXX	AXXX	BXXX	C O O O O O O
C000 FFFF	CXXX	DXXX	EXXX	FXXX	C C O O O O O
Rocker ON = Closed (C); OFF = Open (O); X = Don't care.					

Table VII-Switch (S1 or S2) Rocker Position Guide for Using Two 2732 EPROM's in the CDP18S625

Link of LK9 or LK13	1	2	3	4	Switch (S1 or S2) Rocker Position 4 3 2 1 5 6 7 8
	Socket Designation				
(LK9) Bank A (LK13) Bank B	U22 U24	U26 U28	U23 U25	U27 U29	
Address Area					
0000-1FFF	0XXX	1XXX	—	—	O O O C O O O O
2000 3FFF	—	—	2XXX	3XXX	O O C C O O O O
4000 5FFF	4XXX	5XXX	—	—	O C O C O O O O
6000 7FFF	—	—	6XXX	7XXX	O C C C O O O O
8000 9FFF	8XXX	9XXX	—	—	C O O C O O O O
A000 BFFF	—	—	AXXX	BXXX	C O C C O O O O
C000 DFFF	CXXX	DXXX	—	—	C C O C O O O O
E000 FFFF	—	—	EXXX	FXXX	C C C C O O O O
Rocker ON = Closed (C); OFF = Open (O); X = Don't care.					

Table VIII-Switch (S1 or S2) Rocker Position Guide for Using One 2732 EPROM in the CDP18S625

Link of LK9 or LK13	1	2	3	4	Switch (S1 or S2) Rocker Position
	Socket Designation				4 3 2 1 5 6 7 8
(LK9) Bank A (LK13) Bank B	U22 U24	U26 U28	U23 U25	U27 U29	
Address Area					
0000-0FFF	0XXX	—	—	—	OOOO COCO
1000 1FFF	—	1XXX	—	—	OOOC COCO
2000 2FFF	—	—	2XXX	—	OOCO COCO
3000 3FFF	—	—	—	3XXX	OOCC COCO
4000 4FFF	4XXX	—	—	—	OCOO COCO
5000 5FFF	—	5XXX	—	—	OCOC COCO
6000 6FFF	—	—	6XXX	—	OCCO COCO
7000 7FFF	—	—	—	7XXX	OCCC COCO
8000 8FFF	8XXX	—	—	—	COOO COCO
9000 9FFF	—	9XXX	—	—	COOC COCO
A000 AFFF	—	—	AXXX	—	COCO COCO
B000 BFFF	—	—	—	BXXX	COCC COCO
C000 CFFF	CXXX	—	—	—	CCOO COCO
D000 DFFF	—	DXXX	—	—	CCOC COCO
E000 EFFF	—	—	EXXX	—	CCCO COCO
F000 FFFF	—	—	—	FXXX	CCCC COCO

Rocker ON = Closed (C); OFF = Open (O); X = Don't care.

CDP18S625

Installation in the Micromonitor CDP18S030

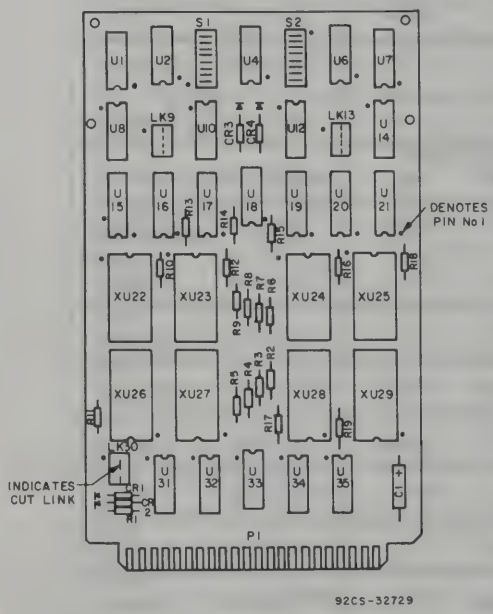
The RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. Depending on the ROM/PROM complement used, addressing should be selected as described in the **ROM/PROM Installation** section. Link LK30 should be connected as follows:

3 to 6 — shorted
2 to 7 — open (Cut preprinted link)
1 to 8 — shorted

When the CDP18S625 is used in this manner, it will respond only to the block address set by the user. The memory disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the value set on the CDP18S625 even though the EXM bit is true. This arrangement allows for the substitution of a given block of user memory and enables the remainder of user memory space to operate normally.

General Setup Information

If it is desired to use only one of the two ROM/PROM Banks provided on the CDP18S625, the user should set up the unused Bank exactly the same as for the used Bank. In this way no system memory area is lost.



Layout diagram of RCA COSMAC Microboard 8/16/32-Kilobyte ROM CDP18S625

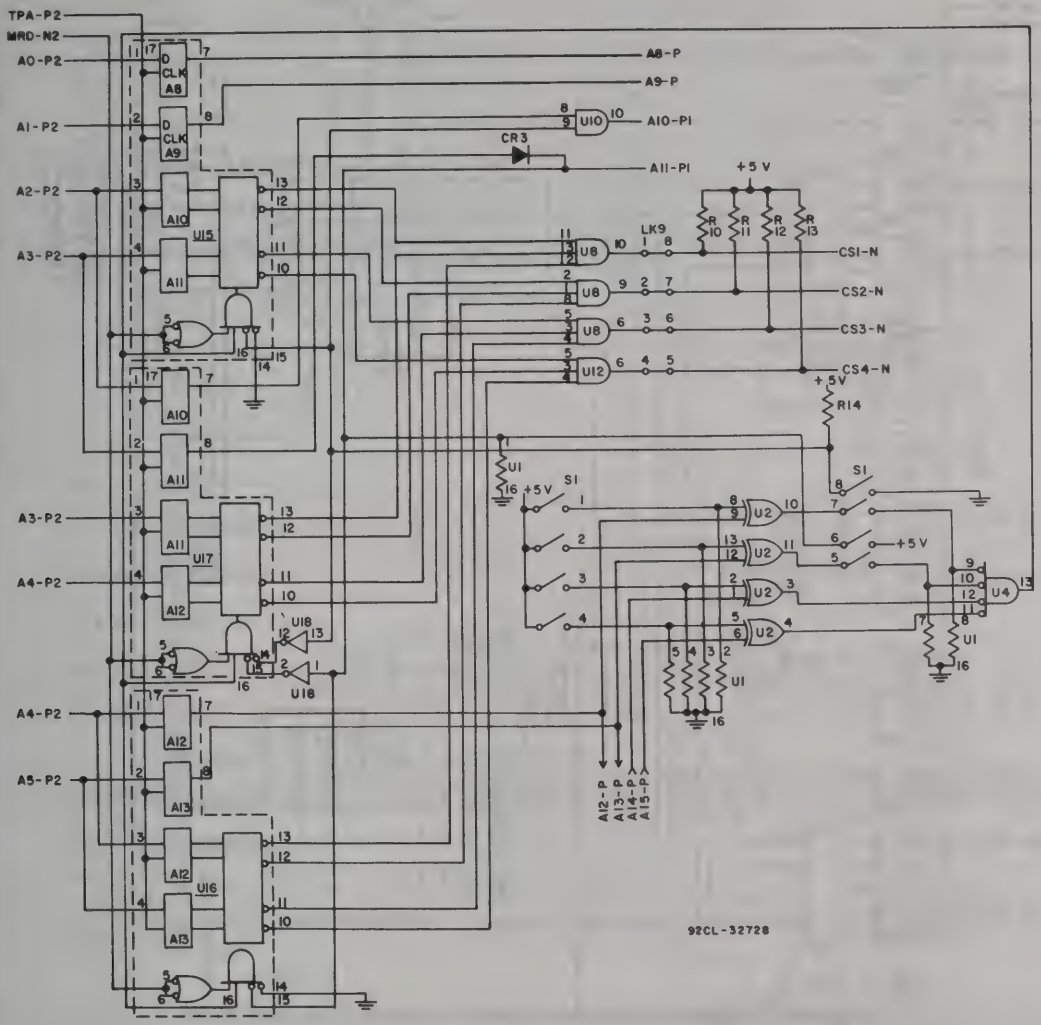
Parts List

C1 = 15 μF, 50 V
CR1-CR4 = 1N270
R1-R19 = 22 kΩ, ¼ W
S1, S2 = 8-rocker DIP switch

U1, U7 = resistor module, 22 kΩ, 16 pin
U2, U6 = CD4070BE
U4 = CD4002BE
U8, U12, U14 = CD4073BE
U10 = CD4081BE
U15-U17, U19-U21 = CDP1866CE
U18 = CD4069BE
U31, U32 = CDP1856CE
U33 = CD4068BE
U34, U35 = CD4050BE

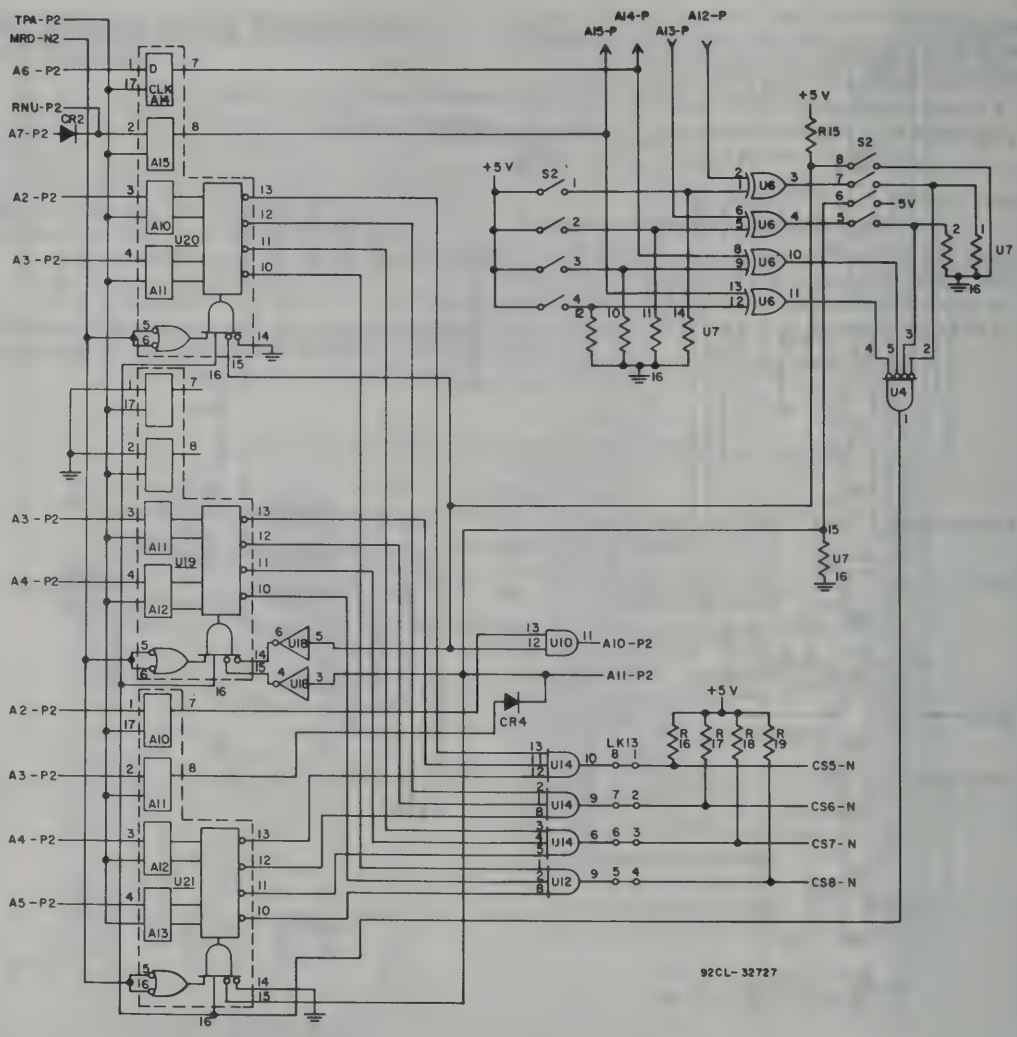
XU22-XU29 = 24-pin socket

CDP18S625



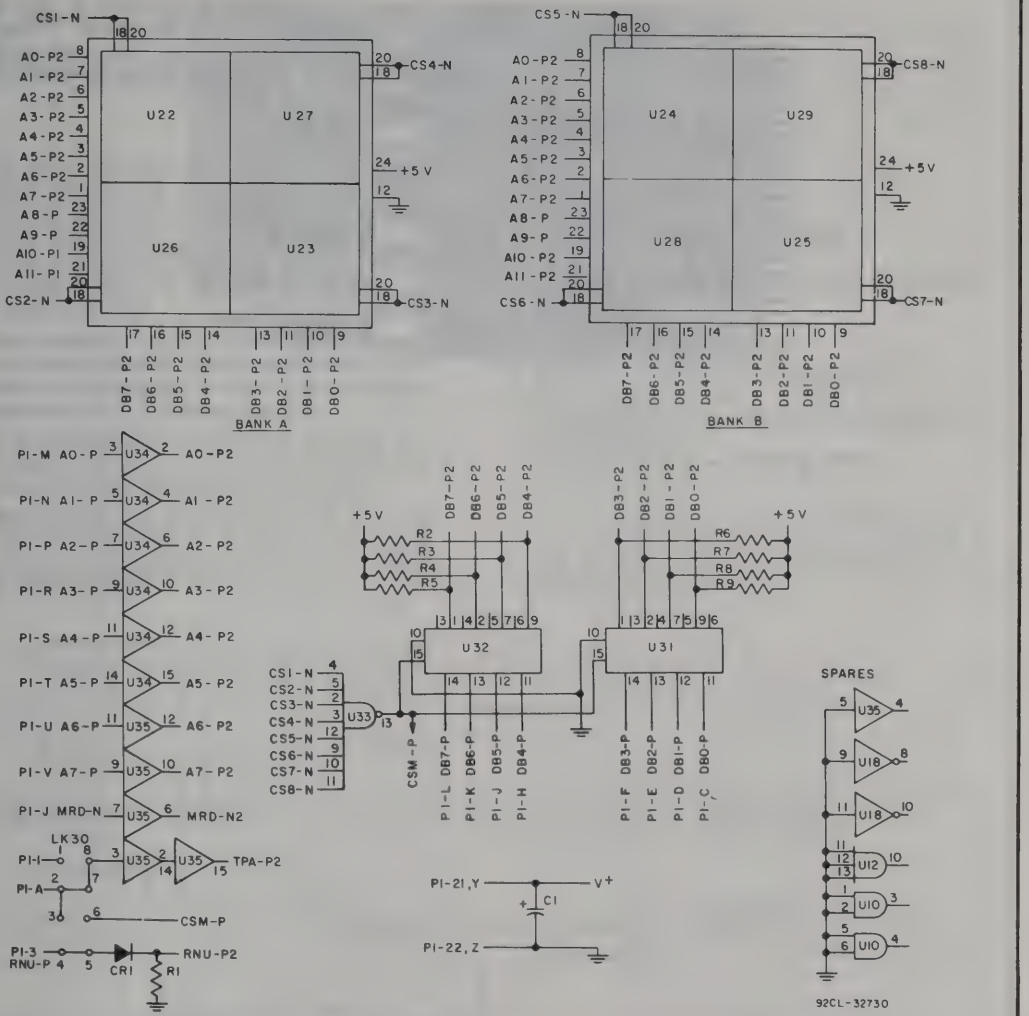
RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 Logic Diagram - Bank A - Control Section

CDP18S625



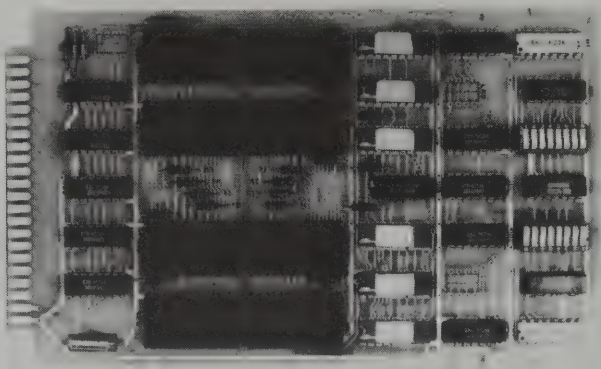
RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 Logic Diagram - Bank B - Control Section

CDP18S625



RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625
Logic Diagram - Memory Section

CDP18S625



CDP18S626

RCA COSMAC Microboard 32/64-Kilobyte EPROM/ROM/RAM

The RCA COSMAC Microboard 32/64-kilobyte EPROM/ROM/RAM CDP18S626 is a versatile memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The CDP18S626 contains 16 24-pin sockets which can be populated as follows:

1. With industry-type 2716 EPROM or a mask-programmable ROM, the CDP18S626 provides 32 kilobytes of contiguous read-only memory in either high-or-low half of memory space.
2. With industry-type 2732 EPROM or a mask programmable ROM, the CDP18S626 provides 64 kilobytes of contiguous read only memory.
3. With industry-type 6116 CMOS static RAM the CDP18S626 provides 32 kilobytes of contiguous static read-write memory in either high-or-low half of memory space.
4. With a combination of 2716-type EPROM/ROM and 6116-type static RAM in either high-or-low half of address space, the CDP18S626 provides 32 kilobytes of memory.

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Small size (4.5 x 7.5 inches)**
- **Compatible with COSMAC Development Systems**
- **Fully buffered**
- **High noise immunity**
- **Flexible address assignment**
- **Member of extensive Microboard family**
- **Simple system interface**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Temperature range — -40° C to +85° C**

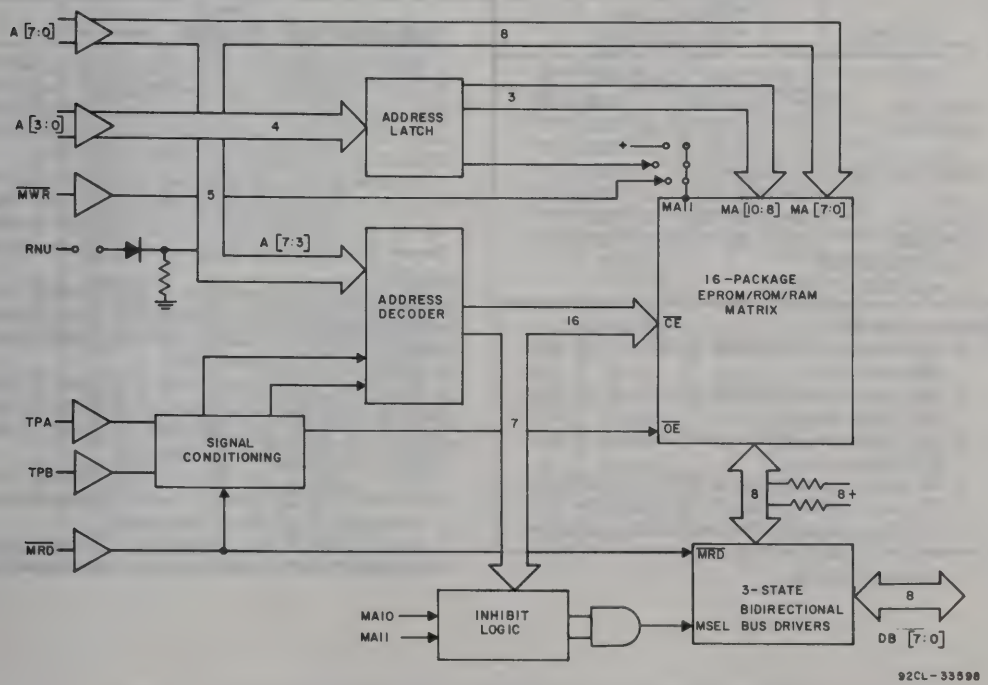


Fig 1. — RCA COSMAS Microboard 32/64-kilobyte EPROM/ROM/RAM CDP18S626 — Block Diagram

CDP18S626

The CDP18S626 includes inhibit features that make it possible to inhibit 1-, 2-, or 4-kilobyte segments in contiguous memory spaces in certain banks, as shown in the Memory Maps in Figs. 2, 3, and 4.

Note: The CDP18S626 is factory-linked to accept the 2716-type EPROM/ROM in low-half of address space. The linking arrangements for the CDP18S626 can easily be changed to permit other operating modes as listed in Table III. Examples are shown in Figs. 5, 6, and 7.

Specifications

Memory Inhibit

EPROM or RAM	Address Space (Hexadecimal)	
2732-Type EPROM	or E000-EFFF or F000-FFFF or E000-FFFF or E000-E3FF or E400-E7FF or E800-EBFF or EC00-EFFF or F000-F3FF or F400-F7FF or F800-FBFF or FC00-FFFF	
	Low-Half	High-Half
2716-Type EPROM or 6116-Type RAM or 2716-Type EPROM/ 6116-Type RAM Combination	7000-77FF or 7800-7FFF or 7000-7FFF or 7000-73FF or 7400-77FF or 7800-7BFF or 7C00-7FFF	F000-F7FF or F800-FFFF or F000-FFFF or F000-F3FF or F400-F7FF or F800-FBFF or FC00-FFFF

Memory Capacity

65,536 bytes - 16 EPROM/ROM's, 2732 type, 4096 x 8

32,768 bytes - 16 EPROM/ROM's, 2716 type, 2048 x 8

32,768 bytes - 16 CMOS static RAM's 6116 type, 2048 x 8

32,768 bytes - Combination of EPROM/ROM type 2716 and CMOS static RAM type 6116. Four 8-kilobyte blocks each of which can be assigned to the 6116 or 2716 types for a total of 14 different combinations.

Memory Addressing

EPROM-type 2732 - Contiguous 65,536 bytes in full address space

EPROM-type 2716 - Contiguous 32,768 bytes in low-or-high-address space

RAM-type 6116 - Contiguous 32,768 bytes in low-or-high-address space

EPROM/RAM Combination - type 2716/6116 - Contiguous 32,768 bytes in low-or-high-address space

Operating Temperature Range

−40° C to +85° C

(For operation over the full temperature range, the user must select the ROM or RAM specified for this range.)

Dimensions

4.5 inches x 7.5 inches (114.3 mm x 190.5 mm). Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

At 5 volts and a 2-MHz system clock, approximately 1 milliampere plus the power required for the user-selected EPROM or ROM.

Connector

System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers.

Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 32/64-Kilobyte EPROM/ ROM/ RAM CDP18S626.

A7 through A0 — Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each memory device for the low-address byte, which becomes stable after TPA.

Bits 1 and 0 are latched in a CDP1866CE (U27) Latch-Decoder at the trailing edge of TPA. The outputs of this latch, A9 and A8, are wired to each memory device for on-chip decoding.

Bits 3 and 2 are latched in a CDP1866CE (U28) Latch-Decoder at the trailing edge of TPA. The outputs of the latch, A11 and A10, are wired to each memory device for on-chip decoding.

Bits 7 and 6 are latched and decoded in a CDP1866CE (U28). Each of the four outputs decodes a 16-kilobyte block of memory space.

Bits 5 and 4 are latched and decoded in a CDP1866CE (U27). Each of the four outputs decodes

a 1-kilobyte segment of each 4-kilobyte block. The outputs of the two one-of-four decoders are ORed to provide 16 chip selects for unique decoding of sixteen 4-kilobyte memory blocks. This description refers to the board populated with the 2732-type EPROM/ROM.

If a 2048 x 8 memory device (2716-type EPROM/ROM or 6116-type RAM) is used, high-or low-address space is selected by latching bit A7 with TPA and using the appropriate links to link the output to chip enable on U28. Bits 6 and 5 are then linked to Latch-Decoder U28. Each of the four outputs of U28 decodes an 8-kilobyte block. Bits 4 and 3 are linked to Latch-Decoder U27, where each of the four outputs decodes a 2-kilobyte segment of each 8-kilobyte block. Thus, the same OR gates used for the 2732 type EPROM/ROM also provide the required 16 chip selects for low- or high-address space when the 2716-type or the 2716/6116-type ROM/RAM combination are used.

DB7 through DB0 — These **Data Bus** lines are bidirectional and are interfaced through two CDP1856CE 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a memory select signal. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted *to* the Microboard interface bus; when MRD is false, data bits are transmitted *from* the Microboard interface bus.

$\overline{\text{MRD}}$-Memory Read. When true, $\overline{\text{MRD}}$ indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the chip-select decoders.

$\overline{\text{MWR}}$-Memory Write. This signal is buffered. It conditions each RAM chip and the chip-select decoders and is the write command.

TPA-Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866CE (U28 and U27) and CD4013BE (U29) latches. Latching takes place at the TPA trailing edge.

TPB-Timing Pulse B. This signal is used to condition the output enable (OE) signal for the memory devices, in order to avoid bus contention.

RNU-Run Utility. This signal, through pins 8 and 9 on link LKE, forces execution of a program to start at address 8000H. This feature allows the user to put an on-board utility program at location 8000H. (H indicates hexadecimal notation)

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P *	In/Out	Data Bus	3	RNU-P *	—	Run Utility
D	DB1-P *	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N*	In	Clear-Mode Control
L	DB7-P *	In/Out	Data Bus	10	WAIT-N *	In	Wait-Mode Control
M	A0-P *	Out	Multiplexed Address Bus	11	_5 V/_15 V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N*	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

*Signals used on RCA COSMAC Microboard CDP18S626.

CDP18S626

Inhibit Logic

The following paragraph applies only to the 2732 EPROM/ROM. For addresses of the "holes" that can be inserted in the Memory Maps, refer to the listings under Memory Addressing.

In order to enable the Bus Buffer/Separators with MSEL, one of the inputs to NAND gate U22 must be in the active low state. For example, if bank F must be inhibited, open link LKA between pins 9 and 10. Similarly, if bank E must be inhibited, open link LKA between pins 7 and 12. If only 1-kilobyte "holes" within either bank are required, decoder U5 and two link locations on link LKE must be programmed, while links on LKA between pins 7:12 and 9:10 remain closed. One of the four decoder outputs selects the 1-kilobyte segment to be inhibited. Banks E or F are selected by linking pins 7:10 or 6:11 on LKE.

Linking Arrangements

Tables II-1 through II-15 provide the required links for combinations of memory types and memory space allocation. These tables also provide the means for inhibiting access within the "holes" in memory space which may be occupied by memory on other boards.

Links are arranged in groups called LKA, LKB, LKC, LKD, and LKE. These groups are arranged in the DIP (dual-in-line package) configuration to mate with the DIP sockets mounted on the Microboard. These links can be programmed by the use of DIP SHUNT devices.

The CDP18S626 Microboard Computer is shipped with DIP shunts as shown in Fig. 6, and linked according to Table II-1 for the 2716-type EPROM in the low-half of address space, with no inhibit features.

Table III lists the modes of operation for the CDP18S626 and the memory types that can be used with this Microboard. All 15 options are summarized in the tables for links Tables II-1 through II-15.

In the following most common modes of operation the programming of the DIP shunt is simple. The programming applies to the 2732-type EPROM for the full addressable range 0000-FFFF, and to the 2716-type EPROM and the RAM-type 6116 for the low-half of address space 0000-7FFF. The programmed links are illustrated in Figs. 5, 6, and 7.

Inhibit Features

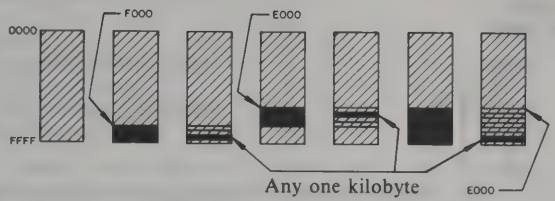
For example, if inhibit features are desired for the 2732, proceed as follows: First, set up links A, B, C, D, and E as required for full address space (no inhibit). To inhibit segment F000-F3FF, make the required changes as shown in Table II-6 as follows. Leave links LKA, LKB, and LKD as is, open links 2:15 and 3:14 on LKC, and close links 1:16, 2:15 and 6:11 on LKE.

Table III — Modes of Operation for the CDP18S626 Microboard

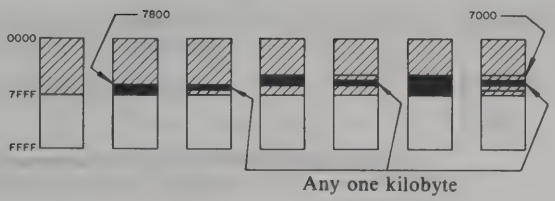
Table	Memory		Address Space		Inhibit Feature	
	Class	Type	Low-Half	High-Half		
RAM						
II-1*	EPROM	2716	0000-7FFF	—	—	NO
II-2	EPROM	2716	0000-7FFF	—	YES	—
II-3	EPROM	2716	—	8000-FFFF	—	NO
II-4	EPROM	2716	—	8000-FFFF	YES	—
II-5	EPROM	2732	0000-FFFF		—	NO
II-6	EPROM	2732	0000-FFFF		YES	—
II-7	EPROM	2732	0000-EFFF		YES BANK F	—
II-8	RAM	6116	0000-7FFF	—	—	NO
II-9	RAM	6116	0000-7FFF	—	YES	—
II-10	RAM	6116	—	8000-FFFF	—	NO
II-11	RAM	6116	—	8000-FFFF	YES	—
EPROM/RAM Combination						
II-12	2716/6116		0000-7FFF	—	—	NO
II-13	2716/6116		0000-7FFF	—	YES	—
II-14	2716/6116		—	8000-FFFF	—	NO
II-15	2716/6116		—	8000-FFFF	YES	—

*Factory-supplied option, See Fig. 6.

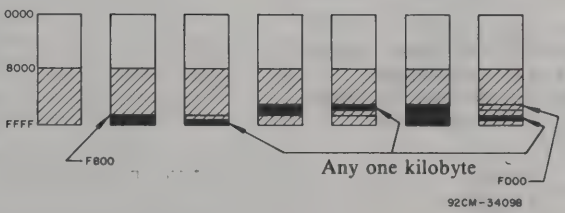
1. Using the 2732-type EPROM



2. Using the 2716-type EPROM
   (a) Low-Half Address Space



   (b) High-Half Address Space

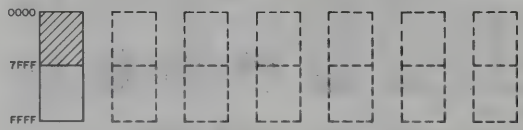


Note: Cross-Hatched Areas Indicate Address Range Covered. Black Areas Indicate Programmable Inhibit Area

Fig. 2 — Memory Maps

CDP18S626

3. Using the 6116-type RAM
   (a) Low-Half Address Space



1-kilobyte and 2-kilobyte segments between 7000 and 7FFF can be inhibited similarly as shown under 2(a).

   (b) High-Half Address Space

1-kilobyte and 2-kilobyte segments between F000 and FFFF can be inhibited similarly as shown under 2(b).

4. Using the 2716-type EPROM and the 6116-type RAM
   (a) Low-Half Address Space
   14 different combinations of 8-kilobyte blocks of 2716-type EPROM and 6116-type RAM
   Each 8-kilobyte segment may be filled with either a 2716-type EPROM or a 6116-type RAM

1-kilobyte and 2-kilobyte segments between 7000 and 7FFF can be inhibited similarly as shown under 2(a).

Note: Cross-Hatched Area Indicates Address Range Covered

92CM-34097

Fig. 3 - Memory Maps

5. Using the 2716-type EPROM and the 6116-type RAM
   (a) High-Half Address Space
   14 different combinations of 8-kilobyte blocks of 2716-type EPROM and 6116-type RAM
   Each 8-kilobyte segment may be filled with either a 2716-type EPROM or a 6116-type RAM

1-kilobyte and 2-kilobyte segments between F000 and FFFF can be inhibited similarly as shown under 2(b).

Note: Cross-Hatched Area Indicates Address Range Covered

Fig. 4 - Memory Maps

LKA: Install unprogrammed 9-Section DIP Shunt
LKB: Leave Open
LKC: Install unprogrammed 8-Section DIP Shunt
LKD: Leave Open
LKE: Leave Open

Note: Cross-Hatched Area Indicates Socket with DIP Shunt Installed

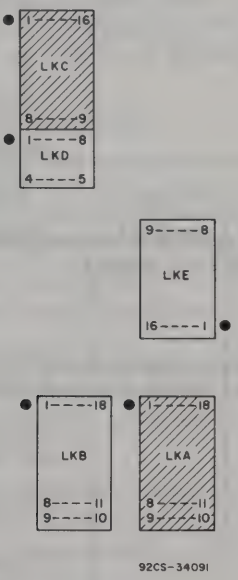
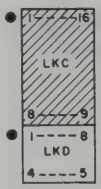
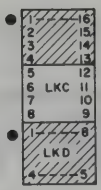


Fig. 5 - Linking Arrangements for EPROM/ROM Type 2732 (addressable range: 0000-FFFF.)

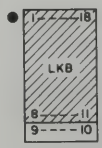
CDP18S626

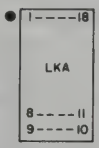


LKA: Leave Open
LKB: Install unprogrammed 8-Section DIP Shunt (9:10 Is Open)
LKC: Install unprogrammed 8-Section DIP Shunt
LKD: Leave Open
LKE: Leave Open



LKA: Leave Open
LKB: Install unprogrammed 8-Section DIP Shunt (9:10 Is Open)
LKC: Install unprogrammed 4-Section DIP Shunt (5:12, 6:11, 7:10, 8:9 Are Open)
LKD: Install unprogrammed 4-Section DIP Shunt
LKE: Leave Open





92CS-34092

Note: Cross-Hatched Area Indicates Socket with DIP Shunt Installed

Fig. 6 - Linking Arrangements for EPROM/ROM Type 2716 (addressable range: 0000-7FFF.)

92CS-34094

Note: Cross-Hatched Area Indicates Socket with DIP Shunt Installed

Fig. 7 - Linking Arrangments for RAM Type 6116 (addressable range: 0000-7FFF.)

Table II-1 — Linking Arrangements for 2716-Type EPROM
No Inhibit Feature, Low-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
		DIP Shunt*		DIP Shunt*					
Open	1:18	Closed	1:18	Closed	1:16	Open	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Open	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	Open	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Open	4:5	Open	4:13
Open	5:14	Closed	5:14	Closed	5:12			Open	5:12
Open	6:13	Closed	6:13	Closed	6:11			Open	6:11
Open	7:12	Closed	7:12	Closed	7:10			Open	7:10
Open	8:11	Closed	8:11	Closed	8:9			Open	8:9
Open	9:10	Open	9:10						

*Factory-installed.

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-1, *then* make the changes in links LKB, LKC, and LKE in Table II-2 for the segments to be inhibited.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 10. For the relation of these sockets to memory address space, refer to Table IV.

Table II-2 — Linking Arrangements for 2716-Type EPROM
Inhibit Feature, Low-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
7000-77FF	XU-14		Open 7:12			
7800-7FFF	XU-18		Open 8:11			
7000-7FFF	XU-14 XU-18		Open 7:12 Open 8:11			
7000-73FF	XU-14			Open 2:15		Close 1:16 Close 7:10
7400-77FF	XU-14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
7800-7BFF	XU-18			Open 2:15		Close 1:16 Close 6:11
7C00-7FFF	XU-18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

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Table II-3 — Linking Arrangements for 2716-Type EPROM
No Inhibit Feature, High-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Open	1:16	Open	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Open	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	Open	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Open	4:5	Open	4:13
Closed	5:14	Closed	5:14	Closed	5:12			Open	5:12
Closed	6:13	Open	6:13	Closed	6:11			Open	6:11
Closed	7:12	Closed	7:12	Closed	7:10			Open	7:10
Closed	8:11	Closed	8:11	Closed	8:9			Open	8:9
Closed	9:10	Closed	9:10						

Note: Pin position 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-3, *then* make the changes in links LKB, LKC, and LKE as shown in Table II-4.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 10. For the relation of these sockets to memory address space, refer to Table IV.

Table II-4 — Linking Arrangements for 2716-Type EPROM
Inhibit Feature, High-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
F000-F7FF	XU-14		Open 7:12			
F800-FFFF	XU-18		Open 8:11			
F000-FFFF	XU-14, XU-18		Open 7:12 Open 8:11			
F000-F3FF	XU-14			Open 2:15		Close 1:16 Close 7:10
F400-F7FF	XU14			Open 2:15 Open 4:13		Close 1:16 Close 3:14 Close 7:10
F800-FBFF	XU-18			Open 2:15		Close 1:16 Close 6:11
FC00-FFFF	XU-18			Open 2:15 Open 4:13		Close 1:16 Close 3:14 Close 6:11

Table II-5 — Linking Arrangements for 2732-Type EPROM
No Inhibit Feature

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Closed	1:18	Open	1:18	Closed	1:16	Open	1:8	Open	1:16
Closed	2:17	Open	2:17	Closed	2:15	Open	2:7	Open	2:15
Closed	3:16	Open	3:16	Closed	3:14	Open	3:6	Open	3:14
Closed	4:15	Open	4:15	Closed	4:13	Open	4:5	Open	4:13
Closed	5:14	Open	5:14	Closed	5:12			Open	5:12
Closed	6:13	Open	6:13	Closed	6:11			Open	6:11
Closed	7:12	Open	7:12	Closed	7:10			Open	7:10
Closed	8:11	Open	8:11	Closed	8:9			Open	8:9
Closed	9:10	Open	9:10						

Note: Pin position 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-5, *then* make the changes in links LKA, LKC, and LKE as shown in Table II-6.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 10. For the relation of these sockets to memory address space, refer to Table IV.

Table II-6 — Linking Arrangements for 2732-Type EPROM
Inhibit Feature

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
E000-EFFF	XU14	Open 7:12				
F000-FFFF	XU18	Open 9:10				
E000-FFFF	XU14, XU18	Open 7:12 Open 9:10				
E000-E3FF	XU14			Open 2:15 Open 3:14		Close 1:16 Close 2:15 Close 7:10
E400-E7FF	XU14			Open 2:15 Open 3:14 Open 4:13		Close 1:16 Close 2:15 Close 7:10 Close 3:14
E800-EBFF	XU14			Open 2:15 Open 3:14 Open 4:13		Close 1:16 Close 2:15 Close 7:10 Close 4:13
EC00-EFFF	XU14			Open 2:15 Open 3:14 Open 4:13		Close 1:16 Close 2:15 Close 7:10 Close 5:12

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Table II-6 – Linking Arrangements for 2732-Type EPROM Inhibit Feature – Cont'd

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
F000-F3FF	XU18			Open 2:15 Open 3:14		Close 1:16 Close 2:15 Close 6:11
F400-F7FF	XU18			Open 2:15 Open 3:14 Open 4:13		Close 1:16 Close 2:15 Close 6:11 Close 3:14
F800-FBFF	XU18			Open 2:15 Open 3:14 Open 4:13		Close 1:16 Close 2:15 Close 6:11 Close 4:13
FC00-FFFF	XU18			Open 2:15 Open 3:14 Open 4:13		Close 1:16 Close 2:15 Close 6:11 Close 5:12

Table II-7 — Linking Arrangements for 2732-Type EPROM Inhibit Bank F

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
DIP Shunt*				DIP Shunt*					
Closed	1:18	Open	1:18	Closed	1:16	Open	1:8	Open	1:16
Closed	2:17	Open	2:17	Closed	2:15	Open	2:17	Open	2:15
Closed	3:16	Open	3:16	Closed	3:6	Open	3:6	Open	3:14
Closed	4:15	Open	4:15	Closed	4:13	Open	4:5	Open	4:13
Closed	5:14	Open	5:14	Closed	5:12			Open	5:12
Closed	6:13	Open	6:13	Closed	6:11			Open	6:11
Closed	7:12	Open	7:12	Closed	7:10			Open	7:10
Closed	8:11	Open	8:11	Closed	8:9			Open	8:9
Open	9:10	Open	9:10						

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

Table II-8 — Linking Arrangements for 6116-Type RAM
No Inhibit Feature, Low-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Closed	1:16	Closed	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Closed	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:15	Closed	3:6	Open	3:14
Open	4:15	Closed	4:13	Closed	4:13	Closed	4:5	Open	4:13
Open	5:14	Closed	5:14	Open	5:12			Open	5:12
Open	6:13	Closed	6:13	Open	6:11			Open	6:11
Open	7:12	Closed	7:12	Open	7:10			Open	7:10
Open	8:11	Closed	8:11	Open	8:9			Open	8:9
Open	9:10	Open	9:10						

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-8, *then* make the changes in links LKB, LKC, and LKE as shown in Table II-9.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 8. For the relation of these sockets to memory address space, refer to Table IV.

Table II-9 — Linking Arrangements for 6116-Type RAM
Inhibit Feature, Low-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
7000-77FF	XU-14		Open 7:12			
7800-7FFF	XU-18		Open 8:11			
7000-7FFF	XU-14 XU-18		Open 7:12 Open 8:11			
7000-73FF	XU-14			Open 2:15		Close 1:16 Close 7:10
7400-77FF	XU-14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
7800-7BFF	XU-18			Open 2:15		Close 1:16 Close 6:11
7C00-7FFF	XU-18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

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Table II-10 — Linking Arrangements for 6116-Type RAM
No Inhibit Feature, High-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Open	1:16	Closed	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Closed	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	Closed	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Closed	4:5	Open	4:13
Closed	5:14	Closed	5:14	Open	5:12			Open	5:12
Open	6:13	Open	6:13	Open	6:11			Open	6:11
Open	7:12	Closed	7:12	Open	7:10			Open	7:10
Open	8:11	Closed	8:11	Open	8:9			Open	8:9
Open	9:10	Closed	9:10						

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-10, *then* make the changes in links LKB, LKC, and LKE as shown in Table II-11.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 8. For the relation of these sockets to memory address space, refer to Table IV.

Table II-11 — Linking Arrangements for 6116-Type RAM
Inhibit Feature, High-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
F000-F7FF	XU-14		Open 7:12			
F800-FFFF	XU-18		Open 8:11			
F000-FFFF	XU-14, XU-18		Open 7:12 Open 8:11			
F000-F3FF	XU-14			Open 2:15		Close 1:16 Close 7:10
F400-F7FF	XU-14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
F800-FBFF	XU-18			Open 2:15		Close 1:16 Close 6:11
FC00-FFFF	XU-18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

Table II-12 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination No Inhibit Feature, Low-Half Address Space

LINK									
LKA Position		LKB Position		LKC Position		LKD Position		LKE Position	
Open	1:18	Closed	1:18	Closed	1:16	Link	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Positions	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	for RAM	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Selection	4:5	Open	4:13
Open	5:14	Closed	5:14	Link	5:12			Open	5:12
Open	6:13	Closed	6:13	Positions	6:11			Open	6:11
Open	7:12	Closed	7:12	for ROM	7:10			Open	7:10
Open	8:11	Closed	8:11	Selection	8:9			Open	8:9
Open	9:10	Open	9:10	*See Note Δ*		*See Note Δ*			

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

For mixing 2716-type ROM's and 6116-type RAM's, select the appropriate ROM/RAM link positions in links LKC and LKD. See Table below.

If ROM is selected for the given memory segment, close the appropriate link position on LKC and open the corresponding link position on LKD. If RAM is selected for the segment, close the appropriate link position on LKD and open the corresponding link position on LKC.

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position for ROM Selection	Position for RAM Selection	Position
0000-1FFF	XU1, XU6 XU11, XU15			5:12	1:8	
2000-3FFF	XU2, XU7 XU12, XU16			6:11	2:7	
4000-5FFF	XU3, XU8 XU13, XU17			7:10	3:6	
6000-7FFF	XU4, XU9 XU14, XU18			8:9	4:5	

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To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-12, *then* make the changes in links LKB, LKC, and LKE as shown in Table II-13.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 8. For the relation of these sockets to memory address space, refer to Table IV.

Table II-13 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination Inhibit Feature, Low-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
7000-77FF	XU14		Open 7:12			
7800-7FFF	XU18		Open 8:11			
7000-7FFF	XU14, XU18		Open 7:12 Open 8:11			
7000-73FF	XU14			Open 2:15		Close 1:16 Close 7:10
7400-77FF	XU14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
7800-7BFF	XU18			Open 2:15		Close 1:16 Close 6:11
7C00-7FFF	XU18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

Table II-14 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination No Inhibit Feature, High-Half Address Space

LINK									
LKA Position		LKB Position		LKC Position		LKD Position		LKE Position	
Open	1:18	Closed	1:18	Open	1:16	Link	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Positions	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	for RAM	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Selection	4:5	Open	4:13
Closed	5:14	Closed	5:14	Link	5:12			Open	5:12
Open	6:13	Open	6:13	Positions	6:11			Open	6:11
Open	7:12	Closed	7:12	for ROM	7:10			Open	7:10
Open	8:11	Closed	8:11	Selection	8:9			Open	8:9
Open	9:10	Closed	9:10	*See Note Δ Next Page*		*See Note Δ Next Page*			

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

△For mixing 2716-type ROM's and 6116-type RAM's, select the appropriate ROM/RAM link positions in links LKC and LKD. See Table below.

If ROM is selected for the given memory segment, close the appropriate link position on LKC and open the corresponding link position on LKD. If RAM is selected for the segment, close the appropriate link position on LKD and open the corresponding link position on LKC.

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position for ROM Selection	Position for RAM Selection	Position
8000-9FFF	XU1, XU6 XU11, XU15			5:12	1:8	
A000-BFFF	XU2, XU7 XU12, XU16			6:11	2:7	
C000-DFFF	XU3, XU8 XU13, XU17			7:10	3:6	
E000-FFFF	XU4, XU9 XU14, XU18			8:9	4:5	

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-14, *then* make the changes in links LKB, LKC, and LKE as indicated below.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 8. For the relation of these sockets to memory address space, refer to Table IV.

Table II-15 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination Inhibit Feature, High-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
F000-F7FF	XU14		Open 7:12			
F800-FFFF	XU18		Open 8:11			
F000-FFFF	XU14, XU18		Open 7:12 Open 8:11			
F000-F3FF	XU14			Open 2:15		Close 1:16 Close 7:10
F400-F7FF	XU14			Open 2:15 Open 4:13		Close 1:16 Close 3:14 Close 7:10
F800-FBFF	XU18			Open 2:15		Close 1:16 Close 6:11
FC00-FFFF	XU18			Open 2:15 Open 4:13		Close 1:16 Close 3:14 Close 6:11

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Table IV — Relation of Sockets to Memory Address Space for CDP18S626 COSMAC Microboard 32/64-kilobyte EPROM/ROM/RAM

Memory Address Space Selected		Socket
Low-Half	High-Half	
0000-07FF	8000-87FF	XU1
0800-0FFF	8800-8FFF	XU6
1000-17FF	9000-97FF	XU11
1800-1FFF	9800-9FFF	XU15
2000-27FF	A000-A7FF	XU2
2800-2FFF	A800-AFFF	XU7
3000-37FF	B000-B7FF	XU12
3800-3FFF	B800-BFFF	XU16
4000-47FF	C000-C7FF	XU3
4800-4FFF	C800-CFFF	XU8
5000-57FF	D000-D7FF	XU13
5800-5FFF	D800-DFFF	XU17
6000-67FF	E000-E7FF	XU4
6800-6FFF	E800-EFFF	XU9
7000-77FF	F000-F7FF	XU14
7800-7FFF	F800-FFFF	XU18

How To Use Linking Arrangement Tables to Mix RAM/ROM's

To determine the linking arrangements required for a 4-block 2716/6116-type RAM/ROM combination shown below using the high-half of address space (8000-FFFF), and the instructions shown on page 18 for mixing RAM/ROM's, proceed as follows:

8000-9FFF	2716 ROM	No. 1 Block
A000-BFFF	6116 RAM	No. 2 Block
C000-DFFF	6116 RAM	No. 3 Block
E000-FFFF	6116 RAM	No. 4 Block

If the 2716-type ROM is selected to fill the first block, that is, address space 8000-9FFF, the appropriate link position for ROMs on link LKC (5:12) must be closed, and the corresponding link position for RAMs on link LKD (1:8) must be open. (Similarly, if the first block contained RAMs and the second block ROMs, the linking arrangement would be — close 1:8 on Link LKD, open 5:12 on link LKC).

Complete the linking arrangements for the remaining blocks:

For No. 2 block (6116-type RAM) using address space A000-BFFF, close link position 2:7 on link LKD, open link position 6:11 on link LKC.

For No. 3 block (6116-type RAM) using address space C000-DFFF, close link position 3:6 on link LKD, open link position 7:10 on link LKC.

For No. 4 block (6116-type RAM) using address space E000-FFFF, close link position 4:5 on link LKD, open link position 8:9 on LKC.

See Table V for a summary of the required linking arrangements for this RAM/ROM combination.

Table V - Linking Arrangements for 2716/6116-Type ROM/RAM Combination

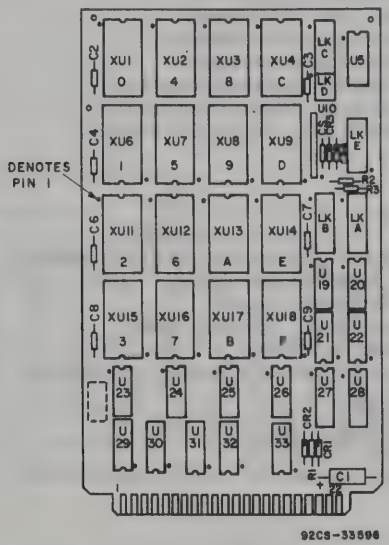
Memory Address Space and Socket		ROM/RAM Type Combination	Link Positions On Links LKD and LKC
Segment	Socket		
8000-9FFF	XU1, XU6 XU11, XU15	2716 ROM	Open 1:8 on LKD, Close 5:12 on LKC
A000-BFFF	XU2, XU7 XU12, XU16	6116 RAM	Close 2:7 on LKD, Open 6:11 on LKC
C000-DFFF	XU3, XU8 XU13, XU17	6116 RAM	Close 3:6 on LKD, Open 7:10 on LKC
E000-FFFF	XU4, XU9 XU14, XU18	6116 RAM	Close 4:5 on LKD, Open 8:9 on LKC

Installation in the COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III)

The RCA COSMAC Microboard CDP18S626 may be installed in the CDS II and CDS III in any memory slot 1 through 8. The following connections must be made: To supply the TPA signal, connect pins 1 and A of the selected slot on the CDS backplane. To supply the TPB signal, connect pin B on slot 12 to pin B on the selected slot on the CDS backplane. On the CDP18S005 (CDS II), it is also necessary to connect a wire from pin D on slot 10 to pin 3 on the selected slot. This last connection supplies the RNU signal. On the CDP18S626 Microboard a jumper must be connected between 8:9 on link LKE. The Microboard should be linked for the low half of address space. This arrangement permits use of the existing utility program in the CDS systems at address 8000.

Installation in COSMAC Microboard Computer Development Systems

When a CDP18S626 Microboard 32/64-Kilobyte EPROM/ROM/RAM is added to a Microboard Computer Development System, where the Monitor program is located at address space 8000, a jumper must be connected between pins 8 and 9 of link LKE to supply the RNU signal.



A hexadecimal number 0 through F is indicated on each of the 24-pin ROM/RAM socket locations. The numbers represent the ascending order of the socket addresses as shown in Table IV.

Note 1: Sockets LKC and LKB have factory-installed DIP Shunts. In socket LKB the DIP Shunt is justified to pin 1 leaving pin 9:10 unoccupied.

Fig. 8 - Layout Diagram of RCA COSMAC Microboard 32/64-Kilobyte EPROM/ROM/RAM CDP18S626.

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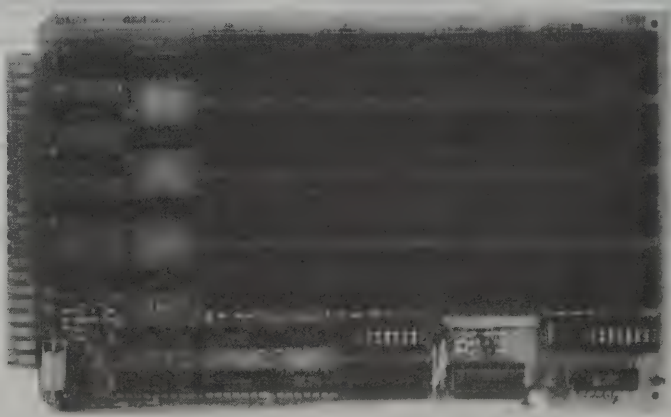
Parts List

C1 = 22 μF, 25 V
C2-C9 = 0.1 μF, 50 V
CR1-CR4 = 1N270
LKA, LKB = 18-pin DIP socket
LKC, LKE = 16-pin DIP socket
LKD = 8-pin DIP socket
LKC, LKB = 16-pin DIP SHUNT
(See Note, Fig. 8)
R1-R3 = 22 kilohms, 1/4 W, 5%
U5 = CD4556BE
U10 = resistor module, SIP, 10 kilohms
U19,U29 = CD4013BE
U20,U21 = CD4011BE
U22 = CD4068BE
U23-U26 = CD4071BE
U27, U28 = CDP1866CE
U30, U31 = CDP1856CE
U32, U33 = CD4050BE
XU1-XU4 = 24-pin DIP socket
XU6-XU9 = 24-pin DIP socket
XU11-XU18 = 24-pin DIP socket

Suggested Vendors for DIP SHUNT networks:
CTS KEENE, Inc.
3230 Riverside Avenue
Paso Robles, California, 93446
Order No. 198D-X
(X is the number of sections, 2 through 12)

AMP Inc.
Harrisburg, Pennsylvania, 17105
Order No. 435704-X
(X is the number of sections, 2 through 12)



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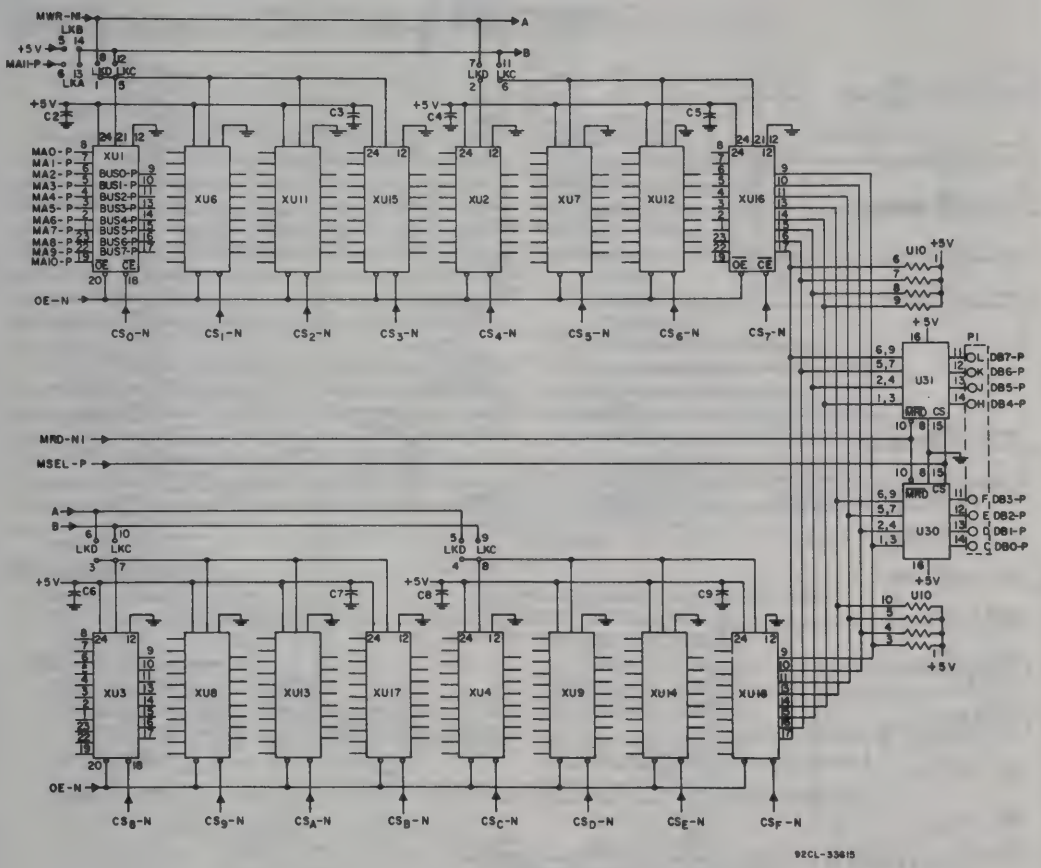

Fig. 9 - RCA COSMAC Microboard 32/64-Kilobyte EPROM/ROM/RAM CDP18S626 Logic Diagram — Memory Matrix Section.

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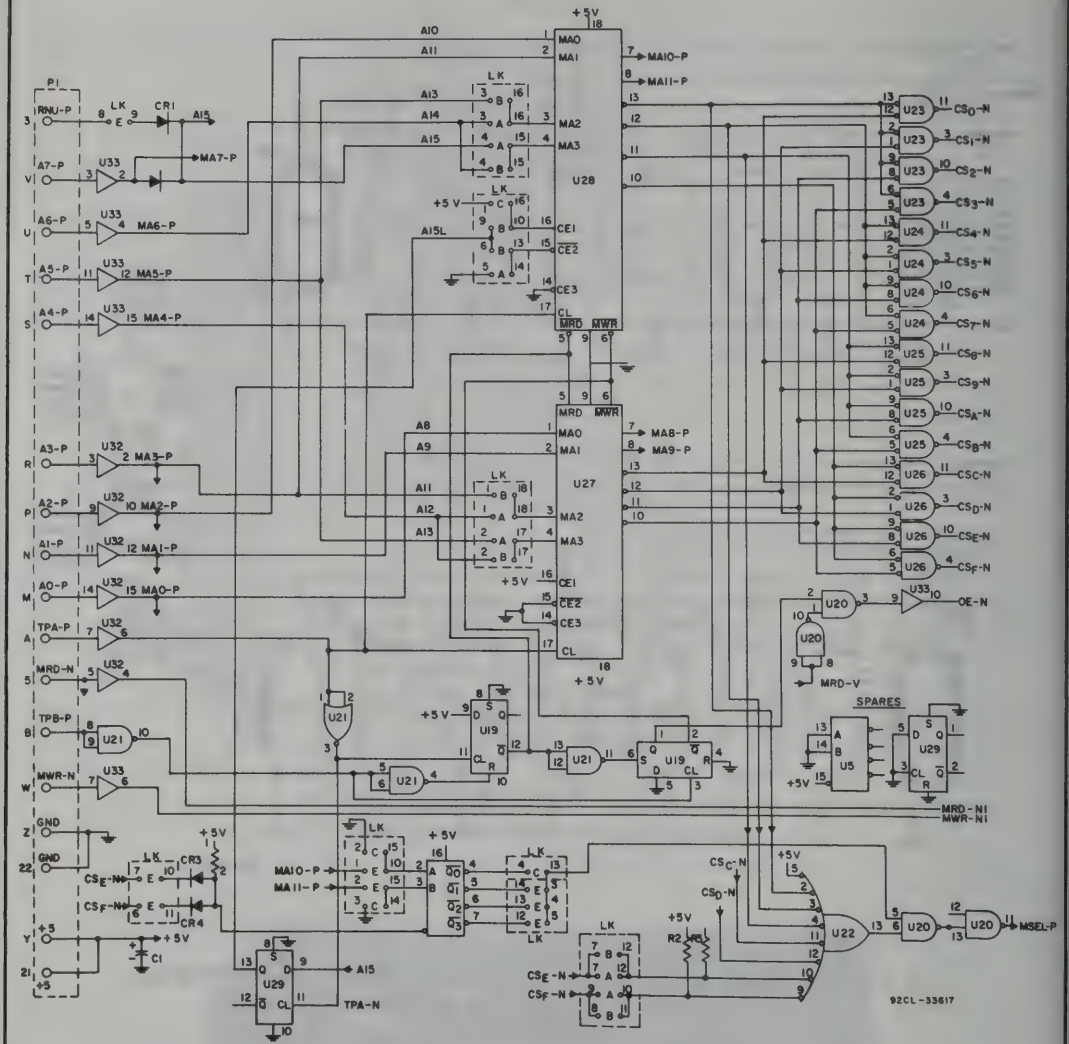

Fig. 10 - RCA COSMAC Microboard 32/64-Kilobyte EPROM/ROM/RAM CDP18S626 Logic Diagram — Memory Decoding Section.

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RCA COSMAC Microboard 4-Kilobyte CMOS EPROM

The RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627 is a memory module having on-board address latches and decoders and an on-board EPROM programmer. The sixteen 24-pin sockets provided permit the easy interchange of user-supplied CDP18U42 CMOS EPROM's. An Erase Verify mode is provided to insure the complete erasure of an EPROM prior to its programming. Address lines and data lines are buffered to minimize loading of the Microboard bus interface.

The CDP18S627 can be configured by means of a four-rocker binary-encoded DIP switch to accupy any even 4-kilobyte block in the 64-kilobyte memory system space. Each socket has a unique, fixed, 256-byte address within the 4-kilobyte board space. Any number of sockets from 1 to 16 may be populated, but the board always preempts the whole of its assigned 4-kilobyte address space.

Features

- **Low-power static CMOS**
- **High noise immunity**
- **Operable from single 5-volt supply (READ mode)**
- **Fully buffered**
- **Three modes of operation:**
  - **Read**
  - **Erase Verify**
  - **Program**
- **Flexible address assignment**
- **Temperature Range - -40° C to +85° C**
- **Simple system interface**
- **Small board size - (4.5 x 7.5 inches)**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Compatible with COSMAC Development Systems**
- **Member of extensive Microboard family**

Specifications

Memory Capacity

4096 bytes (16 sockets accepting CDP18U42 CMOS EPROM's).

Memory Addressing

Switch selectable board address

Board can occupy any contiguous 4-kilobyte block on any 4-kilobyte boundary within the 64-kilobyte address space.

Operating Temperature Range

-40° C to +85° C.

Power Requirements

+5 volts at 6 milliamperes typical, operating at 2.5-MHz system clock and using sixteen CDP18U42 CMOS EPROM's.

+22 volts ± 1 volt at 8 milliamperes typical for programming.

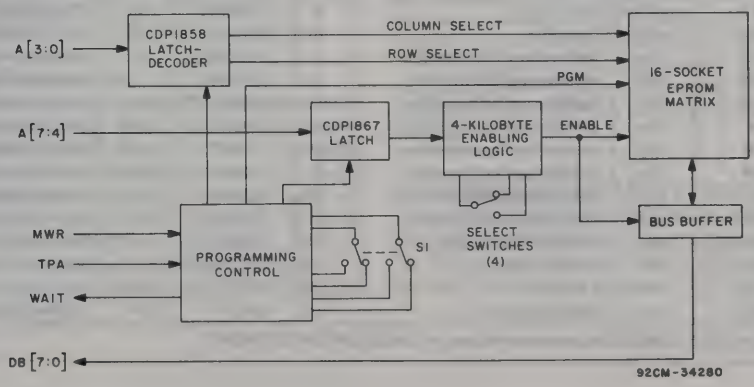


Fig. 1 - Block diagram of RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627.

CDP18S627

Programming Time
Approximately 41 seconds for entire board (4 kilobytes).

Dimensions
4.5 x 7.5 inches (114.3 x 190.5 mm).
Board pitch 0.5-inch (12.7 mm) minimum.

Connector
System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers.
Programming voltage: two jacks, E.F. Johnson No. 105-0757-001 or equivalent;
two mating plugs, E.F. Johnson No. 105-0777-001, provided with CDP18S627.

Microboard Bus Interface Signals Connector P1

The following signals are generated or received by the RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627. For additional information on these signals, refer to the published data for the CDP1802A COSMAC Microprocessor (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.** These signals are summarized in Table I which gives a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). These signals are discussed below. The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard CDP18S627.

A7 through A0 - Memory address bus on which the high- and low-order address bytes are multiplexed. These signals are wired to a CDP1852CE (U12,U14) 8-bit latch. The address lines are fed through during a read operation and latched during a write operation. The outputs from the CDP1852CE are wired to each EPROM socket for the low-address byte which becomes stable after TPA.

Bits 3 through 0 (A3 through A0) are latched in a CDP1858CE (U10), 4-bit latch with decode, at the trailing edge of TPA. Bits 0 and 1 are decoded into four chip select lines labeled CS0-P through CS3-P. Bits 2 and 3 are decoded into four chip

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P *	In/Out	Data Bus	3	RNU-P *	—	Run Utility
D	DB1-P *	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N*	In	Clear-Mode Control
L	DB7-P *	In/Out	Data Bus	10	WAIT-N *	In	Wait-Mode Control
M	A0-P *	Out	Multiplexed Address Bus	11	-5 V/-15 V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N*	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

*Signals used on RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627.

enable lines labeled CE0-N through CE3-N. These eight lines are wired to the EPROM socket matrix to uniquely select the proper EPROM socket.

Bits 7 through 4 (A7 through A4) are latched into a CDP1867CE (U19), 4-bit latch and decoder memory interface, at the trailing edge of TPA. These bits are compared with the setting of the four DIP switch rockers. When they are equal the board is enabled.

DB7 through DB0 - Eight bidirectional data lines. Taken from the Microboard Universal Backplane and interfaced through two CDP1856CE (U15,U16) bus buffer/separators, these lines transfer the data between the CPU and the EPROM's on the board.

$\overline{\text{MRD}}$ - A Read command from the CPU to the memories. When true, $\overline{\text{MRD}}$ indicates data will be read from memory. $\overline{\text{MRD}}$ must be used to condition output drivers in all memory components or the output buffers to avoid contention on the data bus.

$\overline{\text{MWR}}$ - A Write command from the CPU to the memories. Address lines are stable at this time.

TPA - A timing pulse generated by the CPU which occurs once in each machine cycle. The trailing edge of TPA is used to latch the high-order memory address.

RNU - Run Utility Software. This signal is supplied to force the most significant address bit true. As a result, the program start is at memory location 8000 (hexadecimal notation) instead of 0000.

$\overline{\text{WAIT}}$ (also referred to as EX WAIT-OP) - Wait or Pause signal to the CPU. Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate but subsequent clock transitions are ignored. This signal is used to halt the CPU when EPROM's are being programmed on the board.

$\overline{\text{CLEAR}}$ (also referred to as RESET-OP) - Reset signal. This input signal is used to reset the on-board programming circuitry.

Modes of Operation

The RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627 has three modes of operation, ERASE VERIFY, PROGRAM, and READ. The modes selection switch (S1) is used to select the desired mode. The ERASE VERIFY and PROGRAM modes are selected when S1 is in the position labeled PROGRAM/ERASE VERIFY. The READ mode is selected when S1 is in the position labeled READ.

The CDP18S627 is designed to use CDP18U42 (256-word x 8-bit) CMOS EPROM's. These EPROM's erase to an all zero state, that is, all locations should contain 00 when erasure is complete. The ERASE VERIFY mode is used to verify total erasure. In this mode, a weak zero (a location not completely erased) will be read as a one. This mode may be used with or without the programming voltage present, and is best done just prior to programming.

The PROGRAM mode is used to program EPROM's on the board. In this mode, writing to the board will program the selected EPROM(s). On-board circuitry takes care of all timing requirements. The $\overline{\text{WAIT}}$ line is used to halt CPU operations when a location is being programmed. A recommended way to program EPROM's on the board is to use any COSMAC UTILITY program. The EPROM's can be programmed from the terminal, directly from a floppy disk, or by moving a block of code already in memory to the address space selected for the CDP18S627. [Note: The user must apply a programming voltage (22 V $\pm$ 1 V) across connectors J1 and J2.]

The READ mode is used when programming is complete. Placing the board in this mode disables the programming circuitry. Read operations can be performed but write operations are ignored.

Address Selection

The RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627 can be configured to occupy any even 4-kilobyte block in the 64-kilobyte memory system space. The desired combination of the four high-order address bits (A12, A13, A14, and A15) should be set in the binary-encoded four-rocker DIP switch (S2). Looking at the DIP switch with the rocker numbers on the top of the switch, the up position of the rocker selects a one and the down position selects a zero. The least significant bit is controlled by rocker 1. Thus, with rocker 1 in the up position and rockers 2, 3, and 4 in the down position, the 4-kilobyte block 1000-1FFF is selected. Table II gives the board address space as a function of the rocker position.

The physical address map of the on-board memory matrix is given in Table III. This table is used to identify the address space of a particular EPROM socket on the board.

Installation in a Microboard System

The RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627 may be installed in any position in the 5-Card Microboard Chassis (CDP18S675), in the 22-Card Microboard Chassis (CDP18S670), or in any

CDP18S627

Table II - Board Address Space as a Function of Rocker Position

Board Address Space	Rocker 1	Rocker 2	Rocker 3	Rocker 4
0000-0FFF	Down	Down	Down	Down
1000-1FFF	Up	Down	Down	Down
2000-2FFF	Down	Up	Down	Down
3000-3FFF	Up	Up	Down	Down
4000-4FFF	Down	Down	Up	Down
5000-5FFF	Up	Down	Up	Down
6000-6FFF	Down	Up	Up	Down
7000-7FFF	Up	Up	Up	Down
8000-8FFF	Down	Down	Down	Up
9000-9FFF	Up	Down	Down	Up
A000-AFFF	Down	Up	Down	Up
B000-BFFF	Up	Up	Down	Up
C000-CFFF	Down	Down	Up	Up
D000-DFFF	Up	Down	Up	Up
E000-EFFF	Down	Up	Up	Up
F000-FFFF	Up	Up	Up	Up

Down=0 Up=1

other Chassis utilizing the RCA COSMAC Universal Backplane. The board comes prelinked so that no link changes are required. Table IV summarizes the required link connections.

Installation in the COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III)

The RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627 may be installed in a CDS system in any memory slot (slots 1 through 8 of the CDS backplane) with the following link connections made on the board.

For the WAIT line, LK1 2:7 must be closed
LK1 1:8, 3:6, and 4:5 must be open
For the TPA line, LK2 3:6 must be closed
LK2 1:8 and 2:7 must be open
For the RNU line, LK2 4:5 must be closed (only if board is to reside at location 0000)
For the RESET line, LK3 2:3 must be closed
LK3 1:4 must be open

No Bank Select wiring is required on the backplane. If the board is to reside at location 0000, however, the RNU-P signal must be connected to the memory section of the backplane by a jumper from pin D of CDS slot 10 to pin 3 of any memory slot (slots 1 through 8). Table IV summarizes the required link connections.

Table III - Physical Address Map of the On-board Memory Matrix

Chip Address Space	EPROM Socket Number
X000-X0FF	U1A
X100-X1FF	U2A
X200-X2FF	U3A
X300-X3FF	U4A
X400-X4FF	U1B
X500-X5FF	U2B
X600-X6FF	U3B
X700-X7FF	U4B
X800-X8FF	U1C
X900-X9FF	U2C
XA00-XAFF	U3C
XB00-XBFF	U4C
XC00-XCFF	U1D
XD00-XDFF	U2D
XE00-XEFF	U3D
XF00-XFFF	U4D

X=Don't Care

Table IV - Required LINK Connections

LINK	Microboard System	CDS II or III System
LK1 (WAIT line link)		
1:8	CLOSED*	OPEN
2:7	OPEN*	CLOSED
3:6[2]	OPEN*	OPEN*
4:5[2]	OPEN*	OPEN*
LK2 (RNU and TPA link)		
1:8	OPEN*	OPEN*
2:7	CLOSED*	OPEN
3:6	OPEN*	CLOSED
4:5	CLOSED*[1]	CLOSED*[1]
LK3 (RESET link)		
1:4	CLOSED*	OPEN
2:3	OPEN*	CLOSED

*Indicates state of link connections when the board is shipped.
[1]If the RNU-P signal is being used and this board is to reside at location 0000, this link must be closed. The board is shipped with this link connection closed.
[2]Pins 3:6 and 4:5 of link LK1 provide additional programming pulse width. This feature is not required, and these pins may be ignored.

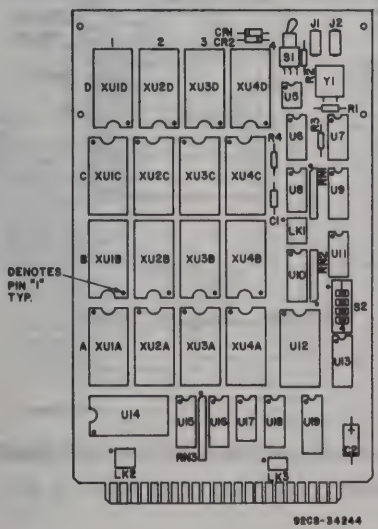


Fig. 2 - Layout diagram of RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627.

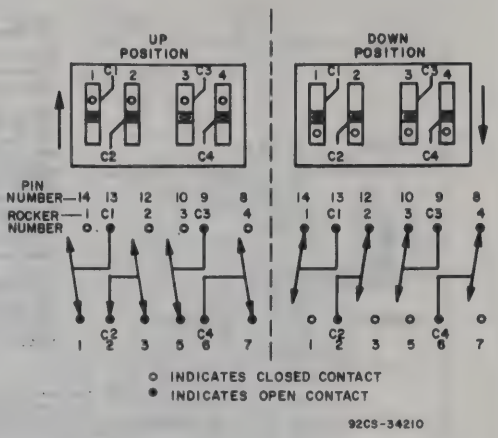


Fig. 1 - Typical circuit diagram of rocker switch (Top View).

Parts List

C1=0.1 μF, 50 V
C2=22 μF, 25 V
C3, C4=22 pF, 100 V
CR1=1N914
CR2=1N270
R1=22 MΩ, ¼W
R2=18 kΩ, ¼W
R3=3.9 kΩ ¼W
R4=22 kΩ, ¼W
RN1, RN2=Resistor Module, SIP, 8-Pin, 22 kΩ
RN3=Resistor Module, SIP, 10-Pin, 22 kΩ
S1=Switch, Toggle, Subminiature, DPDT
S2=Switch, 4-Position DIP, SPDT
U5=CA3140E
U6=CD4024BE
U7, U11=CD4013BE
U8=CD4066BE
U9=CD40103BE
U10=CDP1858CE
U12, U14=CDP1852CE
U13=CD4049UBE
U15, U16=CDP1856CE
U17=CD4001UBE
U18=CD4050BE
U19=CDP1867CE
XU1A-XU4D=24-Pin DIP Socket
Y1=Crystal, 2.0000 MHz

CDP18S627

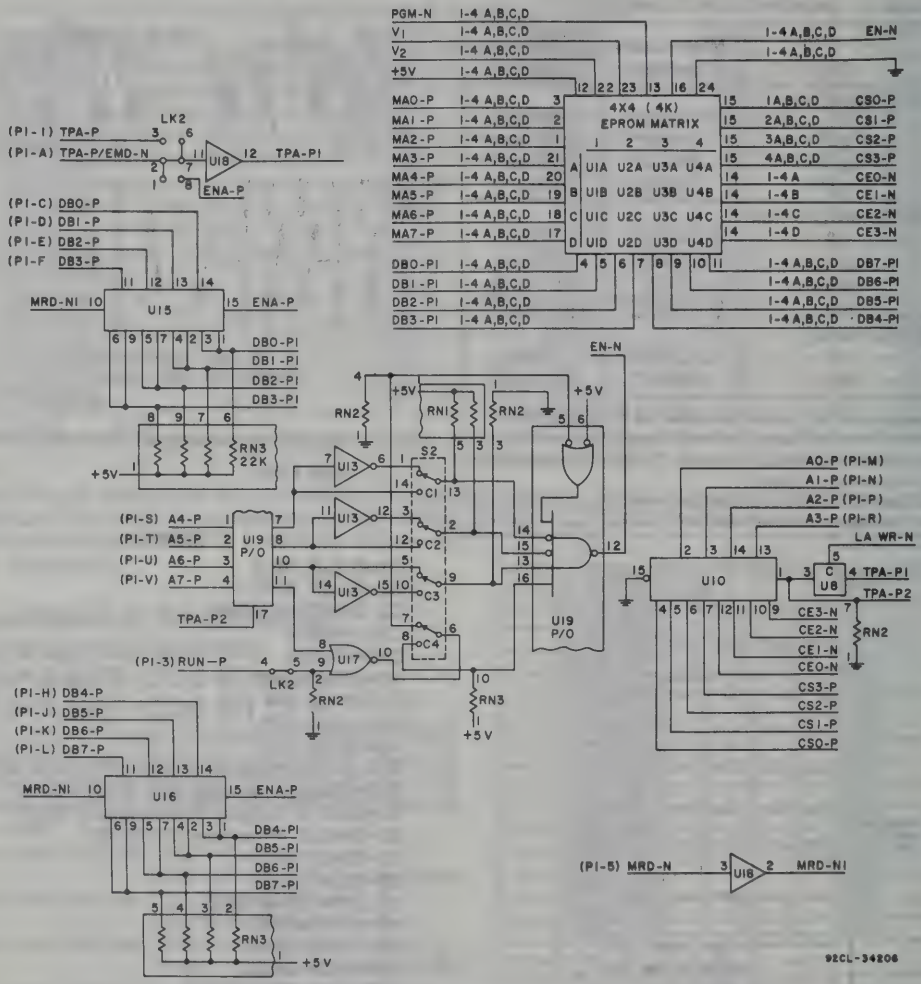


Fig. 3 - Logic diagram for RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627.

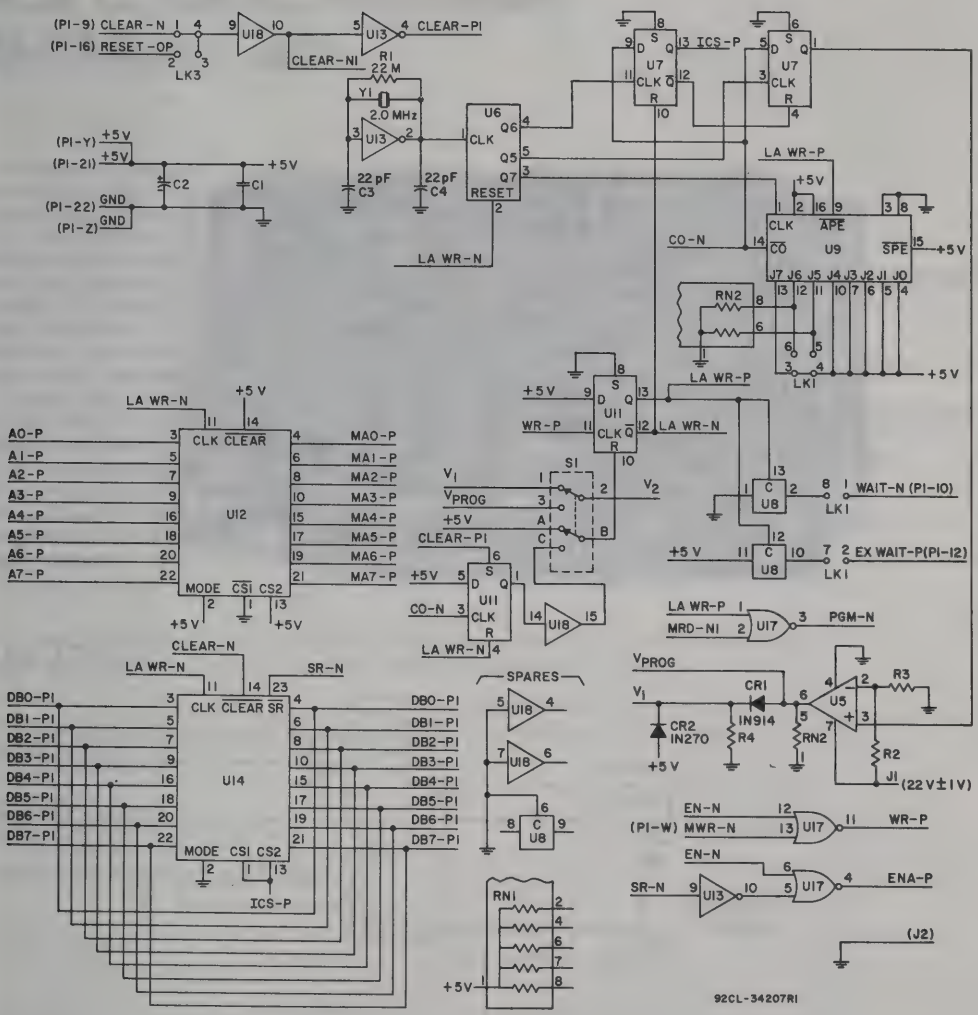
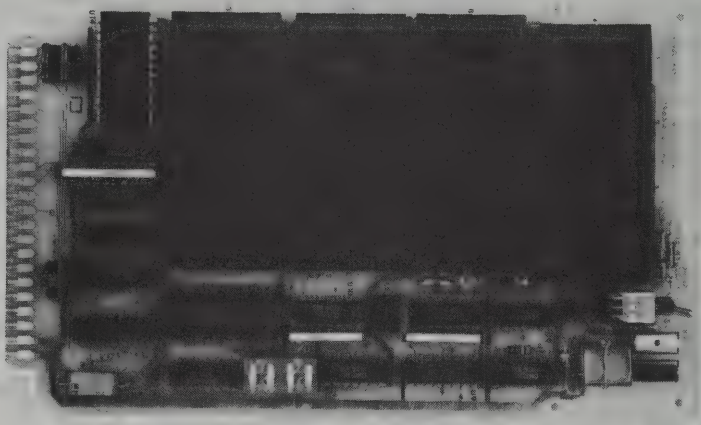


Fig. 4 - Logic diagram for RCA COSMAC Microboard 4-Kilobyte CMOS EPROM CDP18S627.

CDP18S627



CDP18S629

RCA COSMAC Microboard 32-Kilobyte RAM

The RCA COSMAC Microboard 32-kilobyte RAM CDP18S629 is a memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The CDP18S629 contains 16 24-pin sockets populated with 2K x 8 static RAM's providing 32 kilobytes of contiguous static RAM in either high-or-low half of memory space. These sockets or any portion of them in blocks of four may be populated by user-supplied ROM's instead of RAM's to provide any of sixteen different combinations of ROM/EPROM and RAM. The CDP18S629 also includes inhibit features which make it possible to inhibit 1-, 2-, or 4-kilobyte segments in contiguous memory space in certain banks as shown in the Memory Maps in Figs. 2 and 3. The CDP18S629 Microboard is preprogrammed for the low-half of address space, with no inhibit features.

Features

- **Low-power static CMOS**
- **Operable from single 5-volt supply**
- **Small size (4.5 x 7.5 inches)**
- **Compatible with COSMAC Development Systems**
- **Fully buffered**
- **High noise immunity**
- **Flexible address assignment**
- **Member of extensive Microboard family**
- **Simple system interface**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Temperature range — -40°C to +85°C**

Specifications

Memory Capacity

32,768 bytes - 16 CMOS static RAM's 6116 type, 2048 x 8

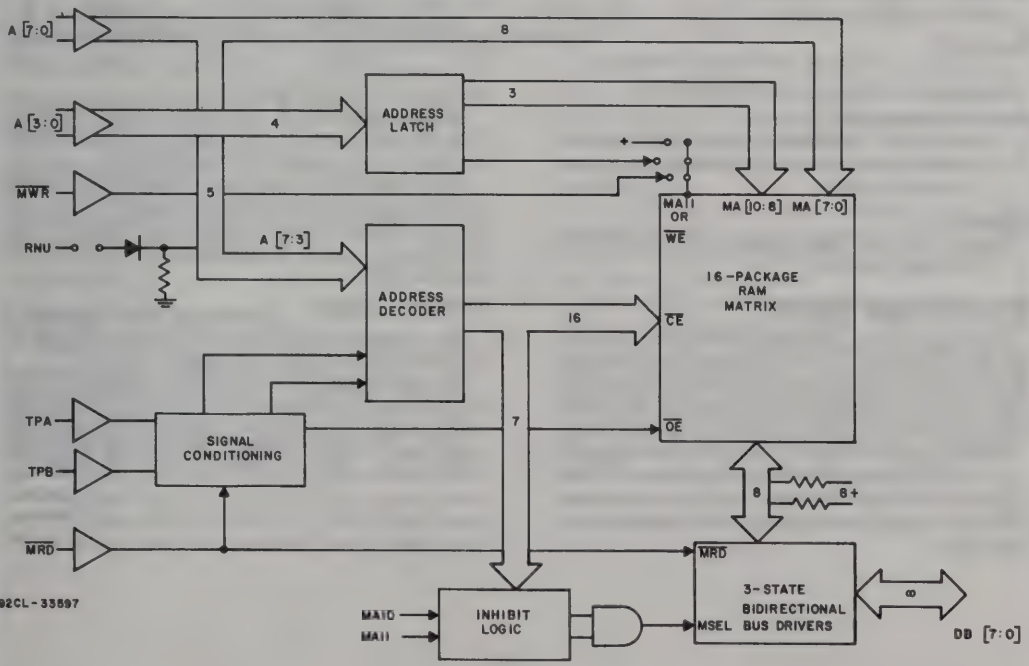


Fig. 1 — RCA COSMAC Microboard 32-Kilobyte RAM CDP18S629 Block Diagram.

CDP18S629

32,768 bytes - Combination of EPROM/ROM 2716 (user supplied) and CMOS static RAM 6116. Four 8-kilobyte blocks each of which can be assigned to the 6116 or 2716 types for a total of 16 different combinations.

Memory Addressing

6116 type - Contiguous 32,768 bytes in low-or-high address space. Factory-installed DIP shunts place the CDP18S629 in the low-half of address space.

2716/6116 Combination - Contiguous 32,768 bytes in low-or-high address space.

Memory Inhibit

EPROM or RAM	Programmable Inhibit Address Space	
	Low-Half	High-Half
6116-Type RAM or 2716-Type EPROM/ 6116-Type RAM combination	7000-77FF	F000-F7FF
	or 7800-7FFF	or F800-FFFF
	or 7000-7FFF	or F000-FFFF
	or 7000-73FF	or F000-F3FF
	or 7400-77FF	or F400-F7FF
	or 7800-7BFF	or F800-FBFF
	or 7C00-7FFF	or FC00-FFFF

Operating Temperature Range

–40° C to +85° C

Dimensions

4.5 inches x 7.5 inches (114.3 mm x 190.5mm). Board pitch 0.5 inch (12.7 mm minimum).

Power Requirements

+5 volts at 27 milliamperes typical operating at 2-MHz system clock and populated with sixteen 6116-type RAM's

Connector

System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers.

Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 32-kilobyte RAM CDP18S629. These signals are discussed below.

A7 through A0 — Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each memory device for the low-address byte, which becomes stable after TPA.

When a 2048 x 8 memory device (2716-type EPROM or 6116-type RAM) is used, high-or-low address space is selected by latching bit A7 with TPA and using the appropriate links to link the output to chip enable on U28. Bits 6 and 5 are then linked to Latch-Decoder U28. Each of the four outputs of U28 decodes an 8-kilobyte block. Bits 4 and 3 are linked to Latch-Decoder U27, where each of the four outputs decodes a 2-kilobyte segment of each 8-kilobyte block. The outputs of the two one-of-four decoders are ORed to provide 16 chip selects for decoding of sixteen 2-kilobyte memory blocks in high- or low-address space.

DB7 through DB0 — These **Data Bus** lines are bidirectional and are interfaced through two CDP-1856C 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a memory select signal. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted *to* the Microboard interface bus; when MRD is false, data bits are transmitted *from* the Microboard interface bus.

MRD-Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the chip-select decoders.

MWR-Memory Write. This signal is buffered. It conditions each RAM chip and the chip-select decoders and is the write command.

TPA-Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866C (U28 and U27) and CD4013B (U29) latches. Latching takes place at the TPA trailing edge.

TPB-Timing Pulse B. This signal is used to condition the output enable (OE) signal for the memory devices, in order to avoid bus contention.

RNU-Run Utility. This signal, through pins 8 and 9 on link LKE, forces execution of a program to start at address 8000 (hexadecimal notation). This feature allows the user to put an on-board utility program at location 8000.

Inhibit Logic

For addresses of the "holes" that can be inserted in the Memory Maps, refer to Figures 2 and 3.

In order to enable the Bus Buffer/Separators with MSEL, one of the inputs to NAND gate U22 must be in the active low state. For example, if high-address-space bank F800-FFFF must be inhibited open link LKB between pins 8 and 11. Opening link LKB between pins 7 and 12 inhibits the next lower address space bank (F000-F7FF). If link LKB is open between pins 8 and 11 and between pins 7 and 12, the entire

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P *	In/Out	Data Bus	3	RNU-P *	—	Run Utility
D	DB1-P *	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N*	In	Clear-Mode Control
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Control
M	A0-P *	Out	Multiplexed Address Bus	11	_5 V/_15 V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N*	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

*Signals used on RCA COSMAC Microboard 32-Kilobyte RAM CDP18S629.

address range (F000-FFFF) is inhibited. If only 1-kilobyte "holes" within either bank are required, decoder U5 and links on LKE and LKC must be programmed while links on LKB between pins 7:12 and 8:11 remain closed. One of the four decoder outputs selects the 1-kilobyte segment to be inhibited within the two banks, when the appropriate bank F800-FFFF or F000-F7FF is first selected by linking pins 6:11 or 7:10 on LKE.

Linking Arrangements

Tables II-1 through II-8 provide the required links for combinations of memory types and memory space allocation. These tables also provide the means for inhibiting access within the "holes" in memory space which may be occupied by memory on other boards.

Links are arranged in groups called LKA, LKB, LKC, LKD, and LKE. These groups are arranged in the DIP (dual-in-line package) configuration to mate with the DIP sockets mounted on the Microboard. These links can be programmed by the use of the DIP SHUNT devices.

Table III lists the modes of operation for the CDP18S629 and the memory types which can be used with this Microboard. All 8 options are summarized in the tables II-1 through II-8.

For example, if inhibit features are desired for the 6116-type RAM proceed as follows: First, set up links LKA, LKB, LKC, LKD, and LKE as required for full address space (no inhibit). To inhibit segment (7800-7BFF) make the required changes as shown in Table II-2 as follows. Leave links LKA, LKB, and LKD as is, open links 2:15 on LKC, and close links 1:16 and 6:11 on LKE.

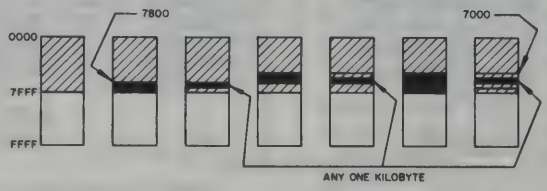
CDP18S629

Table III — Modes of Operation for the CDP18S629 Microboard

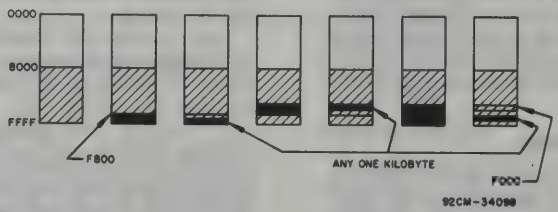
Table	Memory		Address Space		Inhibit Feature	
	Class	Type	Low-Half	High-Half		
RAM						
II-1*	RAM	6116	0000-7FFF	—	—	NO
II-2	RAM	6116	0000-7FFF	—	YES	—
II-3	RAM	6116	—	8000-FFFF	—	NO
II-4	RAM	6116	—	8000-FFFF	YES	—
EPROM/RAM Combination						
II-5	2716/6116		0000-7FFF	—	—	NO
II-6	2716/6116		0000-7FFF	—	YES	—
II-7	2716/6116		—	8000-FFFF	—	NO
II-8	2716/6116		—	8000-FFFF	YES	—

*Factory option, See Fig. 4.

1. Using the 6116-type RAM
   (a) Low-Half Address Space



   (b) High-Half Address Space

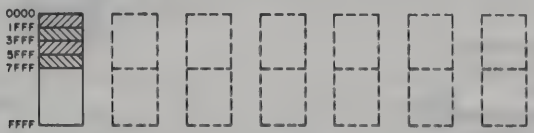


Note: Cross-Hatched Area Indicates Address Range Covered, Black Areas Indicate Programmable Inhibit Area

Fig. 2 — Memory Maps.

2. Using the 2716-type EPROM and the 6116-type RAM
(a) Low-Half Address Space

16 Different Combinations of 8-kilobyte Blocks of 2716-type EPROM and 6116-type RAM
Each 8-kilobyte segment may be filled with either a 2716-type EPROM or a 6116-type RAM



92CM-34097

1-kilobyte and 2-kilobyte segments between 7000 and 7FFF can be inhibited similarly as shown under 1(a).

Using the 2716-type EPROM and the 6116-type RAM
(a) High-Half Address Space

16 Different Combinations of 8-kilobyte Blocks of 2716-type EPROM and 6116-type RAM
Each 8-kilobyte segment may be filled with either a 2716-type EPROM or a 6116-type RAM

92CS-34093

1-kiloybte and 2-kilobyte segments between F000 and FFFF can be inhibited similarly as shown under 1(b)

Note: Cross-Hatched Area Indicates Address Range Covered

Fig. 3 — Memory Maps

CDP18S629

LKA: Leave Open
LKB: Install unprogrammed
8-Section DIP Shunt
(9:10 Is Open)
LKC: Install unprogrammed
4-Section DIP Shunt
(5:12, 6:11, 7:10, 8:9 Are Open)
LKD: Install unprogrammed
4-Section DIP Shunt
LKE: Leave Open

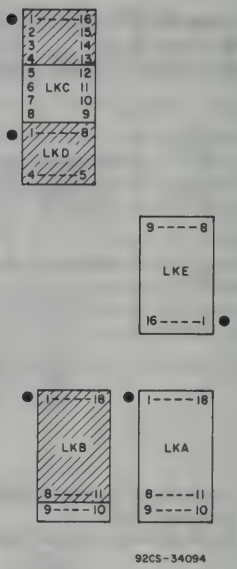


Fig. 4 — Linking Arrangements for RAM 6116
(Addressable Range 0000 to 7FFF. No Inhibit Features)

Table II-1 — Linking Arrangements for 6116-Type RAM
No Inhibit Feature, Low-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Closed	1:16	Closed	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Closed	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:15	Closed	3:6	Open	3:14
Open	4:15	Closed	4:13	Closed	4:13	Closed	4:5	Open	4:13
Open	5:14	Closed	5:14	Open	5:12			Open	5:12
Open	6:13	Closed	6:13	Open	6:11			Open	6:11
Open	7:12	Closed	7:12	Open	7:10			Open	7:10
Open	8:11	Closed	8:11	Open	8:9			Open	8:9
Open	9:10	Open	9:10						

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

Table II-2 — Linking Arrangements for 6116-Type RAM Inhibit Feature, Low-Half Address Space

To inhibit the various memory spaces shown in Table II-2, *first* setup the link positions as shown in Table II-1, *then* make the changes in links LKB, LKC, and LKE in Table II-2 for the segments to be inhibited.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 7. For the relation of these sockets to memory address space, refer to Table IV.

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
7000-77FF	XU-14		Open 7:12			
7800-7FFF	XU-18		Open 8:11			
7000-7FFF	XU-14 XU-18		Open 7:12 Open 8:11			
7000-73FF	XU-14			Open 2:15		Close 1:16 Close 7:10
7400-77FF	XU-14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
7800-7BFF	XU-18			Open 2:15		Close 1:16 Close 6:11
7C00-7FFF	XU-18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

Table II-3 — Linking Arrangements for 6116-Type RAM No Inhibit Feature, High-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Open	1:16	Closed	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Closed	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	Closed	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Closed	4:5	Open	4:13
Closed	5:14	Closed	5:14	Open	5:12			Open	5:12
Open	6:13	Open	6:13	Open	6:11			Open	6:11
Open	7:12	Closed	7:12	Open	7:10			Open	7:10
Open	8:11	Closed	8:11	Open	8:9			Open	8:9
Open	9:10	Closed	9:10						

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

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Table II-4 — Linking Arrangements for 6116-Type RAM Inhibit Feature, High-Half Address Space

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-3, *then* make the changes in links LKB, LKC, and LKE as shown in Table II-4.

For the physical location of the XU-Series sockets referred to in the table below, see Fig. 7. For the relation of these sockets to memory address space, refer to Table IV.

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
F000-F7FF	XU-14		Open 7:12			
F800-FFFF	XU-18		Open 8:11			
F000-FFFF	XU-14, XU-18		Open 7:12 Open 8:11			
F000-F3FF	XU-14			Open 2:15		Close 1:16 Close 7:10
F400-F7FF	XU14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
F800-FBFF	XU-18			Open 2:15		Close 1:16 Close 6:11
FC00-FFFF	XU-18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

Table II-5 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination No Inhibit Feature, Low-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Closed	1:16	Link	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Positions	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	for RAM	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Selection	4:5	Open	4:13
Open	5:14	Closed	5:14	Link	5:12			Open	5:12
Open	6:13	Closed	6:13	Positions	6:11			Open	6:11
Open	7:12	Closed	7:12	for ROM	7:10	*See Table* II-6		Open	7:10
Open	8:11	Closed	8:11	Selection	8:9			Open	8:9
Open	9:10	Open	9:10	*See Table* II-6					

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

For mixing 2716-type ROM's and 6116-type RAM's, select the appropriate ROM/RAM link positions in links LKC and LKD. See Table II-6.

If ROM is selected for the given memory segment, close the appropriate link position on LKC and open the corresponding link position on LKD. If RAM is selected for the segment, close the appropriate link position on LKD and open the corresponding link position on LKC.

Table II-5 – Linking Arrangements for 2716/6116-Type ROM/RAM Combination No Inhibit Feature, Low-Half Address Space (Cont'd)

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position for ROM Selection	Position for RAM Selection	Position
0000-1FFF	XU1, XU6 XU11, XU15			5:12	1:8	
2000-3FFF	XU2, XU7 XU12, XU16			6:11	2:7	
4000-5FFF	XU3, XU8 XU13, XU17			7:10	3:6	
6000-7FFF	XU4, XU9 XU14, XU18			8:9	4:5	

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-5, *then* make the changes in links LKB, LKC, and LKE as indicated below.

For the physical location of the XU-Series sockets referred to in the tables below, see Fig. 7. For the relation of these sockets to memory address space, refer to Table IV.

Table II-6 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination Inhibit Feature, Low-Half Address Space

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
7000-77FF	XU14		Open 7:12			
7800-7FFF	XU18		Open 8:11			
7000-7FFF	XU14 XU18		Open 7:12 Open 8:11			
7000-73FF	XU14			Open 2:15		Close 1:16 Close 7:10
7400-77FF	XU14			Open 2:15 Open 4:13		Close 1:16 Close 7:10 Close 3:14
7800-7BFF	XU18			Open 2:15		Close 1:16 Close 6:11
7C00-7FFF	XU18			Open 2:15 Open 4:13		Close 1:16 Close 6:11 Close 3:14

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Table II-7 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination No Inhibit Feature, High-Half Address Space

LINK									
LKA		LKB		LKC		LKD		LKE	
Position		Position		Position		Position		Position	
Open	1:18	Closed	1:18	Open	1:16	Link	1:8	Open	1:16
Open	2:17	Closed	2:17	Closed	2:15	Positions	2:7	Open	2:15
Open	3:16	Closed	3:16	Closed	3:14	for RAM	3:6	Open	3:14
Open	4:15	Closed	4:15	Closed	4:13	Selection	4:5	Open	4:13
Closed	5:14	Closed	5:14	Link	5:12			Open	5:12
Open	6:13	Open	6:13	Positions	6:11			Open	6:11
Open	7:12	Closed	7:12	for ROM	7:10			Open	7:10
Open	8:11	Closed	8:11	Selection	8:9	*See Table below*		Open	8:9
Open	9:10	Closed	9:10	*See Table below*					

Note: Pin positions 8:11 on link LKA are unused, and are, therefore, "don't-care" conditions.

For mixing 2716-type ROM's and 6116-type RAM's, select the appropriate ROM/RAM link positions in links LKC and LKD. See Table below.

If ROM is selected for the given memory segment, close the appropriate link position on LKC and open the corresponding link position on LKD. If RAM is selected for the segment, close the appropriate link position on LKD and open the corresponding link position on LKC.

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position for ROM Selection	Position for RAM Selection	Position
8000-9FFF	XU1, XU6 XU11, XU15			5:12	1:8	
A000-BFFF	XU2, XU7 XU12, XU16			6:11	2:7	
C000-DFFF	XU3, XU8 XU13, XU17			7:10	3:6	
E000-FFFF	XU4, XU9 XU14, XU18			8:9	4:5	

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Table II-8 — Linking Arrangements for 2716/6116-Type ROM/RAM Combination Inhibit Feature, High-Half Address Space

To inhibit the various memory address spaces shown in the chart below, *first* setup the link positions as shown in Table II-7, *then* make the changes in links LKB, LKC, and LKE as indicated below.

For the physical location of the XU-Series sockets referred to in the tables below, see Fig. 7. For the relation of these sockets to memory address space, refer to Table IV.

Memory Address Space and Socket		LINK				
		LKA	LKB	LKC	LKD	LKE
Segment	Socket	Position	Position	Position	Position	Position
F000-F7FF	XU14		Open 7:12			
F800-FFFF	XU18		Open 8:11			
F000-FFFF	XU14, XU18		Open 7:12 Open 8:11			
F000-F3FF	XU14			Open 2:15		Close 1:16 Close 7:10
F400-F7FF	XU14			Open 2:15 Open 4:13		Close 1:16 Close 3:14 Close 7:10
F800-FBFF	XU18			Open 2:15		Close 1:16 Close 6:11
FC00-FFFF	XU18			Open 2:15 Open 4:13		Close 1:16 Close 3:14 Close 6:11

Table IV — Relation of Sockets to Memory Space for CDP18S629 COSMAC Microboard 32-kilobyte RAM.

Memory Address Space Selected		Socket
Low-Half	High-Half	
0000-07FF	8000-87FF	XU1
0800-0FFF	8800-8FFF	XU6
1000-17FF	9000-97FF	XU11
1800-1FFF	9800-9FFF	XU15
2000-27FF	A000-A7FF	XU2
2800-2FFF	A800-AFFF	XU7
3000-37FF	B000-B7FF	XU12
3800-3FFF	B800-BFFF	XU16

Memory Address Space Selected		Socket
Low-Half	High-Half	
4000-47FF	C000-C7FF	XU3
4800-4FFF	C800-CFFF	XU8
5000-57FF	D000-D7FF	XU13
5800-5FFF	D800-DFFF	XU17
6000-67FF	E000-E7FF	XU4
6800-6FFF	E800-EFFF	XU9
7000-77FF	F000-F7FF	XU14
7800-7FFF	F800-FFFF	XU18

CDP18S629

How To Use Linking Arrangement Tables to Mix RAM/ROM's

To determine the linking arrangements required for a 4-block 2716/6116-type RAM/ROM combination shown below using the high-half of address space (8000-FFFF), and the instructions shown in Table II-7 for mixing RAM/ROM's, proceed as follows:

8000-9FFF	2716 ROM	No. 1 Block
A000-BFFF	6116 RAM	No. 2 Block
C000-DFFF	6116 RAM	No. 3 Block
E000-FFFF	6116 RAM	No. 4 Block

If the 2716-type ROM is selected to fill the first block, that is, address space 8000-9FFF, the appropriate link position for ROMs on link LKC (5:12) must be closed, and the corresponding link position for RAMs on link LKD (1:8) must be open. (Similarly, if the first block contained RAMs and the second block ROMs, the linking arrangement would be — close 1:8 on Link LKD, open 5:12 on link LKC).

Complete the linking arrangements for the remaining blocks as follows:

For No. 2 block (6116-type RAM) using address space A000-BFFF, close link position 2:7 on link LKD, open link position 6:11 on link LKC.

For No. 3 block (6116-type RAM) using address space C000-DFFF, close link position 3:6 on link LKD, open link posiion 7:10 on link LKC.

For No. 4 block (6116-type RAM) using address space E000-FFFF, close link position 4:5 on link LKD, open link position 8:9 on LKC.

Table V is a summary of the required linking arrangements for this RAM/ROM combination.

Installation in the COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III)

The RCA COSMAC Microboard CDP18S629 may be installed in the CDS II and CDS III in any memory slot 1 through 8. The following connections must be made: To supply the TPA signal, connect pins 1 and A of the selected slot on the CDS backplane. To supply the TPB signal, connect pin B on slot 12 to pin B on the selected slot on the CDS backplane. On the CDP18S005 (CDS II), it is also necessary to connect a wire from pin D on slot 10 to pin 3 on the selected slot. This last connection supplies the RNU signal. On the CDP18S629 Microboard a jumper must be connected between 8:9 on link LKE. The Microboard should be linked for the low half of address space. This arrangement permits use of the existing utility program in the CDS systems at address 8000.

Installation in COSMAC Microboard Computer Development Systems

When a CDP18S629 Microboard 32-kilobyte RAM is added to a Microboard Computer Development System, where the Monitor program is located at address space 8000, a jumper must be connected between pins 8 and 9 of link LKE to supply the RNU signal.

Table V - Linking Arrangements for RAM/ROM Combination

Memory Address Space and Socket		ROM/RAM Type Combination	Link Positions On Links LKD and LKC
Segment	Socket		
8000-9FFF	XU1, XU6 XU11, XU15	2716 ROM	Open 1:8 on LKD, Close 5:12 on LKC
A000-BFFF	XU2, XU7 XU12, XU16	6116 RAM	Close 2:7 on LKD, Open 6:11 on LKC
C000-DFFF	XU3, XU8 XU13, XU17	6116 RAM	Close 3:6 on LKD, Open 7:10 on LKC
E000-FFFF	XU4, XU9 XU14, XU18	6116 RAM	Close 4:5 on LKD, Open 8:9 on LKC

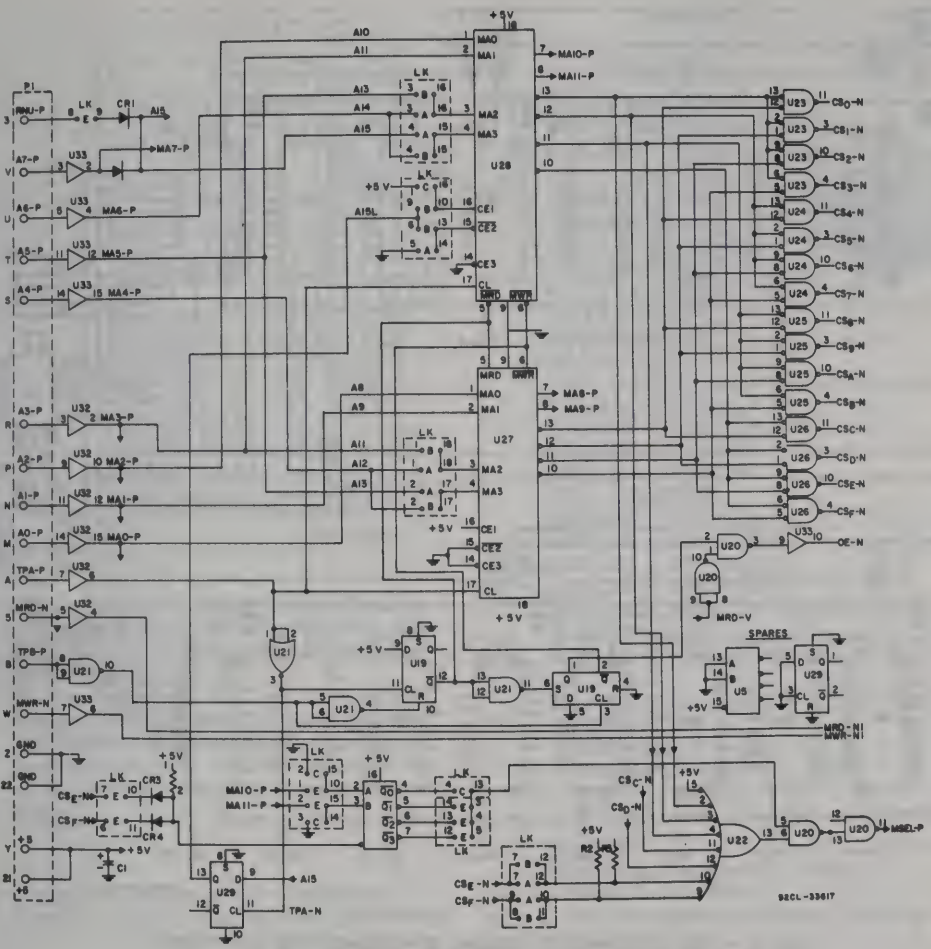


Fig. 5 — RCA COSMAC Microboard 32-Kilobyte RAM CDP18S629 Logic Diagram — Memory Decoding Section.

CDP18S629

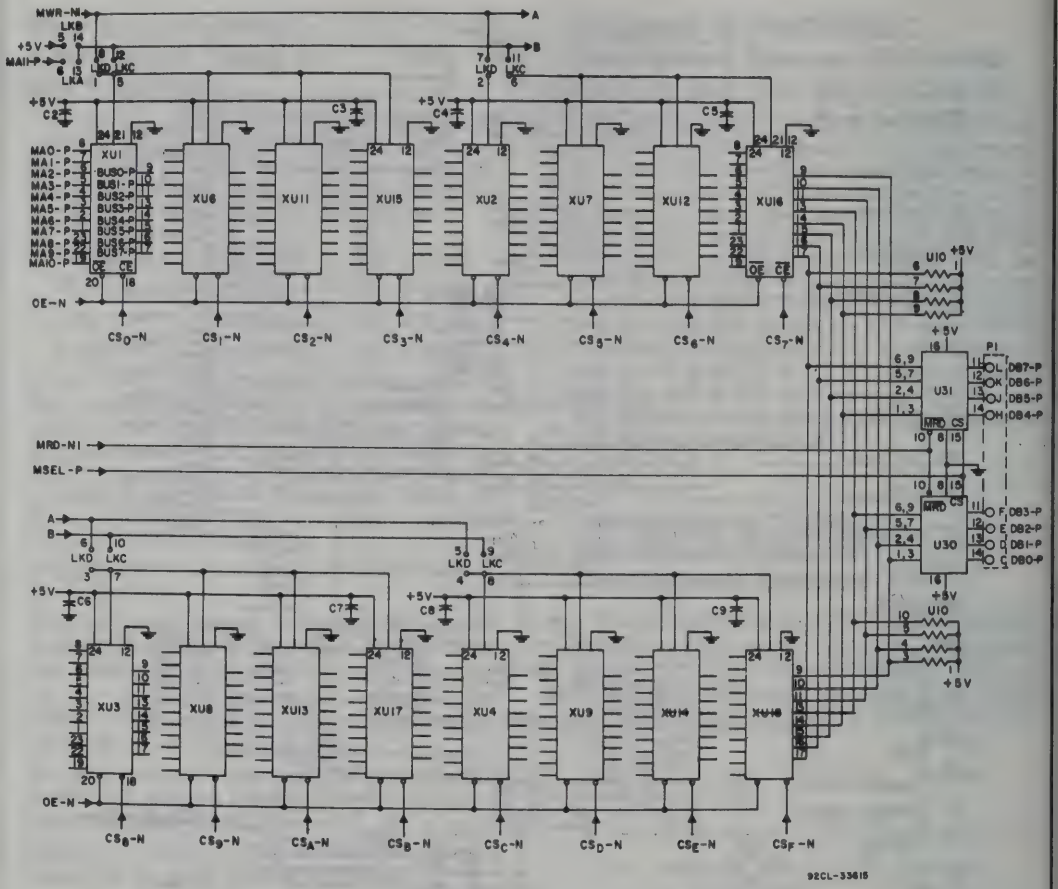
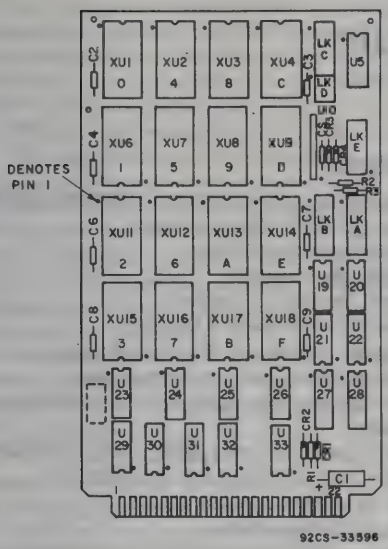


Fig. 6 — RCA COSMAC Microboard 32-Kilobyte RAM CDP18S629 Logic Diagram — Memory Matrix Section.

CDP18S629



A hexadecimal number 0 through F is indicated on each of the 24-pin ROM/RAM socket locations. The numbers represent the ascending order of the socket addresses as shown in Table IV.

Note: Sockets LKC, LKB, and LKD have factory installed DIP SHUNTS. In socket LKC the DIP SHUNT is justified to pin 1 leaving pin positions 5:12, 6:11, 7:10, and 8:9 open. In socket LKB pin position 9:10 is also open. (See Fig. 4)

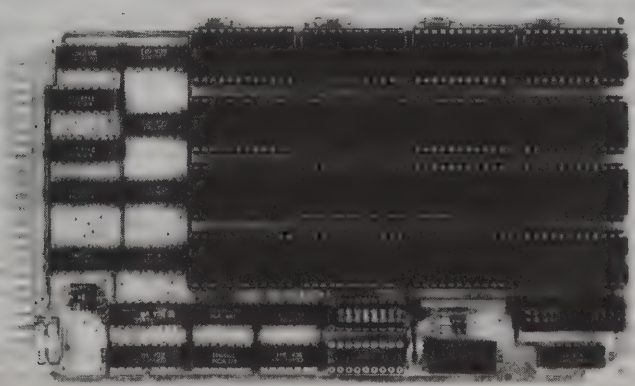
Fig. 7 — Layout Diagram of RCA COSMAC Microboard 32-kilobyte RAM CDP18S629

Parts List

C1 = 22 μF, 25 V
C2-C9 = 0.1 μF, 50 V
CR1-CR4 = 1N270
LKA, LKB = 18-pin DIP socket
LKC, LKE = 16-pin DIP socket
LKD = 8-pin DIP socket
LKC, LKD = 8-pin DIP SHUNT
(See Note, Fig. 7)
LKB = 16-pin DIP SHUNT
(See Note, Fig. 7)
R1-R3 = 22 kilohms, 1/4 W, 5%
U1-U4 = HM6116 P-4
U5 = CD4556BE
U6-U9 = HM6116 P-4
U10 = resistor module, SIP, 10 kilohms
U11-U14 = HM6116 P-4
U15-U18 = HM6116 P-4
U19,U29 = CD4013BE
U20,U21 = CD4011BE
U22 = CD4068BE
U23-U26 = CD4071BE
U27, U28 = CDP1866CE
U30, U31 = CDP1856CE
U32, U33 = CD4050BE
XU1-XU4 = 24-pin DIP socket
XU6-XU9 = 24-pin DIP socket
XU11-XU18 = 24-pin DIP socket

Suggested Vendors for DIP SHUNT networks:
CRS KEENE, Inc.
3230 Riverside Avenue
Paso Robles, California, 93446
Order No. 198D-X
(X is the number of sections, 2 through 12)

AMP Inc.
Harrisburg, Pennsylvania, 17105
Order No. 435704-X
(X is the number of sections, 2 through 12)



CDP18S640A
RCA Microboard Control and Display Module

The RCA Microboard Control and Display Module CDP18S640A provides the operating controls and the display for any Microboard system using the CDP18S601, CDP18S603, CDP18S606, or CDP18S608 Microboard Computer. It includes four switches (RESET, RUN U, RUN P, and STEP/CONT); six hexadecimal display digits; six LED status indicators; a 1-kilobyte Utility ROM UT60 in socket U4; an additional socket that may be used for either 1 kilobyte of mask-programmed ROM (CDP1834) or 1 kilobyte of EPROM (2758) and a one-page (256-byte) RAM for use by either the utility program or the user program.

Components

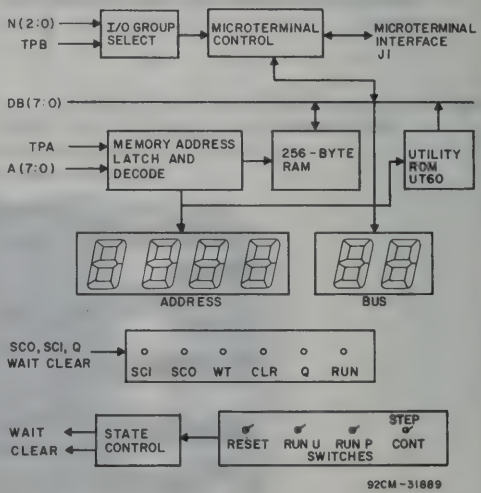
The six-digit hexadecimal **display** utilizes four of the digits for current memory address and two for current data bus content. The six indicator LED's display the status of the following lines: S0, S1 (state code), Q (programmable latched output), WT, CLR (machine mode indicators), and RUN (machine running, not idle, not reset).

The four **control** switches, labeled RESET, RUN P, RUN U, STEP/CONT, enable the operator to clear the system and hold it in the reset state, to initialize and start the user program at address 0000_{16}, to initialize and start the utility program at address 8000_{16}, or to operate the system in either the single-step mode or in the continuous mode. The STEP/CONT switch may also be used as a manual pause during program operation. The single-step mode permits execution of a single machine cycle for each pressing of the RUN U or RUN P switch. By means of this facility, the operator can observe on the six-digit hexadecimal display the address and data sequences of both the fetch and the execute cycles. A special function of the RUN P switch is continued after idle.

The ROM-based **Utility Program** UT60 operates any standard data terminal (RS232C or 20-milliampere loop), through an associated CDP18S601, CDP18S603, CDP18S606, or CDP18S608 Microboard computer, to allow the user to examine memory, alter memory, or begin execution at any specified address. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions include memory insert !M, memory display ?M, memory move $M, memory fill $F, memory substitute !S, and run program $P. The move and fill functions can also be called by user programs.

Features

- **Debugging aid for CDP1802, CDP1804, CDP1805, and CDP1806 Microprocessors**
- **Low-power static CMOS**
- **High noise immunity**
- **Small size (4.5 x 7.5 inches)**
- **Operable from single 5-V supply**
- **Member of extensive Microboard family**
- **Uses Microboard Universal Backplane**
- **Provides control and display for any Microboard system**
- **Four control switches: RESET, RUN PROGRAM, RUN UTILITY, STEP/CONTINUOUS**
- **Six hexadecimal display digits**
- **Six LED status displays**
- **One-page (256-byte) RAM for either utility or user programs**
- **Utility ROM on board (UT60)**
- **Two ROM sockets**
- **0° to 70° C temperature range**



Block diagram of RCA Microboard Control and Display Module CDP18S640A.

The Utility Program includes read and type routines which provide communication with the user terminal. Once the system has been reset, the user can either press RUN P to begin program execution at location 0000_{16} or press RUN U to begin execution of the Utility Program at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and an (LF) half-duplex operation and, at the same time, calculate the time constant to match the baud rate of the data terminal.

The Utility Program also includes user-callable routines which help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are destroyed, however, by the process. The CPU register contents can be examined by displaying memory (?M) beginning at $8C00_{16}$ for 20_{16} bytes.

When the Utility Program is ready to accept commands, it types out an asterisk (*) as a user prompt.

Specifications

Control Switches

RESET—Clears system and latches it in reset state.

RUN P—After RESET, initializes system and starts program execution at 0000_{16}. Continues program execution after idle.

RUN U—After RESET, initializes system and starts UT60 execution at 8000_{16}.

STEP/CONT—In step position, allows execution of a single machine cycle upon depression of RUN P. May be used as manual pause during program execution.

Displays

4 hex digits for address
2 hex digits for data
6 discrete LED's for status:
S0, S1=State code
Q=Programmable latched output
WT, CLR=Machine mode indicators
RUN=Machine running, not at idle, not reset

Memory Capacity

RAM—256 bytes
ROM—1 kilobyte preprogrammed with Utility Program UT60
—1 empty socket for an additional 1-kilobyte ROM (2758 or CDP1834) at address 8400_{16} through $87FF_{16}$.

Operating Temperature Range

0° to 70°C

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Connectors

System interface: edge fingers, 44 pins (dual 22) on 0.156-inch centers
Microterminal interface: connector, 20 pins

Power Requirements

+5 volts at 350 milliamperes, typical operating

Terminal Baud Rates

CDP18S640A (UT60) works with 110, 300, or 1200 baud. Software detects baud rate of terminal and generates a matching rate.

Installation in Microboard System

The CDP18S640A Control and Display module may be installed in any Microboard system incorporating the CDP18S601, CDP18S603, CDP18S606, or CDP18S608 Microboard Computer or equivalent. Signals transmitted through the Microboard Universal Backplane are used to gain control of the CPU mode and to extract information for the display. Table I provides a list of the pins and the signals for the Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the CDP18S640A.

The utility program, UT60, operates on the basis that there is a data terminal interface utilizing the Q output and EF4 input, such as that provided on the CDP18S601, CDP18S603, CDP18S606, or CDP18S608. If UART operation is desired, refer to the technical literature for the CDP18S640A Control and Display Module, CDP18S602 Microboard Computer, and CDP18S641 UART Interface.

The CDP18S640A should be installed in the end slot of the card nest so that physical and visual access is provided for the four control switches and the digital and status displays.

CDP18S640A

Table I - Pin Terminals and Signals for the RCA Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N *	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N *	In	DMA Output
C	DB0-P *	In/Out	Data Bus	3	RNU-P *	—	Run Utility Request
D	DB1-P *	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P *	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P *	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P *	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Request
L	DB7-P *	In/Out	Data Bus	10	WAIT-N *	In	Wait-Mode Request
M	A0-P *	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N *	Out	Memory Write Pulse	19	EF3-N *	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

92CS-34444

*Signals used on RCA Microboard Control and Display Module CDP18S640A.

Manual Operations

RESET Switch. Depression of this momentary switch (S1) causes the assertion of the CLEAR input to the CPU and the removal of the WAIT input, if any. This condition is stored and the system remains in the CLEAR mode until further switch action is made. On the LED status display the CLR (clear) indicator (CR4) is lit and the WT (wait) indicator (CR3) is dark.

RUN P Switch. Depression of this momentary RUN PROGRAM switch (S3) causes the removal of the CLEAR mode, if present. Following a CLEAR mode, RUN P starts execution of the program stored at memory location 0000_{16} after the CPU has executed the initialization cycle. If the STEP/CONT switch is in the STEP position, only one machine cycle will be executed.

If the program reaches an IDLE instruction, it will cycle in continuous S1 states. The RUN P switch may be used to "bump" the system past the IDLE and continue processing. This operation, however, results in the incrementing of register R0.

The RUN P switch affects the RUN, WT, and CLR LED displays. Depression of the RUN P switch will light the RUN indicator (CR6). It will stay lit until an IDLE is encountered or the RESET switch is depressed. The WT and CLR indicators go dark upon depression of RUN P, but WT will light again if the STEP/CONT switch is set in the STEP position.

RUN U Switch. Depression of this momentary RUN UTILITY switch (S2) performs the same functions as the RUN P switch, with an additional function. Depressing RUN U asserts the RNU signal on the Microboard Universal Backplane (Pin 3), resulting in start of execution at memory address 8000_{16}, the location of the utility program UT60.

STEP/CONT Switch. The STEP/CONTINUOUS switch is a toggle switch (S4). When this switch is in the CONT position, operation is continuous at machine speed. When the switch is in the STEP position, each depression of RUN P or RUN U causes execution of one machine cycle. The system stops during TPB so that the ADDRESS and DATA buses are stable and their contents may be observed in the six hexadecimal display modules. The STEP/CONT switch also affects the state code indicators SC0 and SC1, WT, CLR, and RUN. The WT indicator will be lighted when the system is in the STEP mode even though it is off during the execution of

one machine cycle. The CLR indicator will remain dark unless the RESET switch is depressed. The RUN indicator is lighted as soon as a RUN switch is depressed and stays lighted until either an IDLE instruction is encountered or RESET is depressed. The SC0 and SC1 indicators (CR2 and CR1, respectively) tell the state of the CPU. When both are dark, the CPU is in the Fetch state. When SC0 is lighted and SC1 is dark, the CPU is in the Execute state. Thus, stepping through a program, one observes in the Fetch cycle the address of the program step about to be executed and the instruction code on the BUS. Then, in the Execute cycle, one observes the data transaction on the BUS and the memory address to or from which data is transferred. Not all Execute cycles transfer data to or from memory, but most do. Refer to the CPU technical literature for the operation format for each instruction.

The DMA state is indicated when SC0 is dark and SC1 is lighted. The data transaction on the BUS and the memory address may also be observed as described above.

Hexadecimal Displays. The seven-segment hexadecimal LED displays show the current address and data. The high-order address is latched and the low-order address is displayed directly from the bus, so that the full 16-bit memory address may be viewed. The data bus information is displayed directly. Because the STEP mode stops between TPA and TPB, a valid 16-bit address and an 8-bit data byte are displayed for each machine cycle.

Because hexadecimal digits B and D do not map into seven segments uniquely, lower case is used for these symbols. Note that the digit six is displayed as 5 , digit B is displayed as *b* , and digit D is displayed as *d* .

Operations With IDLE. It is often useful to insert IDLE instructions in a program so that one may stop and check for proper operation before continuing. The IDLE condition is observed when the RUN and CLR indicators are both dark. SC0 will be lighted and SC1 dark indicating the S1 or Fetch state. At this point, the operator chooses one of two techniques for analysis. Pressing RESET and then RUN U returns control to UT60, which is then used to examine register and memory content at the point where IDLE was inserted in the program. Alternatively, pressing RUN P only causes the program to continue past the IDLE.

The mechanization of this restart-from-IDLE feature creates the need for caution regarding the Program Counter assignment. After IDLE is detected, depressing RUN P results in a DMA out request. This request breaks out of the IDLE for the DMA cycle and is followed by a fetch of the next instruction. If P=0, R0 is the Program Counter as well as the DMA pointer. The DMA cycle will increment R0, causing a jump over the instruction following the IDLE. In fact, because of capacitive delays, two DMA cycles may occur, resulting in a jump over two instruction locations. Therefore, when R0 is used as the Program Counter, the IDLE should be followed by the insertion of two NO-OP instructions.

It is better to assign P=3 or greater, so that the DMA pointer, R0, is free. In this case, only an IDLE need be inserted where a break is desired.

The STEP mode may be used concurrently with the IDLE and continue operation. The first DMA after RUN P is pressed will not be seen, but any subsequent DMA will be stepped through the same as any other machine cycle.

Using The Microterminal

Connector J1 and associated logic are provided on the CDP18S640A for the attachment of the Microterminal CDP18S021. Because a special utility program, UT5, is provided with the Microterminal, the UT60 ROM in socket location U4, should be replaced with the UT5 ROM. The Microterminal cable connector should be inserted into J1 and the power turned on. Table II provides a list of the pins and the signals for the 20-pin Microterminal connector J1. The four switches on the CDP18S640A are duplicated on the Microterminal keyboard, and either set may be used. The Microterminal display, because it is software refreshed, will not operate

Table II - Microterminal CDP18S021 Connections on Microboard Control and Display Module CDP18S640A (J1)

Pin	Signal	Pin	Signal
1	RUN U-N0	2	CLEAR-N0
3	RUN P-N0	4	STEP-N0
5	V_{LED}	6	DB0-P
7	V_{CC}	8	DB1-P
9	TEF3-N	10	DB2-P
11	IO4-P	12	DB3-P
13	IO3-P	14	DB4-P
15	MRD-N	16	DB5-P
17	TPB-P2	18	DB6-P
19	GND	20	DB7-P

CDP18S640A

in STEP mode, but the Control and Display board operates as usual.

For a detailed description of the Microterminal and its operation, refer to the **Instruction Manual for the RCA COSMAC Microterminal**, MPM-212.

Utility Program UT60

The Utility Program UT60 provided with the CDP18S640A is designed to examine memory, alter memory, and begin program execution at a specified location. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions described include memory insert !M, memory display ?M, memory move $M, memory fill $F, memory substitute !S, and run program $P. The move and fill functions can also be called by user programs.

The UT60 includes read and type routines that provide communication with the user terminal. A "software UART" is provided that uses the Q and EF4 lines for output and input, respectively. The timing constant and duplex mode are determined when the utilities are entered from reset. Once the system has been RESET, the user can either press RUN P to begin program execution at location 0000_{16}, or press RUN U to begin execution of UT60 at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and a (LF) half-duplex operation.

The UT60 also includes user-callable routines that help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are lost, however, by the process. The CPU register contents can be examined by displaying memory (see ?M command below)beginning at $8C00_{16}$ for 20_{16} bytes.

When UT60 is ready to accept commands, it types out an asterisk (*) as a user prompt. The commands described below may then be entered. Where addresses are specified, leading zeroes are assumed; and if more than four digits are entered, only the last four are retained. In all cases, a command is terminated by a carriage return (CR). If a syntactical error is detected during the entry of a command, UT60 will respond with a (?) and reprompt the user with an asterisk (*).

UT60 Commands

?M Commands

Name: Memory Display

Purpose: To allow a specified area of memory to be displayed on the user terminal.

Format: ?M(START ADDR)(OPTION)(CR)

Action: The contents of memory, beginning at the specified (START ADDR) will be transmitted to the user terminal. (OPTION) allows the transmission of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen. If the option is not specified, a default value of 1 byte results.

Examples: ?M2F8 8(CR)
?M2F8-02FF(CR)
Both of these examples produce the same output.

!M Commands

Name: Memory Insert

Purpose: To alter the contents of memory beginning at the specified address.

Format: !M (START ADDR)(SPACE)(DATA)[(CONT)](CR)

Action: A memory location is accessed at the specified (START ADDR). The (DATA) required is one byte specified by two hex digits. The (CONT) option allows data to be continued onto the next line on the terminal with or without changing the current memory address. A (COMMA) will not change the address and after the user inserts (CR)(LF), additional data may be entered. If a (SEMICOLON) is entered and after a user-inserted (CR)(LF), a new address is anticipated. The semicolon allows non-contiguous memory to be loaded with a single insert command. The command may be terminated at any point by the entry of a (CR) not preceded by a (COMMA) or (SEMICOLON).

Examples: !M02F8 7100F840B0F88CB1(CR)

!M02F8 7100F840,(CR)(LF)

B0F8,(CR)(LF)
8CB1(CR)

!M02F8 7100F840B0;(CR)(LF)
03B6 94FB903A0F(CR)

The first and second examples give identical results. The second provides improved readability at the data terminal output. The third example enters data into two memory areas, starting at $02F8_{16}$ and $03B6_{16}$.

$M Commands

Name: Memory Move

Purpose: To move a block of data from one area of memory to another area.

Format: $M(SOURCE ADDR)(OPTION)(SPACE)(DEST ADDR)(CR)

Action: Data is copied from memory location beginning at the (SOURCE ADDR) into locations specified by the (DEST ADDR). (OPTION) allows the transfer of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen. There is no restriction on the direction of the move and the areas may overlap.

Examples: $M02F8 8 03F8(CR)

$M02F8-02FF 03F8(CR)

$M03B0-03BF 02B0(CR)

$M03B0-03BF 03B2(CR)

$F Commands

Name: Memory Fill

Purpose: To load a defined area of memory with a specified constant.

Format: $F(START ADDR)(OPTION)(SPACE)(DATA)(CR)

Action: The specified (DATA) is loaded into memory beginning at the (START ADDR). (OPTION) allows the loading of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen.

Examples: $F02F8 8 00(CR)

$F02F8-02FF 00(CR)

These examples fill with zeros the eight bytes beginning at location $02F8_{16}$.

!S Commands

Name: Memory Substitute

Purpose: To display and, if desired, alter the contents of sequential memory locations beginning at the specified address.

Format: !S(START ADDR)(OPTION)(CR)

Action: A memory location is accessed at the specified (START ADDR). Its contents will not be displayed, however, until (OPTIONS) is entered. (OPTIONS) allows two methods of display: (SPACE) or (LF). If (SPACE) is entered, the current data will be displayed on the same line followed by a hyphen. New data may be entered at this point. Only the last byte entered will be written. If no data is entered, the current data will remain unchanged. If another space is entered, the data in the next sequential memory location will be displayed followed by a hyphen. If a (LF) is entered, a (CR)(LF) will result and the next memory address will be printed followed by the current data and a hyphen. New data may be entered as described above. The command can be terminated by a (CR) or continued by the entry of any number of (OPTIONS).

Examples: !S02F8 63-71 00- 0F-C0(CR)
The current data of 63 is changed to 71. The 00 data is retained, and the 0F is changed to C0.

!S02F8 71- 00- C0- 11-82(LF)
02FC 52-AE(LF)
02FD 00-F8 11-40 23-A3(CR)
In this example, the 71, 00, and C0 are retained and the 11 is changed to 82. Each (LF) causes the next address to be typed followed by its data.

$P Commands

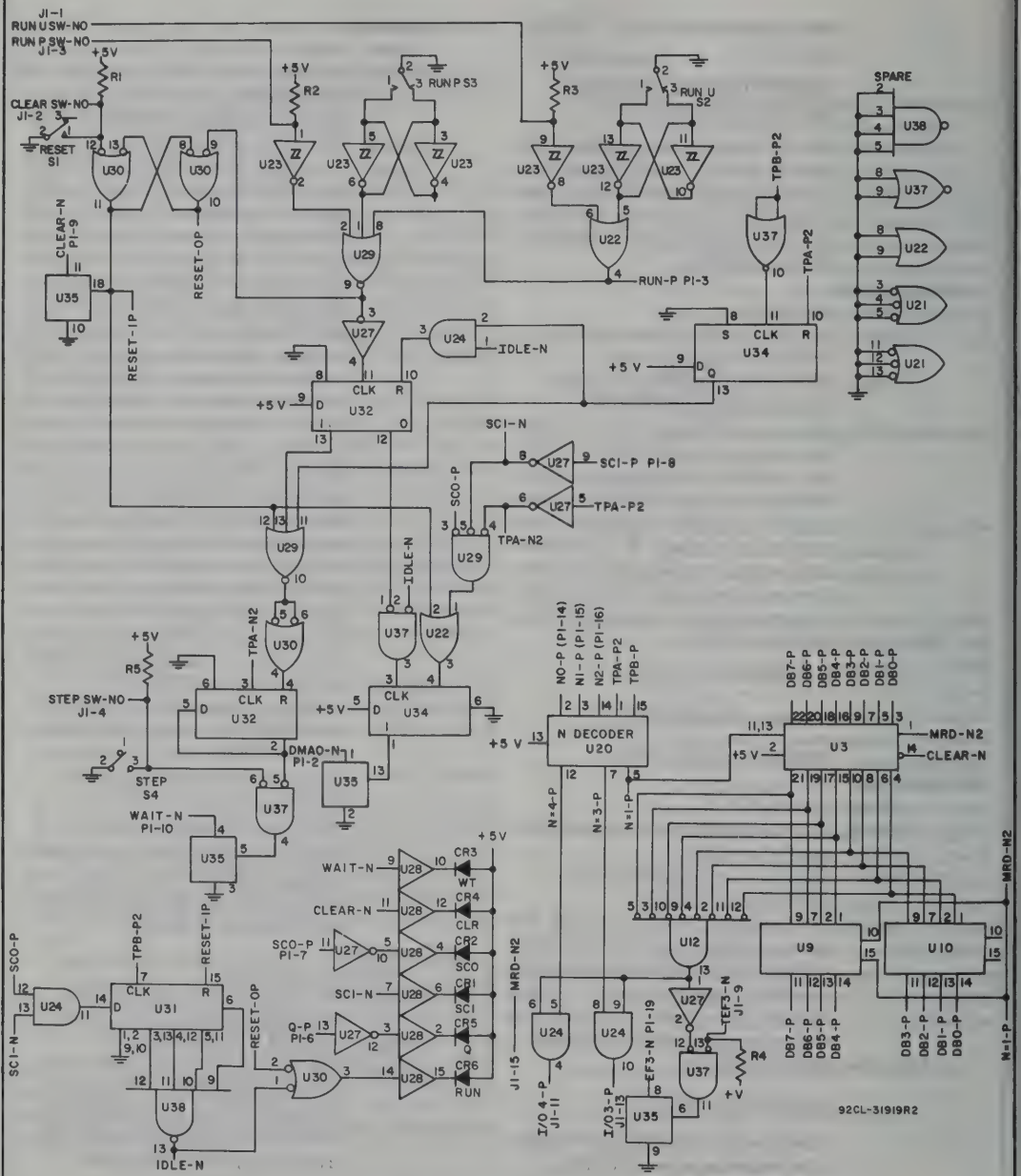
Name: Program Run

Purpose: To allow a user program to be run beginning at the specified address.

Format: $P[(START ADDR)](CR)

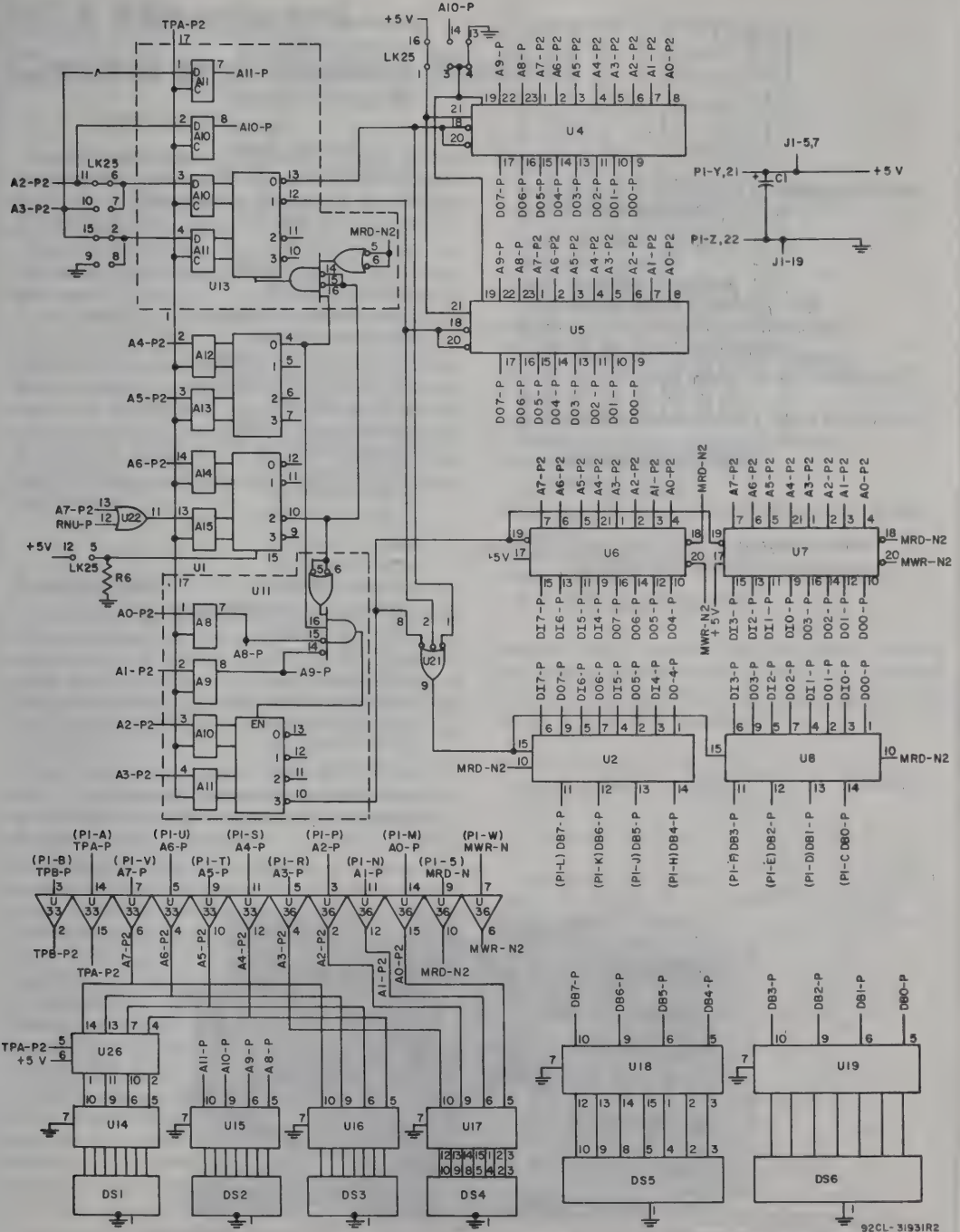
Action: The user program will begin execution at the specified (START ADDR) with P=0 and X=0. If the (START ADDR) is not specified, the default value is 0000_{16}. The interrupt flag is also reset.

CDP18S640A



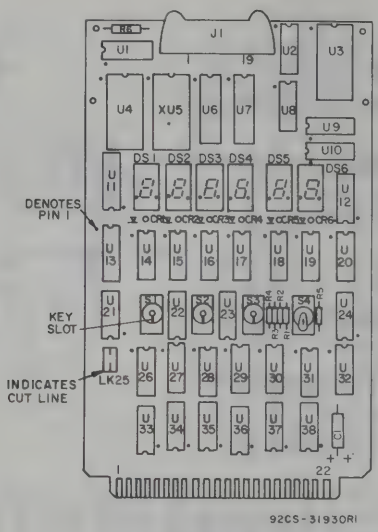
Logic diagram of Microboard Control and Display Module CDP18S640A-control and status indicator portion.

CDP18S640A



Logic diagram of Microboard Control and Display Module CDP18S640A–memory and memory display portion.

CDP18S640A



Layout diagram of RCA Microboard Control and Display Module CDP18S640A.

Parts List

C1=15 μF, 20 V
CR1-CR6=LED
DS1-DS6=7-segment display HP5082-7740
J1=connector, 20 pin
R1-R6=22 kΩ, ¼ W, 5%
S1, S2, S3=switch, momentary
S4=switch, SPDT
U1=CDP1858CE
U2, U8=CDP1856CE
U3=CDP1852CE
U4=Utility ROM UT60
U6, U7=MWS5101
U9, U10=CDP1857CE
U11, U13=CDP1866CE
U12=CD4078BE
U14-U19=MC14495P
U20=CDP1853CE
U21=CD4023BE
U22=CD4071BE
U23=CD40106BE
U24=CD4081BE
U26=CD4042BE
U27=CD4069BE
U28, U33, U36=CD4050BE
U29=CD4025BE
U30=CD4011BE
U31=CD4076BE
U32, U34=CD4013BE
U35=CD4016BE
U37=CD4001BE
U38=CD4012BE
XDS1-XDS6=DIP socket, 10 pin
XU4, XU5=IC socket, 24 pin

RCA Microboard Control and Display Module

The RCA Microboard Control and Display Module CDP18S640A1 provides the operating controls and the display for any Microboard system using the CDP18S602 or CDP18S607 Microboard Computer.

The CDP18S640A1 can also be used with the CDP18S601, CDP18S603, CDP18S606, or CDP18S608 Microboard Computer if the CDP18S641 UART Interface Module is added. The CDP18S640A1 includes four switches (RESET, RUN U, RUN P, and STEP/CONT); six hexadecimal display digits; six LED status indicators; a 1-kilobyte Utility ROM UT61 in socket U4; an additional socket that may be used for either 1 kilobyte of mask-programmed ROM (CDP1834) or 1 kilobyte of EPROM (2758) and a one-page (256-byte) RAM for use by either the utility program or the user program.

Components

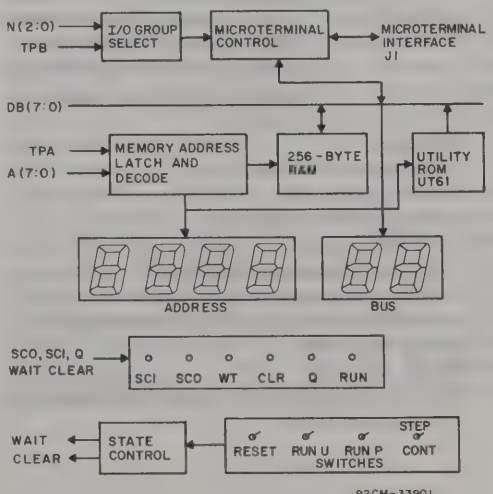
The six-digit hexadecimal **display** utilizes four of the digits for current memory address and two for current data bus content. The six indicator LED's display the status of the following lines: S0, S1 (state code), Q (programmable latched output), WT, CLR (machine mode indicators), and RUN (machine running, not idle, not reset).

The four **control** switches, labeled RESET, RUN P, RUN U, STEP/CONT, enable the operator to clear the system and hold it in the reset state, to initialize and start the user program at address 0000_{16}, to initialize and start the utility program at address 8000_{16}, or to operate the system in either the single-step mode or in the continuous mode. The STEP/CONT switch may also be used as a manual pause during program operation. The single-step mode permits execution of a single machine cycle for each pressing of the RUN U or RUN P switch. By means of this facility, the operator can observe on the six-digit hexadecimal display the address and data sequences of both the fetch and the execute cycles. A special function of the RUN P switch is continued after idle.

The ROM-based **Utility Program** UT61 operates any standard data terminal (RS232C or 20-milliampere loop), through an associated CDP18S602 or CDP18S607 Microboard computer, to allow the user to examine memory, alter memory, or begin execution at any specified address. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions include memory insert !M, memory display ?M, memory move $M, memory fill $F, memory substitute !S, and run program $P. The move and fill functions can also be called by user programs.

Features

- **Debugging aid for CDP1802, CDP1804, CDP1805, and CDP1806 Microprocessors**
- **Low-power static CMOS**
- **High noise immunity**
- **Small size (4.5 x 7.5 inches)**
- **Operable from single 5-V supply**
- **Member of extensive Microboard family**
- **Uses Microboard Universal Backplane**
- **Provides control and display for any Microboard system**
- **Four control switches: RESET, RUN PROGRAM, RUN UTILITY, STEP/CONTINUOUS**
- **Six hexadecimal display digits**
- **Six LED status displays**
- **One-page (256-byte) RAM for either utility or user programs**
- **Utility ROM on board (UT61)**
- **Two ROM sockets**
- **0° to 70° C temperature range**



Block diagram of RCA Microboard Control and Display Module CDP18S640A1.

CDP18S640A1

The Utility Program includes read and type routines which provide communication with the user terminal. Once the system has been reset, the user can either press RUN P to begin program execution at location 0000_{16} or press RUN U to begin execution of the Utility Program at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and an (LF) half-duplex operation and, at the same time, calculate the time constant to match the baud rate of the data terminal.

The Utility Program also includes user-callable routines which help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are destroyed, however, by the process. The CPU register contents can be examined by displaying memory (?M) beginning at $8C00_{16}$ for 20_{16} bytes.

When the Utility Program is ready to accept commands, it types out an asterisk (*) as a user prompt.

Specifications

Control Switches

RESET—Clears system and latches it in reset state.

RUN P—After RESET, initializes system and starts program execution at 0000_{16}. Continues program execution after idle.

RUN U—After RESET, initializes system and starts UT61 execution at 8000_{16}.

STEP/CONT—In step position, allows execution of a single machine cycle upon depression of RUN P. May be used as manual pause during program execution.

Displays

4 hex digits for address
2 hex digits for data
6 discrete LED's for status:
S0, S1=State code
Q=Programmable latched output
WT, CLR=Machine mode indicators
RUN=Machine running, not at idle, not reset

Memory Capacity

RAM—256 bytes
ROM—1 kilobyte preprogrammed with Utility Program UT61
—1 empty socket for an additional 1-kilobyte ROM (2758 or CDP1834) at address 8400_{16} through $87FF_{16}$.

Operating Temperature Range

0° to 70°C

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Connectors

System interface: edge fingers, 44 pins (dual 22) on 0.156-inch centers
Microterminal interface: connector, 20 pins

Power Requirements

+5 volts at 350 milliamperes, typical operating

Terminal Baud Rates

When using the CDP18S640A1, the terminal baud rate can be any one of 14 rates from 50 to 19200 baud as selected on the CDP18S602 or CDP18S607 Microboard Computer (see MB-602, MB607).

If the CDP18S641 UART Interface Module is used in combination with the CDP18S601, CDP18S603, CDP18S606 or CDP18S608 Microboard Computer, the baud rate can be any one of six rates from 110 to 19200 baud.

Installation in Microboard System

The CDP18S640A1 Control and Display module may be installed in any Microboard system incorporating the CDP18S602 or CDP18S607 Microboard Computer or equivalent. Signals transmitted through the Microboard Universal Backplane are used to gain control of the CPU mode and to extract information for the display. Table I provides a list of the pins and the signals for the Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the CDP18S640A1.

The CDP18S640A1 should be installed in the end slot of the card nest so that physical and visual access is provided for the four control switches and the digital and status displays.

Manual Operations

RESET Switch. Depression of this momentary switch (S1) causes the assertion of the CLEAR input to the CPU and the removal of the WAIT input, if any. This condition is stored and the system remains in the CLEAR mode until further switch action is made. On the LED status display the CLR (clear) indicator (CR4) is lit and the WT (wait) indicator (CR3) is dark.

CDP18S640A1

Table I - Pin Terminals and Signals for the RCA Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N *	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N *	In	DMA Output
C	DB0-P *	In/Out	Data Bus	3	RNU-P *	—	Run Utility Request
D	DB1-P *	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P *	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P *	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P *	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Request
L	DB7-P *	In/Out	Data Bus	10	WAIT-N *	In	Wait-Mode Request
M	A0-P *	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N *	Out	Memory Write Pulse	19	EF3-N *	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

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*Signals used on RCA Microboard Control and Display Module CDP18S640A1.

RUN P Switch. Depression of this momentary RUN PROGRAM switch (S3) causes the removal of the CLEAR mode, if present. Following a CLEAR mode, RUN P starts execution of the program stored at memory location 0000_{16} after the CPU has executed the initialization cycle. If the STEP/CONT switch is in the STEP position, only one machine cycle will be executed.

If the program reaches an IDLE instruction, it will cycle in continuous S1 states. The RUN P switch may be used to "bump" the system past the IDLE and continue processing. This operation, however, results in the incrementing of register R0.

The RUN P switch affects the RUN, WT, and CLR LED displays. Depression of the RUN P switch will light the RUN indicator (CR6). It will stay lit until an IDLE is encountered or the RESET switch is depressed. The WT and CLR indicators go dark upon depression of RUN P, but WT will light again if the STEP/CONT switch is set in the STEP position.

RUN U Switch. Depression of this momentary RUN UTILITY switch (S2) performs the same functions as the RUN P switch, with an additional function. Depressing RUN U asserts the RNU signal on the Microboard Universal Backplane (Pin 3), resulting in start of execution at memory address 8000_{16}, the location of the utility program UT61.

STEP/CONT Switch. The STEP/CONTINUOUS switch is a toggle switch (S4). When this switch is in the CONT position, operation is continuous at machine speed. When the switch is in the STEP position, each depression of RUN P or RUN U causes execution of one machine cycle. The system stops during TPB so that the ADDRESS and DATA buses are stable and their contents may be observed in the six hexadecimal display modules. The STEP/CONT switch also affects the state code indicators SC0 and SC1, WT, CLR, and RUN. The WT indicator will be lighted when the system is in the STEP mode even though it is off during the execution of one machine cycle. The CLR indicator will remain dark unless the RESET switch is depressed. The RUN indicator is lighted as soon as a RUN switch is depressed and stays lighted until either an IDLE instruction is encountered or RESET is depressed. The SC0 and SC1 indicators (CR2 and CR1, respectively) tell the state of the CPU. When both are dark, the CPU is in the Fetch state. When SC0 is lighted and SC1 is dark, the CPU is in the Execute state.

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Thus, stepping through a program, one observes in the Fetch cycle the address of the program step about to be executed and the instruction code on the BUS. Then, in the Execute cycle, one observes the data transaction on the BUS and the memory address to or from which data is transferred. Not all Execute cycles transfer data to or from memory, but most do. Refer to the CPU technical literature for the operation format for each instruction.

The DMA state is indicated when SC0 is dark and SC1 is lighted. The data transaction on the BUS and the memory address may also be observed as described above.

Hexadecimal Displays. The seven-segment hexadecimal LED displays show the current address and data. The high-order address is latched and the low-order address is displayed directly from the bus, so that the full 16-bit memory address may be viewed. The data bus information is displayed directly. Because the STEP mode stops between TPA and TPB, a valid 16-bit address and an 8-bit data byte are displayed for each machine cycle.

Because hexadecimal digits B and D do not map into seven segments uniquely, lower case is used for these symbols. Note that the digit six is displayed as 6, digit B is displayed as b, and digit D is displayed as d.

Operations With IDLE. It is often useful to insert IDLE instructions in a program so that one may stop and check for proper operation before continuing. The IDLE condition is observed when the RUN and CLR indicators are both dark. SC0 will be lighted and SC1 dark indicating the S1 or Fetch state. At this point, the operator chooses one of two techniques for analysis. Pressing RESET and then RUN U returns control to UT61, which is then used to examine register and memory content at the point where IDLE was inserted in the program. Alternatively, pressing RUN P only causes the program to continue past the IDLE.

The mechanization of this restart-from-IDLE feature creates the need for caution regarding the Program Counter assignment. After IDLE is detected, depressing RUN P results in a DMA out request. This request breaks out of the IDLE for the DMA cycle and is followed by a fetch of the next instruction. If P=0, R0 is the Program Counter as well as the DMA pointer. The DMA cycle will increment R0, causing a jump over the instruction following the IDLE. In fact, because of capacitive delays, two DMA cycles may occur, resulting in a jump over two instruction locations. Therefore, when R0 is used as the Program Counter, the IDLE should be followed by the insertion of two NO-OP instructions.

It is better to assign P=3 or greater, so that the DMA pointer, R0, is free. In this case, only an IDLE need be inserted where a break is desired.

The STEP mode may be used concurrently with the IDLE and continue operation. The first DMA after RUN P is pressed will not be seen, but any subsequent DMA will be stepped through the same as any other machine cycle.

Using The Microterminal

Connector J1 and associated logic are provided on the CDP18S640A1 for the attachment of the Microterminal CDP18S021. Because a special utility program, UT5, is provided with the Microterminal, the UT61 ROM in socket location U4, should be replaced with the UT5 ROM. The Microterminal cable connector should be inserted into J1 and the power turned on. Table II provides a list of the pins and the signals for the 20-pin Microterminal connector J1. The four switches on the CDP18S640A1 are duplicated on the Microterminal keyboard, and either set may be used. The Microterminal display, because it is software refreshed, will not operate in STEP mode, but the Control and Display board operates as usual.

For a detailed description of the Microterminal and its operation, refer to the **Instruction Manual for the RCA COSMAC Microterminal**, MPM-212.

Table II - Microterminal CDP18S021 Connections on Microboard Control and Display Module CDP18S640A1 (J1)

Pin	Signal	Pin	Signal
1	RUN U-N0	2	CLEAR-N0
3	RUN P-N0	4	STEP-N0
5	V_{LED}	6	DB0-P
7	V_{CC}	8	DB1-P
9	TEF3-N	10	DB2-P
11	IO4-P	12	DB3-P
13	IO3-P	14	DB4-P
15	MRD-N	16	DB5-P
17	TPB-P2	18	DB6-P
19	GND	20	DB7-P

Utility Program UT61

The Utility Program UT61 provided with the CDP18S640A1 is designed to examine memory, alter memory, and begin program execution at a specified location. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions described include memory insert !M, memory display ?M, memory move $M, memory fill $F, memory substitute !S, and run program $P. The move and fill functions can also be called by user programs.

The UT61 includes read and type routines that provide communication with the user terminal. Once the system has been RESET, the user can either press RUN P to begin program execution at location 0000_{16}, or press RUN U to begin execution of UT61 at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and a (LF) half-duplex operation.

The UT61 also includes user-callable routines that help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are lost, however, by the process. The CPU register contents can be examined by displaying memory (see ?M command below) beginning at $8C00_{16}$ for 20_{16} bytes.

When UT61 is ready to accept commands, it types out an asterisk (*) as a user prompt. The commands described below may then be entered. Where addresses are specified, leading zeroes are assumed; and if more than four digits are entered, only the last four are retained. In all cases, a command is terminated by a carriage return (CR). If a syntactical error is detected during the entry of a command, UT61 will respond with a (?) and reprompt the user with an asterisk (*).

UT61 Commands

?M Commands

Name: Memory Display

Purpose: To allow a specified area of memory to be displayed on the user terminal.

Format: ?M(START ADDR)(OPTION)(CR)

Action: The contents of memory, beginning at the specified (START ADDR) will be transmitted to the user terminal. (OPTION) allows the transmission of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen. If the option is not specified, a default value of 1 byte results.

Examples: ?M2F8 8(CR)
?M2F8-02FF(CR)
Both of these examples produce the same output.

!M Commands

Name: Memory Insert

Purpose: To alter the contents of memory beginning at the specified address.

Format: !M (START ADDR)(SPACE)(DATA)[(CONT)](CR)

Action: A memory location is accessed at the specified (START ADDR). The (DATA) required is one byte specified by two hex digits. The (CONT) option allows data to be continued onto the next line on the terminal with or without changing the current memory address. A (COMMA) will not change the address and after the user inserts (CR)(LF), additional data may be entered. If a (SEMICOLON) is entered and after a user-inserted (CR)(LF), a new address is anticipated. The semicolon allows non-contiguous memory to be loaded with a single insert command. The command may be terminated at any point by the entry of a (CR) not preceded by a (COMMA) or (SEMICOLON).

Examples: !M02F8 7100F840B0F88CB1(CR)

!M02F8 7100F840,(CR)(LF)
B0F8,(CR)(LF)
8CB1(CR)

!M02F8 7100F840B0;(CR)(LF)
03B6 94FB903A0F(CR)

The first and second examples give identical results. The second provides

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improved readability at the data terminal output. The third example enters data into two memory areas, starting at $02F8_{16}$ and $03B6_{16}$.

$M Commands

Name: Memory Move

Purpose: To move a block of data from one area of memory to another area.

Format: $M(SOURCE ADDR)(OPTION)(SPACE)(DEST ADDR)(CR)

Action: Data is copied from memory location beginning at the (SOURCE ADDR) into locations specified by the (DEST ADDR). (OPTION) allows the transfer of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen. There is no restriction on the direction of the move and the areas may overlap.

Examples: $M02F8 8 03F8(CR)

$M02F8-02FF 03F8(CR)

$M03B0-03BF 02B0(CR)

$M03B0-03BF 03B2(CR)

$F Commands

Name: Memory Fill

Purpose: To load a defined area of memory with a specified constant.

Format: $F(START ADDR)(OPTION)(SPACE)(DATA)(CR)

Action: The specified (DATA) is loaded into memory beginning at the (START ADDR). (OPTION) allows the loading of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen.

Examples: $F02F8 8 00(CR)

$F02F8-02FF 00(CR)

These examples fill with zeros the eight bytes beginning at location $02F8_{16}$.

!S Commands

Name: Memory Substitute

Purpose: To display and, if desired, alter the contents of sequential memory locations beginning at the specified address.

Format: !S(START ADDR)(OPTION)(CR)

Action: A memory location is accessed at the specified (START ADDR). Its contents will not be displayed, however, until (OPTIONS) is entered. (OPTIONS) allows two methods of display: (SPACE) or (LF). If (SPACE) is entered, the current data will be displayed on the same line followed by a hyphen. New data may be entered at this point. Only the last byte entered will be written. If no data is entered, the current data will remain unchanged. If another space is entered, the data in the next sequential memory location will be displayed followed by a hyphen. If a (LF) is entered, a (CR)(LF) will result and the next memory address will be printed followed by the current data and a hyphen. New data may be entered as described above. The command can be terminated by a (CR) or continued by the entry of any number of (OPTIONS).

Examples: !S02F8 63-71 00- 0F-C0(CR)

The current data of 63 is changed to 71. The 00 data is retained, and the 0F is changed to C0.

!S02F8 71- 00- C0- 11-82(LF)
02FC 52-AE(LF)
02FD 00-F8 11-40 23-A3(CR)

In this example, the 71, 00, and C0 are retained and the 11 is changed to 82. Each (LF) causes the next address to be typed followed by its data.

$P Commands

Name: Program Run

Purpose: To allow a user program to be run beginning at the specified address.

Format: $P[(START ADDR)](CR)

Action: The user program will begin execution at the specified (START ADDR) with P=0 and X=0. If the (START ADDR) is not specified, the default value is 0000_{16}. The interrupt flag is also reset.

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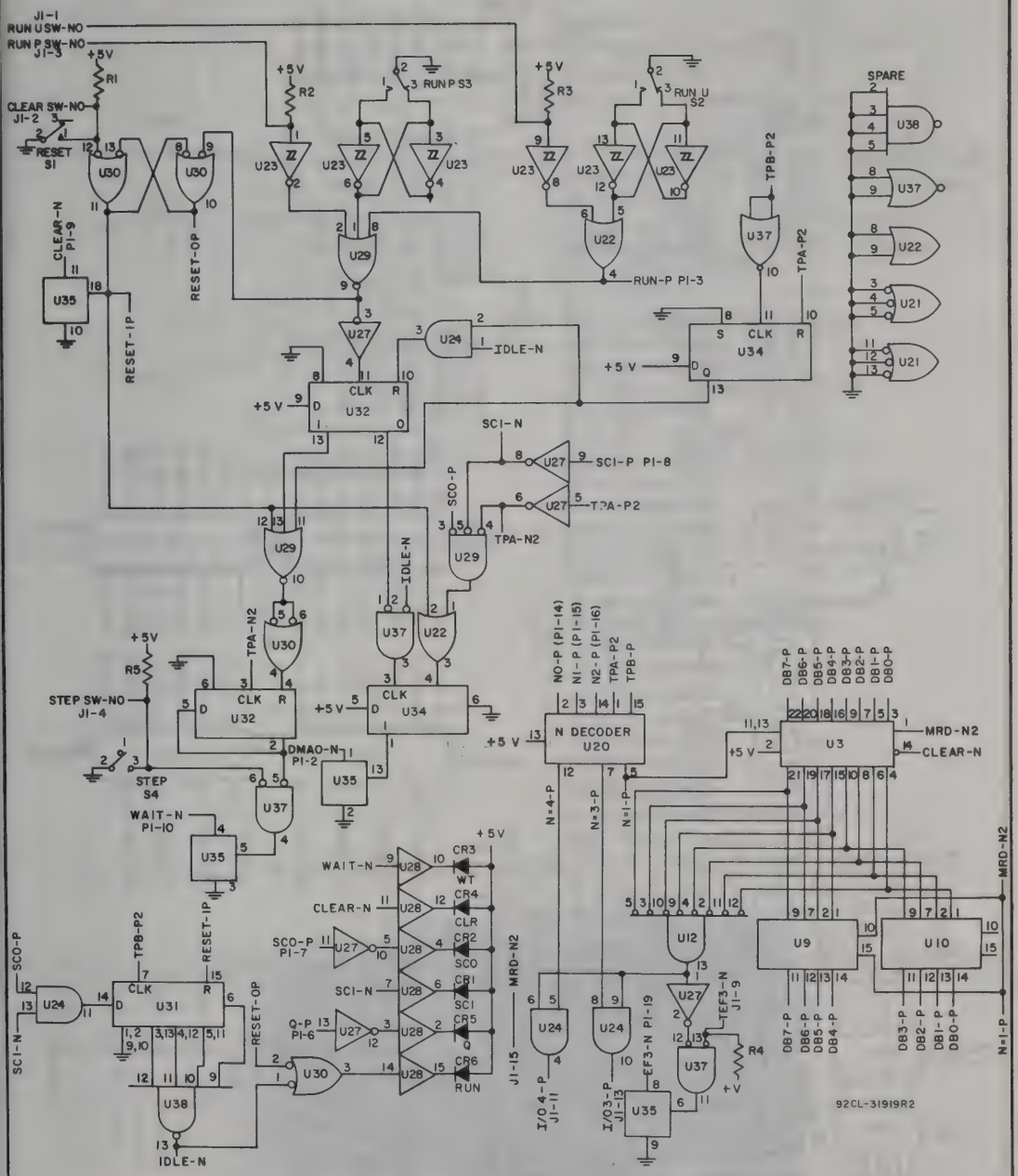
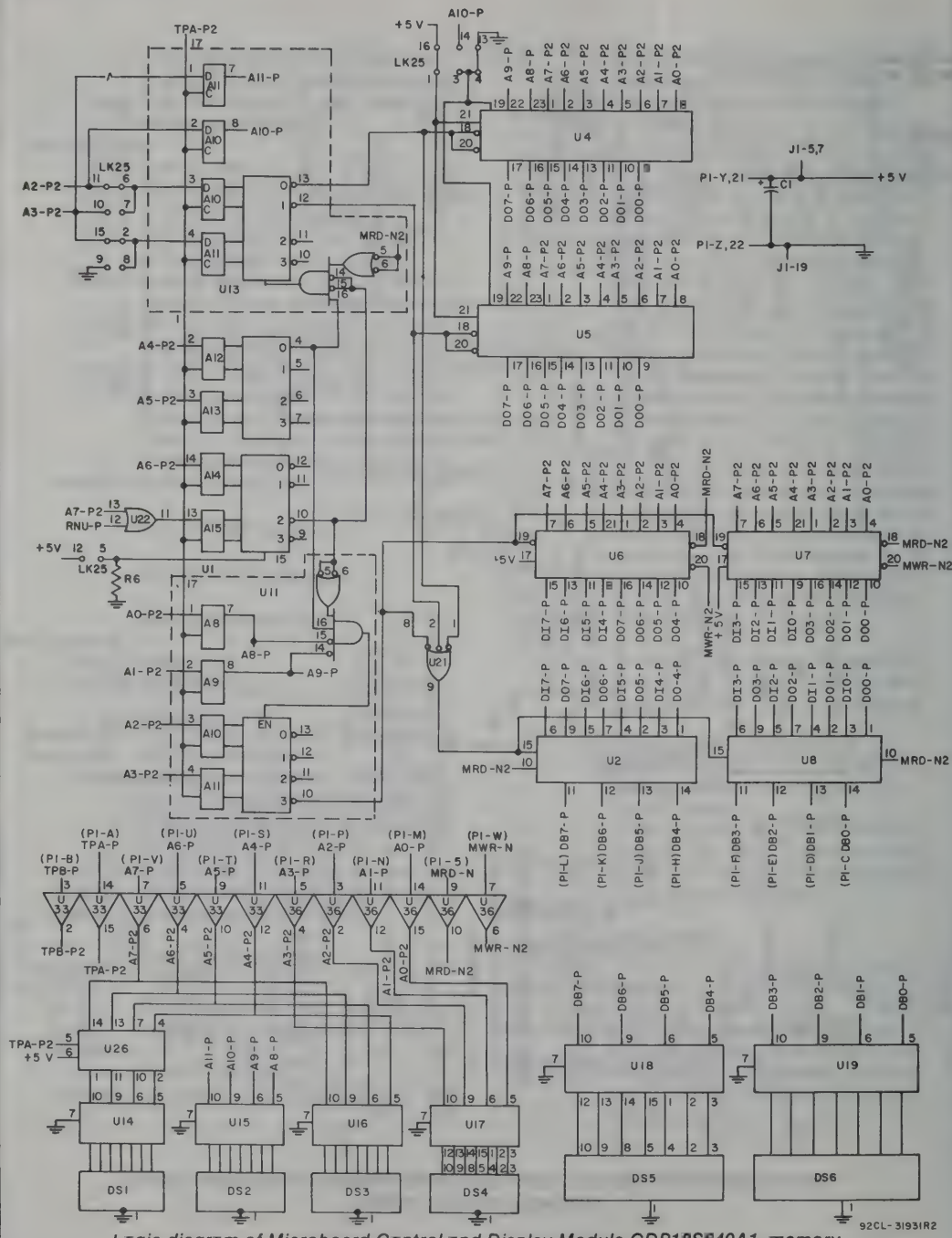


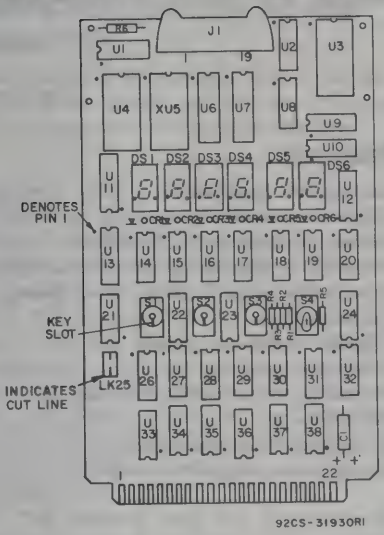
Logic diagram of Microboard Control and Display Module CDP18S640A1-control and status indicator portion.

CDP18S640A1



Logic diagram of Microboard Control and Display Module CDP18S640A1-memory and memory display portion.

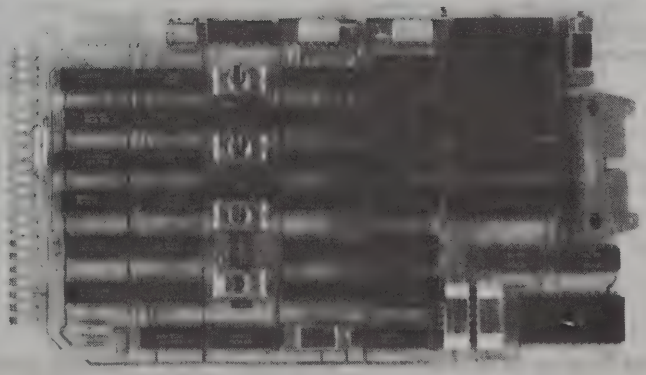
CDP18S640A1



Layout diagram of RCA Microboard Control and Display Module CDP18S640A1.

Parts List

C1=15 μF, 20 V
CR1-CR6=LED
DS1-DS6=7-segment display HP5082-7740
J1=connector, 20 pin
R1-R6=22 kΩ, ¼ W, 5%
S1, S2, S3=switch, momentary
S4=switch, SPDT
U1=CDP1858CE
U2, U8=CDP1856CE
U3=CDP1852CE
U4=Utility ROM UT61
U6, U7=MWS5101
U9, U10=CDP1857CE
U11, U13=CDP1866CE
U12=CD4078BE
U14-U19=MC14495P
U20=CDP1853CE
U21=CD4023BE
U22=CD4071BE
U23=CD40106BE
U24=CD4081BE
U26=CD4042BE
U27=CD4069BE
U28, U33, U36=CD4050BE
U29=CD4025BE
U30=CD4011BE
U31=CD4076BE
U32, U34=CD4013BE
U35=CD4016BE
U37=CD4001BE
U38=CD4012BE
XDS1-XDS6=DIP socket, 10 pin
XU4, XU5=IC socket, 24 pin



CDP18S641
RCA COSMAC Microboard UART Interface

The RCA COSMAC Microboard UART (Universal Asynchronous Receiver Transmitter) Interface Module CDP18S641 is a parallel-to-serial I/O data controller utilizing the RCA CDP1854A UART. The CDP18S641 is designed for use in a Microboard computer system or in the COSMAC Development Systems CDP18S005 and CDP18S007. It provides an efficient byte interface to the system while serial data are transmitted and received at the remote interface. Baud rates from 110 to 19,200 are switch-selectable. It provides for full-duplex operation.

The CDP18S641 also provides two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations.

Features

- Low-power static CMOS
- High noise immunity
- Small board size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with COSMAC Development Systems
- Flexible address assignment
- Selectable baud rate
- Selectable serial interface: RS232C or 20-mA loop
- Paper-tape-reader run control
- Temperature range: 0°C to 70°C

Specifications

UART
CDP1854A, programmed mode.

Parity
Even or odd, or inhibited.

Stop Bits
One or two.

Word Length
5, 6, 7, or 8 bits.

Baud Rate
Crystal-controlled, switch-selectable for 110, 300, 1200, 4800, 9600, or 19,200 baud.

Addressing
I/O space, link-selectable for both N codes and I/O group number.

Serial Interface
20-mA loop or RS232C.

Operating-Temperature Range
0°C to 70°C.

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm);
Board pitch - 0.5 inch (12.7 mm) minimum.

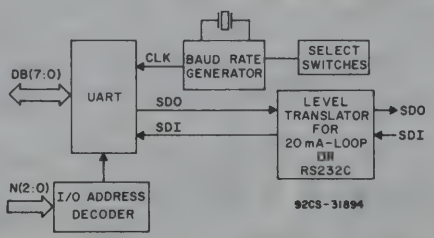
Power Requirements

Voltage (V)	With EIA RS232C Terminal	With 20-mA Loop Terminal
+5	2.0 mA	2.0 mA
−5 to −15	7.5 mA	38 mA
+12 to +15	8.5 mA	40 mA

Connectors

System interface: Edge fingers, 44 pins on 0.156-inch centers.

Serial interface: Two right-angle 10-pin headers to mate with connectors comprised of
housing - AMP 1-86148-2
contact - AMP 86016-1
keying plug - AMP 87077-1



Block diagram of RCA COSMAC Microboard UART Interface CDP18S641.

Microboard Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard UART Interface Module CDP18S641 makes use of the following signals in the Microboard Universal Bus Interface.

DB7 through DB0 - These eight bidirectional data bus lines communicate directly with the CDP1854A UART, which has internal controls to establish direction and timing. In addition, DB7 is used to set the paper-tape-reader control, and DB7 through DB0 are used, through a system of optional links, to define the I/O group chosen for this board.

N0, N1, N2 - The N lines, which define the primary I/O address, are wired to a CDP1853 decoder. The CDP1853 outputs 7 through 1 are connected through optional links to the CDP1854A UART.

MRD - The Memory Read line is used by the CDP1854A UART to identify proper direction of data flow on the bidirectional data bus. When true, this line indicates that data are being read from memory and, therefore, written to the I/O device, if an I/O operation is in progress. The direction is reversed when MRD is false.

TPA - This timing pulse is used only by the N decoder to set its output enable at the trailing edge of TPA.

TPB - This timing pulse is used by the CDP1854A UART to latch data written to it. It is also used by the N decoder to terminate its output enable at the trailing edge of TPB.

INT - This signal may be connected by optional link LK24 pins 1 and 14 to the INT output from the CDP1854A UART. This signal is buffered by a transmission gate so that wired-"OR" connection may be made with other devices driving the backplane INT line.

EF1, EF2, EF3, EF4 - Links are provided (link LK24) so that these flag lines may be wired to outputs from the CDP1854A UART. The outputs are Data Available (DA), Transmitter Holding Register Empty (THRE), Overrun Error or Parity Error (OE/PE), Framing Error (FE), and Serial Data In (SDI).

CLEAR - This signal provides an initialization signal for the CDP1854A UART and resets the paper-tape-motor control.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard UART CDP18S641.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal	
A	TPA-P	*	1	DMAI-N	
B	TPB-P	*	2	DMAO-N	
C	DB0-P	*	3	RNU-P	
D	DB1-P	*	4	INT-N	*
E	DB2-P	*	5	MRD-N	*
F	DB3-P	*	6	Q-P	
H	DB4-P	*	7	SC0-P	
J	DB5-P	*	8	SC1-P	
K	DB6-P	*	9	CLEAR-N	*
L	DB7-P	*	10	WAIT-N	
M	A0-P		11	−5 V/−15 V	*
N	A1-P		12	SPARE	
P	A2-P		13	CLOCK OUT	
R	A3-P		14	N0-P	*
S	A4-P		15	N1-P	*
T	A5-P		16	N2-P	*
U	A6-P		17	EF1-N	*
V	A7-P		18	EF2-N	*
W	MWR-N		19	EF3-N	*
X	EF4-N	*	20	+12 V/+15 V	*
Y	+5 V	*	21	+5 V	*
Z	GND	*	22	GND	*

*Signals used on RCA COSMAC Microboard UART Interface CDP18S641.

Operation

The operation of the RCA COSMAC Microboard UART Interface CDP18S641 can be understood by reference to the logic diagrams. Reference should also be made to the technical data sheet for the

CDP18S641

CDP1854A UART (U10 on the logic diagram) for Mode 1 operation details.

The crystal-controlled oscillator circuit and the divide-by-N counter CD4059AE (U4) provide a clock for the UART at a frequency 16 times the rate selected by the user via the baud rate switch (S1), as required by the UART.

The clear-to-send-in signal CTS-IN from the connector J2 to the UART may be left floating, if desired, and it will assume the true state at the UART. The clear-to-send-out signal CTS-OUT is driven by the data available signal DA from the UART with a trailing edge delay. This signal may be used for handshaking, for example, between two UART modules. This output may be made true all the time by changing link LK18 to the A position.

Any communication with the UART Interface CDP18S641, or with any Microboard I/O Controller, must be started by the transmittal of the I/O group select number assigned to the controller. The system software transmits the group number by issuing an OUT1 (61_{16}) command whose data is the group number desired. This group number then stays selected until another OUT1 command supersedes it. Group number assignment details are given in the next section on **Installation.**

To operate the paper-tape reader, the system software should issue an output instruction 67 with the data byte containing a 1 in bit seven (most significant bit). The CD4096BE J-K flip-flop (U16) is triggered to the set state by this command, making the signal PT RDR low, thus enabling the tape reader. As soon as the reader starts to transmit data, the signal Serial Data In (SDI) causes the J-K flip-flop (U16) to be triggered to the reset state. As a result, one byte is transmitted to the UART and the tape is stopped before the next byte. Another 67 instruction, therefore, must be issued for each successive byte.

Installation in a Microboard Computer System

Installation of the Microboard UART Interface CDP18S641 in a Microboard Computer System requires only the setting of the proper baud rate switch (S1), as marked, unless the preselected addresses are not appropriate. The preselected addresses are as follows:

I/O GROUP = 02_{16}
DATA INPUT = IN2 ($6A_{16}$)
DATA OUTPUT = OUT2 (62_{16})
STATUS INPUT = IN3 ($6B_{16}$)
CONTROL OUTPUT = OUT3 (63_{16})
FLAG AND INTERRUPT LINES ARE OPEN

A system of link positions is provided so that the user can select variations of the above functions. The links are arranged and numbered in a DIP configuration for ease of identification and to allow installation of DIP switches, headers, or other aids in the event frequent changes are anticipated.

For changes in the I/O group assignment, refer to Table II for links LK5 and LK14.

The primary addresses for data transfer and status/control transfer are prewired for Input/Output 2 and Input/Output 3, respectively. Should different I/O instructions be required, Link LK20 should be wired as follows.

For data transfer, wire link LK20 pin 4 to:

Pin 11 = INPUT 2, OUTPUT 2
Pin 9 = INPUT 3, OUTPUT 3
Pin 14 = INPUT 4, OUTPUT 4
Pin 12 = INPUT 5, OUTPUT 5
Pin 10 = INPUT 6, OUTPUT 6
Pin 8 = INPUT 7, OUTPUT 7

For status in or control out, wire link LK20 pin 6 to:

Pin 11 = INPUT 2, OUTPUT 2
Pin 9 = INPUT 3, OUTPUT 3
Pin 14 = INPUT 4, OUTPUT 4
Pin 12 = INPUT 5, OUTPUT 5
Pin 10 = INPUT 6, OUTPUT 6
Pin 8 = INPUT 7, OUTPUT 7

Link LK24 provides a means of connecting the UART interrupt to the system interrupt, as well as the UART status bits to the external flags EF1 through EF4 of the system. The interrupt is then unconditioned, but the flags are enabled by the group select. Thus, an interrupt-identification polling scheme may be implemented by system software. Polling may also be accomplished by reading status from the UART, if the user does not wish to connect the links for status or interrupt. Connections for selecting interrupt or any of the status bits may be identified on the logic diagram.

Installation in a COSMAC Development System CDP18S005 or CDP18S007

Installation in the CDS II (CDP18S005) or the CDS III (CDP18S007) is the same as for installation in a Microboard computer system except that the Development System backplane must have certain signals wired to the UART location. The user should select an empty slot in the I/O section (slots 19 and 20 should be avoided), and then install the following wires in that slot.

Pin 9 to pin 13	RESET-OP
Pin 14 to Slot 13 pin 14	N0-P
Pin 15 to Slot 13 pin 15	N1-P
Pin 16 to Slot 13 pin 16	N2-P

Table II - I/O Group Select Link Connections

I/O	LK5								LK14				
Group	1-16	3-14	5-12	7-10	2-15	4-13	6-11	8-9	1-10	2-9	3-8	4-7	5-6
01	O	O	O	S	S	S	S	O	O	O	O	O	S
02*	O	O	O	S	S	S	S	O	O	O	O	S	O
04	O	O	O	S	S	S	S	O	O	O	S	O	O
08	O	O	O	S	S	S	S	O	O	S	O	O	O
10	O	O	O	S	S	S	S	O	S	O	O	O	O
20	O	O	S	O	S	S	O	S	S	O	O	O	O
30	O	O	S	S	S	S	O	O	S	O	O	O	O
40	O	S	O	O	S	O	S	S	S	O	O	O	O
50	O	S	O	S	S	O	S	O	S	O	O	O	O
60	O	S	S	O	S	O	O	S	S	O	O	O	O
70	O	S	S	S	S	O	O	O	S	O	O	O	O
80	S	O	O	O	O	S	S	S	S	O	O	O	O
90	S	O	O	S	O	S	S	O	S	O	O	O	O
A0	S	O	S	O	O	S	O	S	S	O	O	O	O
B0	S	O	S	S	O	S	O	O	S	O	O	O	O
C0	S	S	O	O	O	O	S	S	S	O	O	O	O
D0	S	S	O	S	O	O	S	O	S	O	O	O	O
E0	S	S	S	O	O	O	O	S	S	O	O	O	O
F0	S	S	S	S	O	O	O	O	S	O	O	O	O

*Group 02 is preprinted. O = Open S = Shorted

CDP18S641

Parts List

C1, C2, C3 = 15 μF, 50 V
C4 = 0.33 μF, 50 V

CR1 – CR7 = 1N914

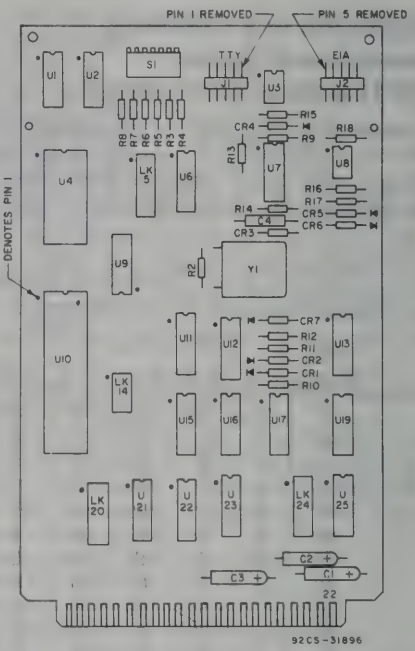
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP 86016-1, keying plug — AMP 87077-1, or equivalent)

R2 = 10 MΩ, ¼ W
R3 – R8 = 22 kΩ, ¼ W
R9 = 910 Ω, ¼ W
R10, R15 = 10 kΩ, ¼ W
R11, R16 = 47 kΩ, ¼ W
R12 = 4.7 kΩ, ¼ W
R13, R14 = 470 Ω, ¼ W
R17 = 4.3 kΩ, ¼ W
R18 = 560 Ω, ¼ W

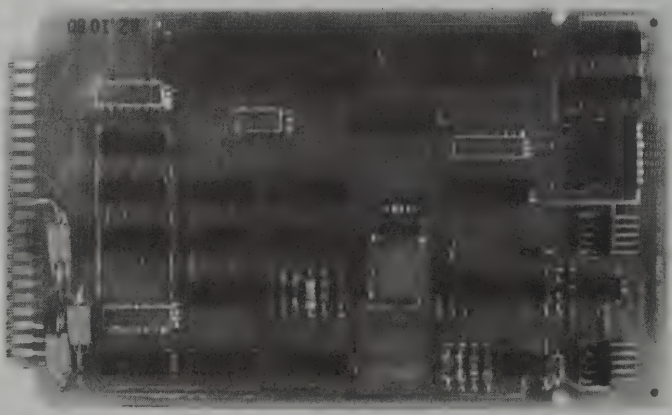
S1 = 7-position DIP

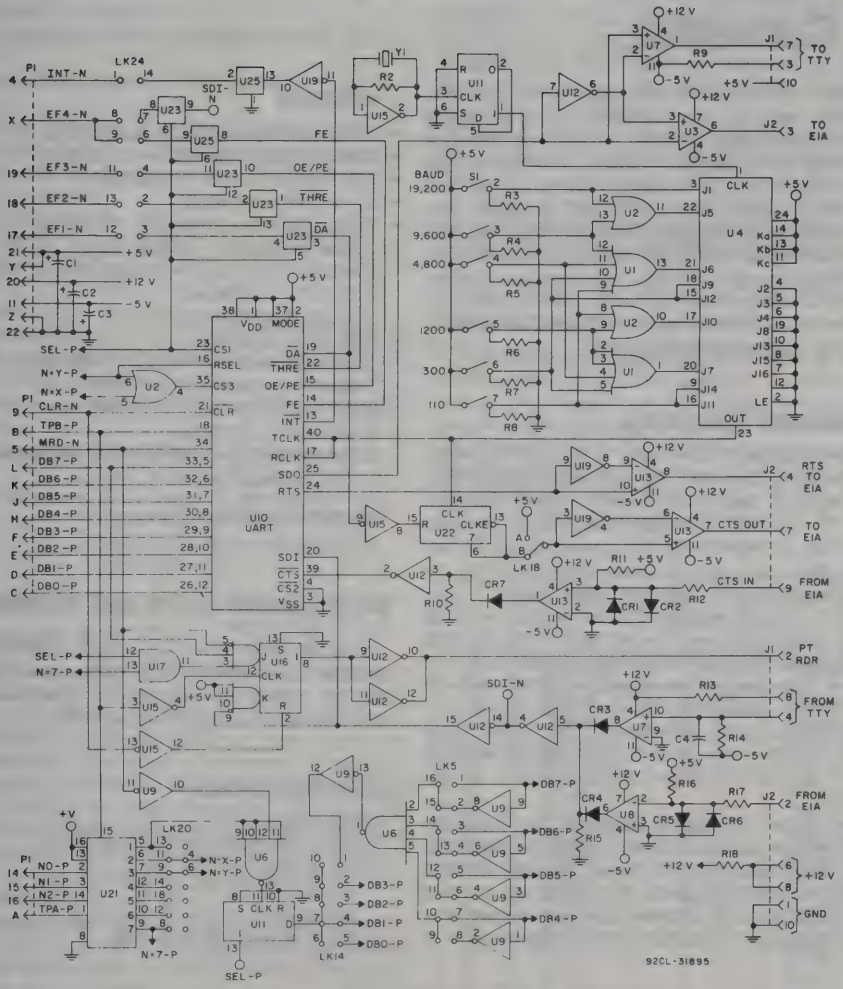
U1 = CD4072BE
U2 = CD4071BE
U3, U8 = CA3140E
U4 = CD4059AE
U6 = CD4012BE
U7, U13 = CA324E
U9, U15, U19 = CD4069BE
U10 = CDP1854ACE
U11 = CD4013BE
U12 = CD4049BE
U16 = CD4096BE
U17 = CD4081BE
U21 = CDP1853CE
U22 = CD4017AE
U23, U25 = CD4016BE

Y1 = 1.8432-MHz crystal



Layout diagram of RCA COSMAC Microboard UART Interface Module CDP18S641.





Logic diagram of RCA COSMAC Microboard UART Interface Module CDP18S641.

CDP18S642
RCA COSMAC Microboard D/A Converter

The RCA COSMAC Microboard D/A Converter CDP18S642 includes two complete digital-to-analog conversion systems having 12-bit or 8-bit resolution. It incorporates hybrid digital-to-analog converters with CMOS control logic to minimize power-supply and cooling requirements. The CDP18S642 provides two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations. It is designed for use in a Microboard computer system and is plug-in compatible with the COSMAC Development Systems CDP18S005 and CDP18S007 to facilitate hardware and software development.

Component Features

Digital-to-Analog Converters. The two twelve-bit digital-to-analog converter components contain fast-settling switches and stable, laser-trimmed thin-film resistors to provide user-selectable output voltage ranges. Trim potentiometers are provided for adjustment of gain and offset. Each converter may be operated independently under software control.

The ±15 volts dc required by the digital-to-analog converter components may be supplied either through the Microboard Universal Backplane connector (P1) or through a user-supplied on-board converter such as Analog Devices Model 940. This converter has an output of ±15 volts at 100 milliamperes. This output is sufficient for the operation of both the CDP18S642 D/A Converter and a CDP18S643 A/D Converter at the same time.

Control Logic. The digital inputs to the digital-to-analog converter components are stored in two 12-bit registers. These registers are buffered from the data bus by an 8-bit and a 4-bit register. The digital input codes, output modes, and I/O addresses are link-selected. The links are arranged in standard DIP configurations so that link selection may be made by DIP switches if desired by the user.

Link Selection. Links LK1, LK2, LK3, and LK4 are arranged in a standard DIP configuration so that DIP switches or DIP headers may be installed if the user desires a rapid link-selection capability.

Features

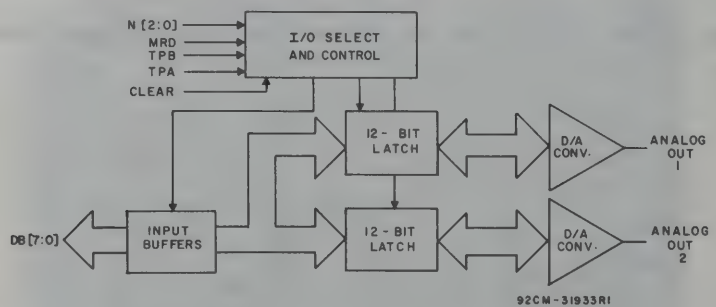
- Low-power static CMOS control logic
- Operable from a single 5-volt supply†
- Two independent D/A channels
- 12- or 8-bit resolution
- Assignable I/O addresses
- Bipolar or unipolar voltage output
- Selectable input codes—straight binary, offset binary, and two's complement
- Locking output connector
- High noise immunity
- Compatible with COSMAC Development Systems
- Temperature range: 0°C to 70°C
- Small board size (4.5 × 7.5 inches)
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane

†With customer-supplied on-board converter

Specifications

Analog Output

Number of channels: 2 independent
Output ranges at ±5 mA:
Bipolar: ±2.5 V, ±5 V, ±10 V
Unipolar: 0 to +5 V, 0 to +10 V
Output impedance: 0.05 ohm



Block diagram of RCA COSMAC Microboard D/A Converter CDP18S642.

Transfer Characteristics
Resolution: 12 or 8 bits
Settling time to ±0.01% of full-scale range: 5 μs max.
Gain and offset: hardware adjustable
Accuracy
Linearity error at 25°C: ± ½ least significant bit max.
Total bipolar drift: ±25 ppm of full-scale range/°C
Power supply sensitivity: 0.02% of full-scale range /% supply volts
Operating Temperature Range
0°C to 70°C
Dimensions
4.5 inches × 7.5 inches (114.3 mm × 190.5 mm)
Board pitch: 0.5 inch (12.7 mm) minimum
Power Requirements
Without converter: +5 V at 26 mA; and, ±15 V at ±50 mA (typical)
With converter (Model 940): 5 V at 200 mA (typical)
Connectors
System interface: Edge fingers, 44 pins on 0.156-inch centers
Analog interface: Right-angle 10-pin header with locks. Berg part No. 65823-049. Mates with Berg connector No. 65847-003/004.

Microboard Bus Interface Signals (Connector P1)

The following signals are received by the COSMAC Microboard D/A Converter CDP18S642. For additional information on these signals, refer to the published data on the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201. The signals are summarized in Table I which gives a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard D/A Converter CDP18S642.

DB7 through DB0 - Eight bidirectional data bus lines. Taken directly from the CPU bus, these lines transfer the data to be converted and the control data from the CPU to the D/A Converter.

N0, N1, N2 - Taken directly from the CPU pins, these lines indicate that an I/O instruction is being executed. They are derived from the three low-order bits of the N register and are valid only during an I/O instruction. The D/A Converter CDP18S642 decodes these lines to control the transfer of data from the data bus to the hybrid D/A converter components on board.

$\overline{\text{MRD}}$ - Derived from the most significant bit of the N register, this signal defines the direction of the I/O data transfer. A low level indicates a transfer from memory to I/O.

TPA, TPB - Timing pulses generated by the CPU which occur once in each machine cycle. TPA is used by the D/A Converter CDP18S642 to enable the signal that transfers data from the buffer registers into the 12-bit data latches. The trailing edge of TPB is used to latch data from the data bus.

CLEAR - A low level on this line indicates a system reset. The leading edge of the clear signal resets the input buffers, causing their outputs to go to a high level. The 12-bit data latches are clocked by TPA of the first cycle following the clear, causing the output of each of the two D/A converter components to go to zero volts.

Operation of the CDP18S642 D/A Converter

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the three low-order bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of the data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal	Pin	Signal
A	TPA-P *	1	DMAI-N
B	TPB-P *	2	DMAO-N
C	DB0-P *	3	RNU-P
D	DB1-P *	4	INT-N
E	DB2-P *	5	MRD-N *
F	DB3-P *	6	Q-P
H	DB4-P *	7	SC0-P
J	DB5-P *	8	SC1-P
K	DB6-P *	9	CLEAR-N*
L	DB7-P *	10	WAIT-N
M	A0-P	11	−5 V/−15 V*
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P *
S	A4-P	15	N1-P *
T	A5-P	16	N2-P *
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MWR-N	19	EF3-N
X	EF4-N	20	+12 V/+15 V*
Y	+5 V *	21	+5 V *
Z	GND *	22	GND *

*Signals used on RCA COSMAC Microboard D/A Converter CDP18S642.

CDP18S642

device or as I/O commands to different devices as addressed by the N lines.

In the Microboard system, the following conventions are established.

- The 61 output instruction is used to transmit a group select number. The output byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts. The lower four bits are linearly encoded and the upper four bits are binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the 6 commands left after reserving the 61 and 69 instructions. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S642 does not provide this feature.

Data Transfers. The D/A Converter CDP18S642 is pre-assigned by links to group 30. To enable the D/A Converter, a 61 instruction followed by the hex data 30 is required. Once the CDP18S642 has been selected, additional I/O instructions, as discussed below, will load the buffers and begin conversion.

- 62 instruction - Loads the four least significant bits of the binary data into the 4-bit input buffer. These bits are contained in the upper four bits of the output byte.

  2^7 ... 2^0
  $b_3\ b_2\ b_1\ b_0\ x\ x\ x\ x$

- 63 instruction - Loads the eight most significant bits of the binary data into the 8-bit input buffer.

  2^7 ... 2^0
  $b_{11}\ b_{10}\ b_9\ b_8\ b_7\ b_6\ b_5\ b_4$

- 64 instruction - Transfers the data from the input buffers into the appropriate data latch and begins conversion. The output byte determines which of the two D/A converter and latch channels is selected.

  2^7 ... 2^0
  $x\ x\ x\ x\ x\ x\ d_1\ d_0$

  $d_0 = 1$ selects channel 2
  $d_1 = 1$ selects channel 1
  x = don't care

The CDP18S642 D/A Converter and the CDP18S643 A/D Converter are both prelinked to group 30. This linking allows both boards to be selected simultaneously. Furthermore, there is no overlap of I/O commands between them. Should a change in I/O address be necessary, Table II lists the addresses and required links.

Table II - I/O Select Code Connections

I/O Select Code	Link LK3 Pin Connections
10	4:5
20	3:6
30 *	3:6, 4:5
40	2:7
50	2:7, 4:5
60	2:7, 3:6
70	2:7, 3:6, 4:5
80	1:8
90	1:8, 4:5
A0	1:8, 3:6
B0	1:8, 3:6, 4:5
C0	1:8, 2:7
D0	1:8, 2:7, 4:5
E0	1:8, 2:7, 3:6
F0	1:8, 2:7, 3:6, 4:5

*LK3 is pre-linked for select code 30.

Digital Input/Analog Output Selection. The CDP18S642 accepts any of the following **input** codes:

straight binary (SB)
offset binary (OB)
two's complement (TC)

Straight binary is used for unipolar operation; offset binary and two's complement are used for bipolar operation. In these latter two codes, the most significant bit indicates the sign of the output from the CPU and the input to the CDP18S642. The analog output of the CDP18S642 as a function of the digital input is given in Table III for the three codes.

The digital input code and the analog output voltage range are link-selectable. The link connections are summarized in Table IV. Both channels of the D/A Converter CDP18S642 are prelinked for ±10-volt TC (two's complement) operation.

Table III - Analog Output of the CDP18S642 as a Function of the Digital Input

Inputs			Output
Straight Binary	Offset Binary	Two's Complement	
111111111111	111111111111	011111111111	+FS
000000000000	100000000000	000000000000	0
——	011111111111	111111111111	−1 LSB
——	000000000000	100000000000	−FS

FS = 2.5, 5.0, or 10.0 volts.

Table IV - Digital Input/Analog Output Links

Input Output Mode Voltage	Link LK1/LK2	Link LK4
TC ±10 V	8:9, 3:14, 4:13	3:6, 4:5*
TC ±5 V	8:9, 3:14, 5:12	3:6, 4:5
TC ±2.5 V	8:9, 1:16, 3:14, 5:12	3:6, 4:5
OB ±10 V	8:9, 3:14, 4:13	1:8, 2:7
OB ±5 V	8:9, 3:14, 5:12	1:8, 2:7
OB ±2.5 V	8:9, 1:16, 3:14, 5:12	1:8, 2:7
SB 0 to +10 V	8:9, 2:15, 5:12	1:8, 2:7
SB 0 to +5 V	8:9, 1:16, 2:15, 5:12	1:8, 2:7

*LK4 is pre-linked for TC ± 10 V.

The **analog outputs** are available at the printed edge connector P2. The pin assignments are given in Table V.

Gain and Offset Adjustments. Potentiometers are provided on the CDP18S642 for both gain and offset adjustments. For channel 1, potentiometer R8 adjusts the gain and R4 adjusts the offset. For channel 2, R7 adjusts the gain and R3 adjusts the offset.

Table VI lists the typical digital input codes and their corresponding output voltages for 12-bit resolution. The user should adjust the **gain** for either unipolar or bipolar operation by first applying the digital input, as given in Table VI, that indicates the maximum positive output voltage and then adjusting the appropriate gain potentiometer to achieve this voltage.

Table V - Analog Outputs—Connector P2 Pin Assignments

Channel 1 Output	P2-2
Channel 2 Output	P2-9
Grounds	P2-1, 3, 7, 8, 10
No Connections	P2-4, 5, 6

The **offset** adjustment is dependent upon the output mode. For unipolar modes, the user should apply the digital input code from Table VI that indicates zero output and then adjust the appropriate offset potentiometer to achieve zero output. For bipolar modes, the user should apply the digital input code from Table VI that indicates the maximum negative output and then adjust the appropriate offset potentiometer to achieve that output.

Operation at ±15 Volts from 5-Volt Supply. An area is provided on the CDP18S642 for the mounting of a dc-to-dc converter to obtain the ±15-volt power from the +5-volt supply. The ±15 volts is connected to the backplane through links LK5 and LK6. **These links are preprinted with the assumption that the remainder of the system is not using +12 volts or −5 volts. If there is a contention, these links must be opened.**

Installation in the COSMAC Development Systems

The CDP18S642 may be installed into any of the available I/O slots (14-18 or 21-23) in the COSMAC Development System (CDS II) CDP18S005 or in the COSMAC DOS Development System (CDS III) CDP18S007 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may be easily allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

Table VI - Digital Input/Analog Output Signals

Digital Input to D/A Converter*	0 to +10 V	0 to +5 V	±10 V	±5 V	±2.5 V
111111111111	0.0000 V	0.0000 V	−10.0000 V	−5.0000 V	−2.5000 V
100000000000	+4.9976 V	+2.4988 V	−0.0049 V	−0.0024 V	−0.0012 V
011111111111	+5.0000 V	+2.5000 V	0.0000 V	0.0000 V	0.0000 V
000000000000	9.9976 V	+4.9988 V	+9.9951 V	+4.9976 V	+2.4988 V
ONE LSB	2.44 mV	1.22 mV	4.88 mV	2.44 mV	1.22 mV

*The input to the D/A converter (U1 or U2) is determined by the digital code being used. The words on the CPU data bus are inverted by the buffer registers.

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When the CDP18S642 is installed in a COSMAC Development System, links LK5 and LK6 must be connected as shown in Table VII. Additionally, the system signals indicated in Table VIII must be connected to the slot on the CDS selected for the CDP18S642.

*Table VII - ± 15-Volt Bus Connections**

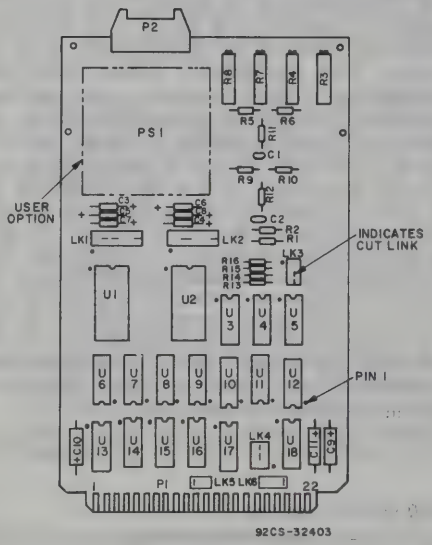
Link	Microboard Chassis	CDS
LK5	C:D CLOSED	A:B CLOSED
LK5	A:B OPEN	C:D OPEN
LK6	A:B CLOSED	C:D CLOSED
LK6	C:D OPEN	A:B OPEN

*These connections are required when the ± 15-volt power is supplied from the backplane. If a dc-to-dc converter is used, the connections may be left open.

*Table VIII - CDS Backplane Connections**

Signal	Jumper to Pin
N0-P	P1-14
N1-P	P1-15
N2-P	P1-16
CLEAR-N	P1-9
− 15 V	P1-N
+ 15 V	P1-V

*These connection are required when the ± 15-volt power is supplied from the backplane. If a dc-to-dc converter is used, the connections may be left open.

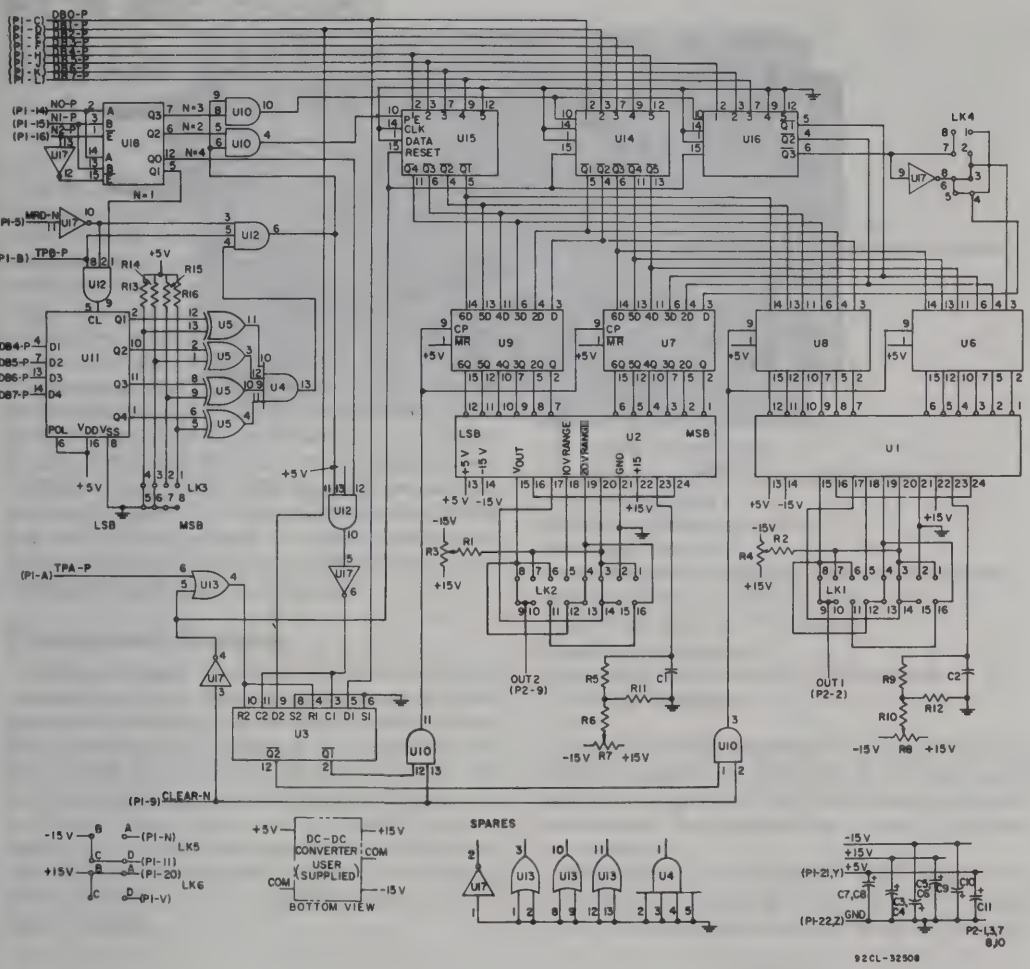


Parts List

C1, C2 = 0.01 μF, 100 V
C3 - C8 = 1 μF, 35 V
C9 - C11 = 15 μF, 50 V
P2 = Connector, 10 position
*PS1 = dc-to-dc converter, Analog Devices Model 940, or equiv.
R1, R2, R11, R12 = 3.9 MΩ, ¼ W
R3, R4, R7, R8 = 50 kΩ, variable
R5, R6, R9, R10 = 270 kΩ, ¼ W
R13 - R16 = 22 kΩ, ¼ W
U1, U2 = 2470869 (D/A converter)
U3 = CD4013BE
U4 = CD4082BE
U5 = CD4070BE
U6 - U9 = CD40174BE
U10 = CD4081BE
U11 = CD4042BE
U12 = CD4073BE
U13 = CD4071BE
U14 - U16 = CD4018BE
U17 = CD4069BE
U18 = CD4555BE

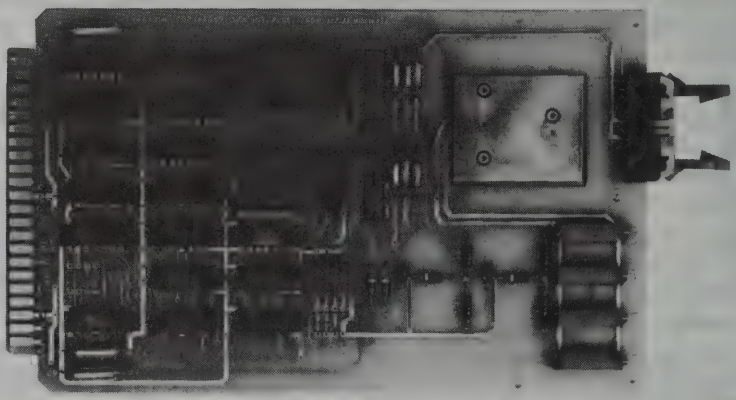
*User option.

CDP18S642



Logic diagram of RCA COSMAC Microboard D/A Converter CDP18S642.

CDP18S642



CDP18S643A

RCA Microboard A/D Converter

The RCA Microboard A/D Converter CDP18S643A is a complete analog-to-digital conversion system having 12-bit or 8-bit resolution. It incorporates a hybrid programmable-gain amplifier and analog-to-digital converter with CMOS control logic to minimize power-supply and cooling requirements. The CDP18S643A provides two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations. The CDP18S643A is designed for use in a Microboard computer system, is expandable by use of the RCA Microboard Universal Backplane, and is plug-in compatible with the RCA Prototyping Systems CDP18S691 and CDP18S692, the RCA Development Systems CDP18S005 (CDSII) and CDP18S007 (CDSIII), and the RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate hardware and software development.

Component Features

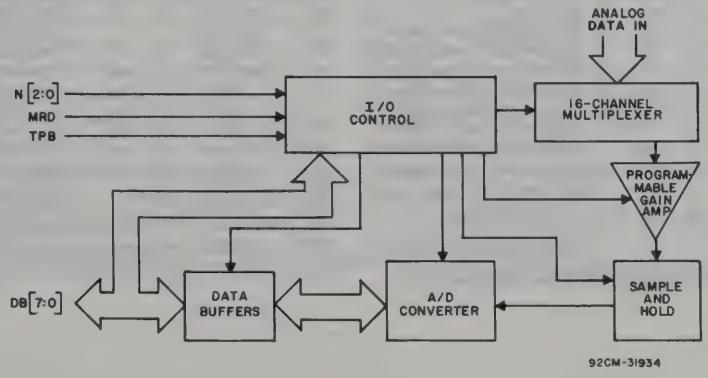
Analog-to-Digital Converter. The analog-to-digital converter is a 12-bit successive-approximation hybrid component containing laser-trimmed thin-film resistors and an internal voltage reference. Trim potentiometers are provided for adjustment of gain and offset. The converter accepts unipolar and bipolar input signals up to 10 volts. Faster conversions are possible by short-cycling or by reducing the resolution to 8 bits. Crystal-controlled oscillator and counter are provided to generate the required delay before conversion to allow the input signal to stabilize.

Features

- **Low-power static CMOS control logic**
- **Multiplexed inputs: 16 single-ended or 8 differential**
- **Scanned or fixed-input mode**
- **Programmable-gain amplifier**
- **Sample and hold**
- **12-bit or 8-bit resolution**
- **Short cycle mode**
- **Short delay mode**
- **Bipolar or unipolar voltage input**
- **Assignable I/O addresses**
- **Output code: straight binary, offset binary, and two's complement**
- **Ribbon-cable input connector**
- **High noise immunity**
- **Compatible with 1800-Series Development Systems**
- **Temperature range: -25° C to 85° C**
- **Small board size (4.5 x 7.5 inches)**
- **Simple system interface**
- **Expandable by use of the RCA Microboard Universal Backplane**

Sample-and-Hold Amplifier. The sample-and-hold amplifier acquires and holds up to ±10-volt analog signals to an accuracy of ±0.01% of full-scale reading in 5 microseconds. The maximum droop rate is 0.5 millivolt per millisecond.

Programmable-Gain Amplifier. The programmable-gain amplifier is a hybrid differential-input amplifier whose gain can be programmed to one of eleven binary-



Block diagram of RCA Microboard A/D Converter CDP18S643A

CDP18S643A

weighted steps from 1 to 1024 volts per volt. The gain and input channel can be selected with a single output instruction thereby allowing the CDP18S643A to handle a wide range of input signals. The on-board potentiometers provide offset adjustment of both the input and output stages of the programmable-gain amplifier.

Analog Multiplexer. The analog multiplexer stage consists of two CMOS 1-of-8 multiplexers that can be configured by the use of links to provide 16 single-ended channels or 8 differential-input channels. The break-before-make switches can be sequentially scanned or randomly selected under software control.

Control Logic. The CDP18S643A A/D Converter contains storage registers for gain, channel selection, resolution, and mode control. The outputs from the CDP18S643A are connected to the CPU bus by means of output instructions from the CPU. The two-level I/O decode logic allows the CDP18S643A to be selected and configured under software control.

Link Selection. Links LK1, LK2, LK3, and LK4 are arranged in a standard DIP configuration so that DIP switches or DIP headers may be installed if the user desires a rapid link-selection capability.

Specifications

Analog Input

Number of channels: 16 single-ended/8 differential

Input range: To ±10 volts

Gain range of programmable-gain amplifier:
1 to 1024 volts per volt in 11 binary steps, software selected

Gain range of analog-to-digital converter component: (link selected)
Bipolar: To ±2.5, ±5, ±10 volts
Unipolar: 0 to +5 volts, 0 to +10 volts

Gain and offset: adjustable

Transfer Characteristics

Resolution: 12 or 8 bits

Conversion time (12-bit):
Standard cycle: 275 μs
Short cycle: 105 μs

Common-mode rejection ratio (differential inputs): 90 dB

Accuracy

Linearity error at 25°C: less than 0.02% of full-scale reading

Table I - Pin Terminals and Signals for the RCA Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P *	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P *	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Request
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V *	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N *	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N *	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N *	In	External Flag
X	EF4-N *	In	External Flag	20	+12V/+15V *	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

92CS-34444

*Signals used on RCA Microboard A/D Converter CDP18S643A.

Total bipolar drift: ±30 ppm of full-scale reading/°C

Power supply sensitivity: ±0.003% of full-scale reading/% supply volts

Differential linearity: ±1/2 LSB

Operating Temperature Range

–25°C to 85°C

Dimensions

4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)

Board pitch: 0.5 inch (12.7 mm) minimum

Power Requirements

+5 volts at 85 mA (typical) and ±15 volts at 50 mA (typical)

Connectors

System interface: Edge fingers, 44 pins on 0.156-inch centers

Analog interface: Right-angle 20-pin header with locks. Berg Part No. 65823-067. Mates with Berg Connector No. 65847-021/022

Microboard Bus Interface Signals (Connector P1)

The following signals are received by the Microboard A/D Converter CDP18S643A. For additional information on these signals, refer to the published data on the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201. The signals are summarized in Table I which gives a list of the pins and the signals for the RCA Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA Microboard A/D Converter CDP18S643A.

DB7 through DB0 - Eight bidirectional data bus lines. Taken directly from the CPU bus, these lines transfer the data from the converter to the CPU and from the CPU to the control logic.

N0, N1, N2 - Taken directly from the CPU pins, these lines indicate that an I/O instruction is being executed. They are derived from the three low-order bits of the N-register and are valid only during an I/O instruction. The A/D Converter CDP18S643A decodes these lines to control the transfer of data between it and the data bus.

$\overline{\text{MRD}}$ - Derived from the most significant bit of the N register, this signal defines the direction of the I/O data transfer. A low level indicates a transfer from memory to I/O, and a high level a transfer from I/O to memory.

TPA, TPB - Timing pulses generated by the CPU which occur once in each machine cycle. TPB is used by the A/D Converter to clear the data-available line and to condition certain of the decoded I/O instructions.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$ - Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S643A uses one of these lines or the $\overline{\text{INT}}$ line to signal the CPU that the conversion is complete and that data is available. The particular line chosen is link-selectable, see Table II, but the $\overline{\text{EF1}}$ connection is preprinted.

Table II - CPU Lines Available for Conversion - Complete Signal

CPU Line	Link LK3	
EF1-N	1:10*	*Preprinted
EF2-N	2:9	
EF3-N	3:8	
EF4-N	4:7	
INT-N	5:6	

$\overline{\text{INT}}$ - Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited or enabled under software control. If Interrupt Enable (IE) is set, recognition of $\overline{\text{INT}}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as the program counter.

$\overline{\text{CLEAR}}$ - A low level on this line, indicating a system reset, clears the conversion-complete flip-flop, sets the resolution to 12 bits, sets the input mode to fixed, and selects channel 1.

Operation of the CDP18S643A A/D Converter

Two Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the three low-order bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of the data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In the Microboard system, the following conventions are established.

•The 61 output instruction is used to transmit a group

CDP18S643A

select number. The output byte is latched and decoded by any Microboard in the system having an I/O function.

•The group number is divided into two parts. The lower four bits are linearly encoded and the upper four bits are binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the 6 commands left after reserving the 61 and 69 instructions. The total number of useful I/O addresses is 114.

•The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S643A does not provide this feature.

Data Transfers. The A/D Converter CDP18S643A is pre-assigned by links to group 30. To enable the CDP18S643A a 61 instruction followed by the hex data 30 is required. Once the CDP18S643A has been selected, additional I/O instructions, as discussed below, will establish modes of operation, begin conversion, and read the data.

•The byte output by the 65 instruction specifies the input channel and amplifier gain and also begins a conversion cycle. The four most significant bits of the byte determine the gain as listed in Table VIII. The four least significant bits provide a binary selection of the input channel. When configured with differential inputs, the bit 3 (2^3) bit becomes a "don't care." When conversion is complete, the CDP18S643A signals the processor through a flag or interrupt line that valid data is available.

•The byte output by the 66 instruction specifies the resolution and the channel selection mode. The bits are encoded as follows:

(LSB) b_0: 0=12-bit resolution
1= 8-bit resolution
b_1: 0=fixed channel
1=sequential scanning
b_2–b_7=don't care

When the CDP18S643A receives a system-reset signal, the resolution is set to 12 bits, and the channel is set to fixed mode.

• The 6A instruction inputs the four least significant bits of the 12 data bits. These four bits become the four most significant bits on the CPU data bus. This instruction is not used in the 8-bit mode.

• The 6B instruction inputs the eight most significant bits of the 12 data bits. In addition, this instruction resets the data-available flag but does not initiate a conversion.

The 6C instruction also inputs the eight most significant bits of the 12 data bits and resets the data-available flag. In addition, it increments the channel if scanning is enabled and initiates another conversion after a 250-microsecond delay to allow the input signal to stabilize at the sample-and-hold device.

The 6D instruction is provided for those applications in which repetitive conversions are made on a single channel with no gain changes. This instruction inputs the eight most significant bits and initiates another conversion with an 80-microsecond delay for settling.

The CDP18S643A A/D Converter and the CDP18S642 D/A Converter are both prelinked to group 30. This linking allows both boards to be selected simultaneously. Furthermore, there is no overlap of I/O commands between them. Should a change in I/O address be necessary, Table III lists the addresses and the required links.

Table III - I/O Select Code Connections

I/O Select Code	Link LK1 Pin Connections
10	4:5
20	3:6
30*	3:6, 4:5
40	2:7
50	2:7, 4:5
60	2:7, 3:6
70	2:7, 3:6, 4:5
80	1:8
90	1:8, 4:5
A0	1:8, 3:6
B0	1:8, 3:6, 4:5
C0	1:8, 2:7
D0	1:8, 2:7, 4:5
E0	1:8, 2:7, 3:6
F0	1:8, 2:7, 3:6, 4:5

*LK1 is pre-linked for select code 30.

Digital Output/Analog Input Selection. The digital output codes that the CDP18S643A can produce may be any one of the following:

straight binary (SB)
offset binary (OB)
Two's complement (TC)

Straight binary is used for unipolar operation; offset binary and two's complement are used for bipolar operation. In these latter two codes, the most significant bit indicates the sign of the output from the CDP18S643A and the input to the CPU. The digital output of the CDP18S643A as a function of the input voltage is given in Table IV for the three codes.

Table IV - Digital Output of the CDP18S643A as a Function of Input Voltage

Input	Straight Binary	Outputs Offset Binary	Two's Complement
+FS	111111111111	111111111111	011111111111
0	000000000000	100000000000	000000000000
−1 LSB	—	011111111111	111111111111
−FS	—	000000000000	100000000000

FS=2.5, 5.0, or 10.0 volts.

The digital output code and the analog input voltage range are link selectable. The links are summarized in Table V. The CDP18S643A is prelinked for ±10-volt two's complement operation.

The **analog inputs**, available at the printed edge connector P2, may be configured as 16 single-ended inputs or as 8 differential inputs. The input mode, which is determined by link LK2 (see Table VI), is prelinked for differential inputs. The differential mode is the preferred one because it takes advantage of the common-mode rejection ratio of the programmable-gain amplifier to reduce line noise, especially in high-noise low-signal environments. The pin assignments for the two modes are listed in Table VII.

Table V - Analog Input/Digital Output Links

Output Mode	Input Voltage	Link LK4
TC	±10 V	2:13, 3:12, 6:9*
TC	±5 V	2:13, 3:12, 7:8
TC	±2.5 V	2:13, 3:12, 5:10, 7:8
OB	±10 V	1:14, 3:12, 6:9
OB	±5 V	1:14, 3:12, 7:8
OB	±2.5 V	1:14, 3:12, 5:10, 7:8
SB	0 to +10 V	1:14, 4:11, 7:8
SB	0 to +5 V	1:14, 4:11, 5:10, 7:8

*Preprinted link connections.

Table VI - Input Mode Selection

Input Mode	Link LK2
Single ended	2:13, 4:12, 5:10, 7:8
Differential	1:14, 3:12, 6:9*

*Preprinted link connections.

Table VII - Pin Assignments for Connector P2

Pin	Channel	
	Single-Ended	Differential
1	0	0
2	8	0−
3	1	1+
4	9	1−
5	2	2+
6	10	2−
7	3	3+
8	11	3−
9	4	4+
10	12	4−
11	5	5+
12	13	5−
13	6	6+
14	14	6−
15	7	7+
16	15	7−
17	GND	GND
18	GND	GND
19	GND	GND
20	PGA-OUT	PGA-OUT

Gain and Offset Adjustments. Potentiometers are provided on the CDP18S643A for both gain and offset adjustments. Because the programmable-gain amplifier uses laser-trimmed thin-film resistors, the need for any external gain adjustment is eliminated. Only offset adjustments are provided for the input and output stages to improve the tracking across the gain range.

The output of the **programmable-gain amplifier** is provided on pin 20 of connector P2 to facilitate these adjustments. With potentiometers R3 and R4 (refer to logic and layout diagrams) initially set at mid-range and a selected input channel shorted, the gain of the pro-

CDP18S643A

grammable-gain amplifier is programmed as indicated in Table VIII to 1 volt per volt. R3 is adjusted to reduce the output of the programmable-gain amplifier to zero. The gain is then programmed to 1024 volts per volt and R4 is adjusted to reduce the output at pin 20 of P2 to zero.

The A/D converter component is of the complementary type. The buffers between the converters and the CPU data bus produce an additional inversion so that the module will output uncomplemented code. The offset and gain of the A/D converter component (U12) are adjusted by the following method. By use of a software loop to perform repeated conversions, an analog signal that should produce all ones at the output of the converter component is selected from Table IX and applied to a selected channel. The data received by the CPU will be the complement of that indicated in Table VIII with the exception of the most significant bit. The most significant bit depends on the digital output code selected. The offset potentiometer R1 is adjusted until all ones are achieved. The analog input is then adjusted to the value as indicated in Table IX that should produce all zeroes at the converter component output, and the gain potentiometer R7 is adjusted until all zeroes are achieved. It should be noted that the buffers between the converters and the CPU data bus produce an additional inversion of the data.

Table VIII - Gain Selection Code for Programmable-Gain Amplifier (Byte output with 65 instruction)

Bits				Gain
b_7	b_6	b_5	b_4	V/V
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	4
0	1	0	0	4
0	1	0	1	8
0	1	1	0	16
0	1	1	1	16
1	0	0	0	32
1	0	0	1	64
1	0	1	0	128
1	0	1	1	128
1	1	0	0	256
1	1	0	1	512
1	1	1	0	1024
1	1	1	1	1024

±15-Volt Power. The ±15-volt power required by the CDP18S643A A/D Converter is supplied through the backplane and links LK5 and LK6. These links are preprinted with the assumption that the remainder of the system is not using +12 volts or –5 volts. See Table X for the ±15-volt bus link connections. The CDP18S642 D/A Converter is configured to accept a user-supplied dc/dc converter that can also supply ±15-volt power to the CDP18S643A A/D Converter.

Table X - ±15-Volt Bus Connections

Link	Microboard Chassis	CDS
LK5	A:B CLOSED C:D OPEN	C:D CLOSED A:B OPEN
LK6	A:B CLOSED C:D OPEN	C:D CLOSED A:B OPEN

Table IX - Analog Input/Digital Output Signals

Digital Output		Input Ranges				
MSB	LSB	±10 V	±5 V	±2.5 V	0 to +10 V	0 to +5 V
000000000000	+FS	9.9927 V	4.9963 V	2.4982 V	9.9963 V	4.9982 V
011111111111	0	0	0	0	+5.0000 V	+2.5000 V
111111111111	–FS	–10 V	–5 V	–2.5 V	0	0
ONE LSB		4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV

Installation in the RCA 1800-Series Development Systems

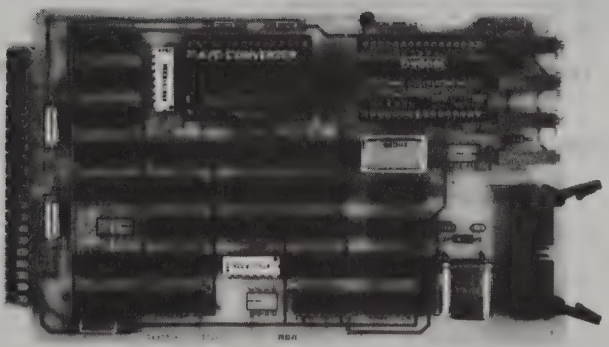
The CDP18S643A may be installed into any of the available I/O slots (14-18 or 21-23) in the Development System (CDS II) CDP18S005, DOS Development System (CDS III) CDP18S007, and in the Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may be easily allocated in place of ROM, thereby saving much time that might have been used in programming PROM's and EPROM's.

When a CDP18S643A is installed in the Development Systems, CDP18S005 or CDP18S007, links LK5 and LK6 must be connected as shown in Table X. In addition, the system signals indicated in Table XI must also be connected on the backplane to the I/O slot on the CDS selected for the CDP18S643A.

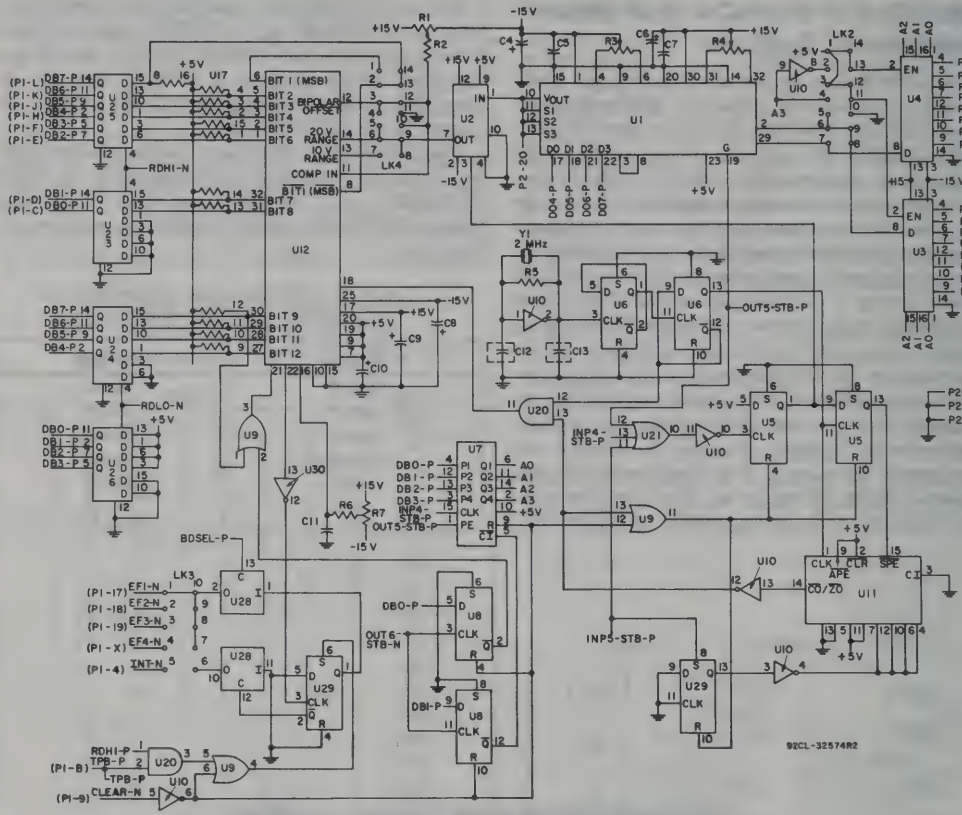
The CDP18S643A Microboard can be installed in the Microboard Computer Development Systems CDP18S693 and CDP18S694 and RCA Prototyping Systems CDP18S692 and CDP18S693 without any modifications.

Table XI - CDS Backplane Connections CDP18S005 and CDP18S007 only

Signal	Jumper
N0-P	P1-14
N1-P	P1-15
N2-P	P1-16
CLEAR-N	P1-9
−15 V	P1-N
+15 V	P1-V

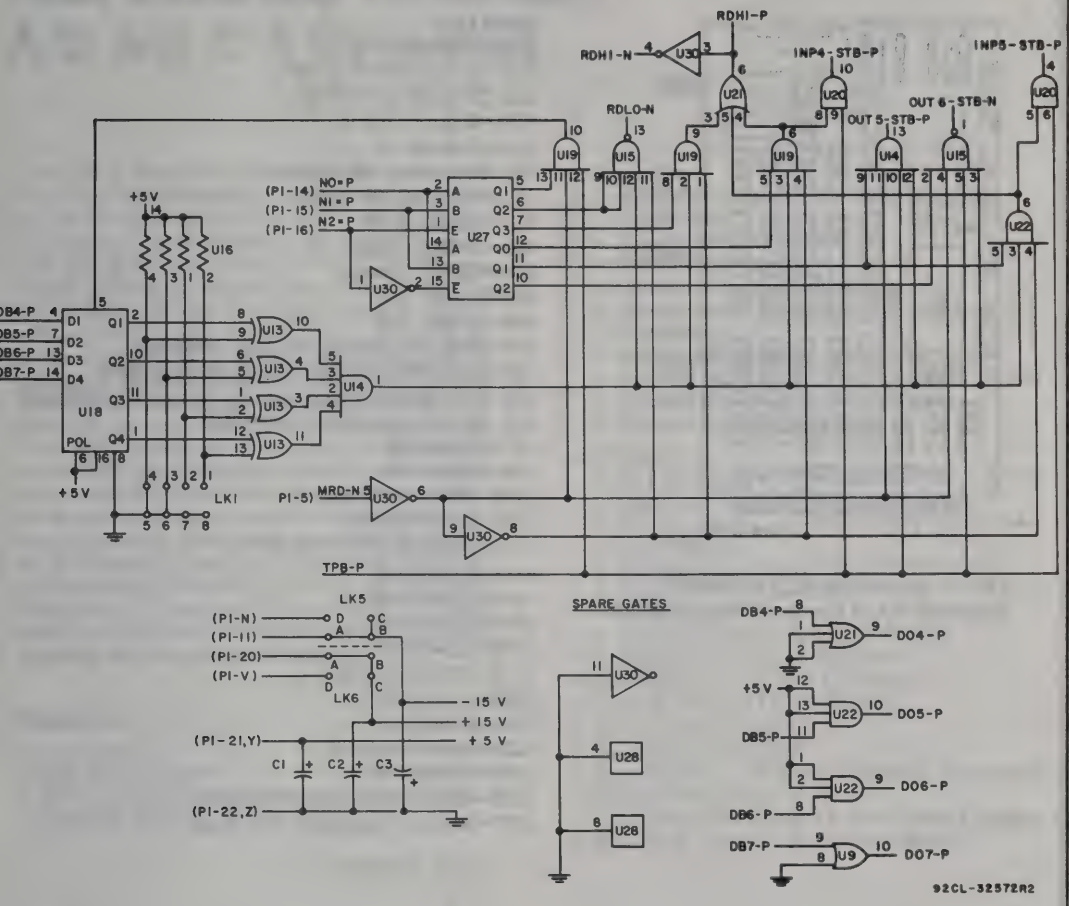


CDP18S643A



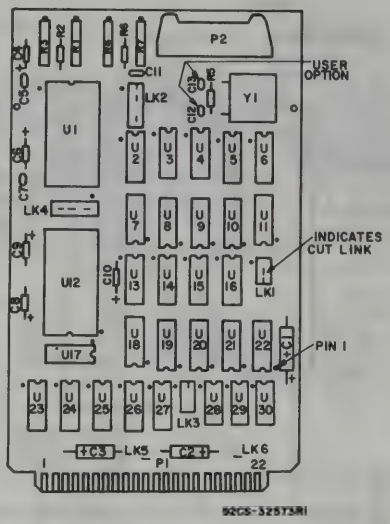
Logic diagram of RCA Microboard A/D Converter CDP18S643A

CDP18S643A



Logic diagram of RCA Microboard A/D Converter CDP18S643A (cont'd)

CDP18S643A



Layout diagram for RCA COSMAC Microboard A/D Converter CDP18S643A

Parts List

C1-C3=15 μF, 50 V
C4, C6, C8-C10=1 μF, 35 V
C5, C7=0.001 μF, 100 V
C11=0.01 μF, 100 V
C12, C13=22 pF
P2=Connector, 20 position
R1, R7=50 kΩ, variable
R2=1.8 MΩ, ¼ W
R3=10 kΩ, variable
R4=100 kΩ, variable
R5=22 MΩ, ¼ W
R6=10 MΩ, ¼ W
U1=3606 (Programmable-Gain Amplifier)
U2=SHC80KP (Sample-and-Hold Amplifier)
U3, U4=IH6108CPE (8-Channel Analog Multiplexer)
U5, U6, U8, U28, U29=CD4013BE
U7=CD4516BE
U9=CD4071BE
U10, U30=CD4069BE
U11=CD40103BE
U12=2483508 (A/D Converter)
U13=CD4070BE
U14=CD4082BE
U15=CD4012BE
U18=CD4042BE
U19, U22=CD4073BE
U20=CD4081BE
U21=CD4075BE
U23-U26=CD4502BE
U27=CD4555BE
U16=resistor module, 22 kΩ, 14 pin
U17=resistor module, 22 kΩ, 16 pin

CDP18S644, CDP18S654

RCA COSMAC Microboard A/D and D/A Converters

The RCA COSMAC Microboard A/D and D/A Converters CDP18S644 and CDP18S654 both contain an analog-to-digital conversion system and two independent digital-to-analog conversion systems, each having 8-bits of resolution. The CDP18S644 is capable of both unipolar and bipolar operation. The CDP18S654 is capable of unipolar operation only.

These Microboards operate from a single 5-volt power supply, require minimal currents because of their primarily CMOS design, and feature two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations.

The CDP18S644 and CDP18S654 are designed for use in a Microboard computer system, are expandable by use of the COSMAC Microboard Universal Backplane, and are plug-in compatible with the RCA Prototyping Systems CDP18S691 and CDP18S692, the RCA COSMAC Development Systems CDP18S005 (CDSII) and CDP18S007 (CDSIII), and the RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate hardware and software development.

Features

- **Low power**
- **High noise immunity**
- **Wide operating temperature range −40° C to +85° C**

A/D Section:
- **Multiplexed inputs — 16 single-ended or 8 differential**
- **Sample-and-hold circuitry**
- **8 bits of resolution**
- **Scanned or fixed channel mode**
- **Straight binary or offset binary output codes (CDP18S644)**
- **Straight binary output codes (CDP18S654)**
- **Unipolar or bipolar input voltage (CDP18S644)**
- **Unipolar input voltage (CDP18S654)**
- **Ribbon-cable input connector**

D/A Section:
- **Two independent D/A channels with 8 bits of resolution**
- **Straight binary or offset binary input codes (CDP18S644)**
- **Straight binary input codes (CDP18S654)**
- **Unipolar or bipolar output voltage (CDP18S644)**
- **Unipolar output voltage (CDP18654)**
- **Ribbon-cable output connector**

- **Operable from a single 5-volt supply**
- **Small board size (4.5 x 7.5 inches)**
- **Simple system interface**
- **Assignable I/O address**
- **Expandable by use of the COSMAC Microboard Universal Backplane**
- **Compatible with COSMAC Development Systems**
- **Member of extensive Microboard family**

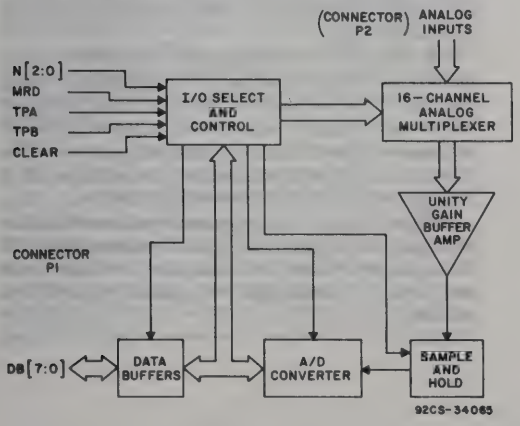


Fig. 1 — Block Digram of A/D Section of RCA COSMAC Microboard A/D and D/A Converters CDP18S644 and CDP18S654

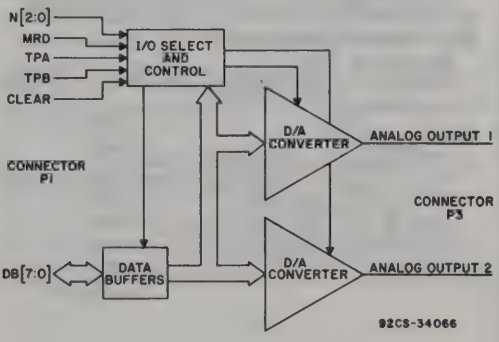


Fig. 2 — Block Diagram of D/A Section of RCA Microboard A/D and D/A Converters CDP18S644 and CDP18S654.

CDP18S644, CDP18S654

Specifications

A/D Input
No. of Channels: 16 single-ended/8 differential
Input Common Mode Range:
0 V to to +2.7 V (CDP18S654)
−2.7 V to +2.7 V (CDP18S644)
A/D Input Voltage Range:
Unipolar operation 0 V to +2.5 V
Bipolar operation −2.5 V to +2.5 V (CDP18S644)

A/D Output
Unipolar operation: Straight binary
Bipolar operation: Offset binary (CDP18S644)

A/D Transfer Characteristics
Resolution: 8 bits
Conversion Time: 215 μs max
Total Common-Mode Error Over A/D Input Range (Differential Input): <1/4 LSB

A/D Accuracy
Differential Linearity: ±3/4 LSB
Power Supply Sensitivity: ±0.16% of full-scale range/% supply volts
Gain Error: Adjustable to zero
Offset Error: Adjustable to zero

D/A Output
Channels: 2 independent
Output Range:
Unipolar operation: 0 V to +2.5 V, 0 V to +2.56 V
Bipolar operation: −2.5 V to +2.5 V, −2.56 V to +2.56 V (CDP18S644)
Output Drive Capability:
Source: 50mA typical
Sink: 10-kΩ pull-down resistor to V neg.
(V neg. = 0 V on CDP18S654, V neg. ≈ −3.0 V on CDP18S644)
Output impedance: 2 Ω

D/A Input
Unipolar Operation: Straight binary
Bipolar Operation: Offset binary (CDP18S644)

D/A Transfer Characteristics
Resolution: 8 bits
Settling Time: (For any step size to within 1/2 LSB) : 15 μs

D/A Accuracy
Differential Linearity: ±1/2 LSB
Power Supply Sensitivity: ±0.08% of full-scale range/% supply volts
Gain Error: Adjustable to zero
Offset Error: Adjustable to zero

Operating Temperature Range
−40°C to +85°C

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board Pitch: 0.5 inch (12.7 mm) minimum

Power Requirements
CDP18S644: + 5 V supply @ 50 mA typical
CDP18S654: + 5 V supply @ 15 mA typical

Connectors
System Interface: Edge fingers, 44 pins on 0.156-inch centers
Analog Input Interface: Right-angle 20-pin header. Berg part no. 65496-007 or equivalent. Mates with Berg part no. 65847-021/022 or equivalent
Analog Output Interface: Right-angle 10-pin header. Berg part no. 65496-001 or equivalent. Mates with Berg part no. 65847-003/004 or equivalent

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboards, CDP18S644 and CDP18S654. For additional information on these signals, refer to the published data for the CDP1802A COSMAC Microprocessor (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.** These signals are summarized in Table 1 which gives a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on RCA COSMAC Microboards, CDP18S644 and CDP18S654.

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus, these lines transfer the data from the CPU to the converter and the control logic.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate that an I/O instruction is being executed. They are derived from the three low-order bits of the N-register and are valid only during an I/O instruction. These lines are decoded to control the transfer of data between the data bus and the RCA Microboards CDP18S644 and CDP18S654.

$\overline{\text{MRD}}$ — Derived from the most significant bit of the N register, this signal defines the direction of the I/O data transfer. A low level indicates a transfer from memory to I/O; and a high level, a transfer from I/O to memory.

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Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P *	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P *	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Request
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N *	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N *	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N *	In	External Flag
X	EF4-N *	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

*Signals used on RCA COSMAC Microboards CDP18S644, CDP18S654.

TPA, TPB - Timing Pulses generated by the CPU which occur once in each machine cycle. Used primarily for latching the data and N lines.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. One of these lines and/or the **$\overline{INT}$** line is used to signal the CPU that the conversion is complete and that data is available. The particular line(s) chosen is link-selectable, see Table II. The **$\overline{EF1}$** connection is preprinted.

$\overline{INT}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited or enabled under software control. If Interrupt Enable (IE) is set, recognition of **$\overline{INT}$** results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as the program counter.

$\overline{CLEAR}$ — A low level on this line, indicating a system reset, clears the conversion-complete flip-flop, sets the input mode to fixed channel, selects channel 0, internally resets the A/D Converter, and places the sample-and-hold circuitry in the sample mode.

The **$\overline{CLEAR}$** signal also clears the latches in the D/A Converters (sets them to an 00H state).

Table II - CPU Lines Available for Conversion-Complete Signal

CPU Line	Link	
	LK4	LK6
EF1-N	4:5*	—
EF2-N	3:6	—
EF3-N	2:7	—
EF4-N	1:8	—
INT-N	—	A:B

*Preprinted

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Two-Level I/O Addressing Conventions

During an I/O instruction, the CPU presents the three low-order bits of its N register on the N2, N1, and N0 lines. N3 generates the $\overline{MRD}$ signal to indicate the direction of the data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In the Microboard system, the following conventions are established:

The OUT 1 (61) instruction is used to transmit a group select number. The output byte is latched and decoded by any Microboard in the system having an I/O function.

The group number is divided into two parts. The lower four bits are linearly encoded and the upper four bits are binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the 6 commands left after reserving the 61 and 69 instructions. The total number of useful I/O addresses is 114.

The INP 1 (69) instruction is reserved for reading the latched output of the 61 instruction. The CDP18S644 and the CDP18S654 do not provide this feature.

The CDP18S644 and the CDP18S654 are preassigned by links to group select 30. To enable these Microboards, a 61 instruction followed by the hex data 30 is required. Once the Microboard has been selected, additional I/O instructions establish modes of operation, begin conversion, and read the data. (Note: To change group select code see Table III).

Control Circuit Operation

The **I/O Select and Control** circuitry consists of CMOS gates, latches, buffers and decoders. This circuitry is used to initialize and select the Microboard. Once this Microboard is selected, the I/O Select and Control circuitry decodes and implements commands, and controls data flow between various parts of the Microboard and the backplane.

The **data buffers** consist of a pair of CMOS CDP1857CE (U34, U35) 4-bit bus separators with enable/disable and data in/data out control pins. These types isolate the board from the backplane and thus minimize loading effects on the backplane.

On-board CMOS **voltage converters,** two for the CDP18S644 (U12, U17) and one for the CDP18S654 (U17) are used to supply the necessary voltages for bipolar (CDP18S644) and unipolar (CDP18S644, CDP18S654) operation.

Table III
I/O Group Select Code Connections

I/O Group Select Code	Link LK5 Pin Connections
10	1:8
20	2:7
30*	1:8, 2:7
40	3:6
50	1:8, 3:6
60	2:7, 3:6
70	1:8, 2:7, 3:6
80	4:5
90	1:8, 4:5
A0	2:7, 4:5
B0	1:8, 2:7, 4:5
C0	3:6, 4:5
D0	1:8, 3:6, 4:5
E0	2:7, 3:6, 4:5
F0	1:8, 2:7, 3:6, 4:5

*LK5 is pre-linked for group select code 30.

Analog Input

The **analog multiplexer** stage consists of two CMOS CD4051BE (U1, U2) 1 – of – 8 multiplexers that can be configured by the use of links to provide 16 single-ended channels or 8 differential input channels. These switches can be sequentially scanned or randomly selected under software control. See Table IV for linking of Input Mode.

Table IV — Input Mode Selection

Input Mode	Link LK1
Single-Ended	2:13, 4:11, 5:10, 7:8
Differential	*1:14, 3:12, 6:9

*Preprinted link connections

The **unity-gain buffer-amplifier** stage consists of BiMOS CA3260AE (U6, U7) op-amps connected in a unity-gain instrumentation-amplifier configuration. This stage is used to provide differential input capability and high input impedance.

The **sample-and-hold amplifier** CA3160AE (U5) acquires and holds analog signals. When a convert command is given, the sample-and-hold amplifier is switched to the hold mode and when the conversion is complete, it is switched back to the sample mode. A built-in delay allows for amplifier settling times.

The **analog-to-digital converter** is an 8-bit successive-approximation CMOS component (U10). A variable, on-board voltage reference is used to adjust the gain of the converter; a separate potentiometer adjusts the offset.

A/D Commands

The four commands discussed below control the A/D section of these Microboards.

OUT 5 (65) instruction — This instruction resets the service request flip-flop and begins a conversion cycle. The byte output by this instruction specifies the input channel. When the board is configured for the single-ended input mode the four least significant bits provide a binary selection of the input channel (1 of 16 individual channels). When the board is configured for the differential input mode, the three least significant bits provide a binary selection of the input channel (1 of 8 channel pairs). The remaining bits are ignored by the channel select logic (See Table V). Upon receiving a system reset, channel 0 is selected if in the single-ended mode; channel pair 0^+, 0^- is selected if in the differential mode.

Table V — Channel Selection Code (Byte output with 65 instruction)

Single-Ended Input Mode		Differential Input Mode	
Byte Output	Channel Selected	Byte Output	Channel Pair Selected
XXXX 0000	0	XXXXX 000	0^+, 0^-
XXXX 0001	1	XXXXX 001	1^+, 1^-
XXXX 0010	2	XXXXX 010	2^+, 2^-
XXXX 0011	3	XXXXX 011	3^+, 3^-
XXXX 0100	4	XXXXX 100	4^+, 4^-
XXXX 0101	5	XXXXX 101	5^+, 5^-
XXXX 0110	6	XXXXX 110	6^+, 6^-
XXXX 0111	7	XXXXX 111	7^+, 7^-
XXXX 1000	8		
XXXX 1001	9		
XXXX 1010	10		
XXXX 1011	11		
XXXX 1100	12		
XXXX 1101	13		
XXXX 1110	14		
XXXX 1111	15		

X's are "don't cares", totally ignored by the channel select logic.

OUT 6 (66) instruction — The byte output by this instruction specifies the channel selection mode. The seven most significant bits in the output byte are ignored. When the least significant bit is 0, the fixed channel mode is selected. When the least significant bit is 1, the sequential scan mode is selected. Upon receiving a system reset, the channel selection is set to the fixed channel mode. (See Table VI).

Table VI —Channel Selection Mode (Byte output with 66 instruction)

Byte Output	Mode Selected
XXXXXXX 0	Fixed Channel
XXXXXXX 1	Sequential Scan

X's are "don't cares", totally ignored by the channel selection mode logic

INP 3 (6B) instruction — This instruction inputs the 8 data bits from the A/D converter, and also resets the service request flip-flop.

INP 4 (6C) instruction — This instruction inputs the 8 data bits from the A/D converter, resets the service request flip-flop and initiates another conversion. In addition, INP 4 (6C) will increment the channel prior to starting another conversion if the sequential scan mode has been enabled and initiates another conversion.

Note: The channels wrap. Incrementing channel pair 7^+, 7^- will select channel pair 0^+, 0^-; incrementing channel 15 will select channel 0 if in the single-ended mode.

Digital Output/Analog Input

The digital output codes that the CDP18S644 can produce are straight binary (used for unipolar operation) and offset binary (used for bipolar operation). The CDP18S654 is limited to unipolar operation and thus produces only straight binary. The digital output as a function of the input voltage for both codes is given in Table VII.

The digital output code and the analog input voltage range are link-selectable. These links are summarized

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Table VII — Digital Output as a Function of Input Voltage for CDP18S644 and CDP18S654

Unipolar Operation, CDP18S644 and CDP18S654			Bipolar Operation, CDP18S644		
Analog Input +2.5V Full Scale	Fraction of Full-Scale Value	Digital Output (Straight Binary)	Analog Input +2.5V Full Scale	Fraction of Full-Scale Value	Digital Output (Offset Binary)
2.490234375 V	FS-1LSB	1111 1111	2.48046875 V	FS-1LSB	1111 1111
1.875 V	+3/4 FS	1100 0000	1.875 V	+3/4 FS	1110 0000
1.25 V	+1/2 FS	1000 0000	1.25 V	+1/2 FS	1100 0000
0.625 V	+1/4 FS	0100 0000	0.625 V	+1/4 FS	1010 0000
0.3125 V	+1/8 FS	0010 0000	0.3125 V	+1/8 FS	1001 0000
0.009765625 V	+1 LSB	0000 0001	0.01953125 V	+1 LSB	1000 0001
0 V	0	0000 0000	0 V	0	1000 0000
			-0.01953125 V	-1 LSB	0111 1111
			-0.3125 V	-1/8 FS	0111 0000
			-0.625 V	-1/4 FS	0110 0000
			-1.25 V	-1/2 FS	0100 0000
			-1.875 V	-3/4 FS	0010 0000
			-2.48046875 V	-FS-1LSB	0000 0001
			-2.5 V	-FS	0000 0000

Note: Analog input voltages given are theoretical center step values.

in Table VIII. Both Microboards are prelinked for straight binary output code and an input voltage range of 0 V to 2.5 V. The CDP18S644 is prelinked for offset binary output code and an input voltage range of -2.5 V to 2.5 V.

Table VIII
Digital Output/Analog Input Links

Output Mode	Input Voltage Range	Link LK2
Straight Binary	0 V to 2.5 V	2:7 Open
Offset Binary (CDP18S644 only)	-2.5 V to 2.5 V (CDP18S644 only)	2:7 Closed

The analog inputs, available at the right-angle connector P2, may be configured as 16 single-ended inputs or as 8 differential inputs. The input mode, which is determined by link LK1 (see Table IV), is prelinked for differential inputs. The pin assignments for the two modes are listed in Table IX.

A/D Adjustment Procedures

Potentiometers are provided on the CDP18S644 and the CDP18S654 Microboards for both gain and offset A/D adjustments. Adjusting the offset potentiometer, R1, moves the transfer function either up or down. Adjusting the gain potentiometer R2, varies the slope of the transfer function (see Fig. 4). The objective of this adjustment procedure is to approach the ideal transfer function for an 8-bit A/D converter.

Table IX
Pin Assignments for Connector P2

Pin	Channel	
	Single-Ended	Differential
1	0	0+
2	8	0-
3	1	1+
4	9	1-
5	2	2+
6	10	2-
7	3	3+
8	11	3-
9	4	4+
10	12	4-
11	5	5+
12	13	5-
13	6	6+
14	14	6-
15	7	7+
16	15	7-
17	GND	GND
18	GND	GND
19	GND	GND
20	SPARE	SPARE

For a 3-bit converter operating in the unipolar mode, see Figs. 3 and 4, the ideal transfer function is achieved when the width of each step is equal to 1 LSB or 1/8 of 2.5 V (2.5 V-0 V) and the slope of the curve passes through the (0 V, 000) point; and for operation in the bipolar mode, when the width of each step is equal to 1 LSB or 1/8 of 5 V (2.5 V— –2.5 V) and the slope of the curve passes through the (0 V, 100) point.

An 8-bit converter operates in a similar fashion. For an 8-bit converter operating in a unipolar mode, the ideal transfer function is achieved when the width of each step is equal to 1 LSB or 1/256 of 2.5 V (2.5 V — 0 V) and the slope of the curve passes through the (0 V, 0000 0000) point; and for bipolar mode operation, when the width of each step is equal to 1/256 of 5 V (2.5 V — –2.5 V) and the slope of the curve passes through the (0 V 1000 0000) point.

A recommended way to accurately adjust the A/D converter is by loading and running the program in Fig. 5. This program will select channel 0 (channel pair 0^+, 0^- if in differential input mode), and do repeated conversions, displaying each of the eight bits on the CRT terminal. The latest value will overlay the previous value. The full procedure is as follows:

1. Set up the desired board configuration (unipolar or bipolar operation, single-ended or differential input).
2. Install Microboard in system, load and run program. Before continuing, allow a few minutes for settling.
3. On channel 0 (channel pair 0^+, 0^- if in differential input mode) apply a signal equal to the lowest acceptable analog input value plus 1/2 LSB (≈ 4.9 V for unipolar operation, ≈ 2.49 V for bipolar operation).
4. Adjust the offset potentimoter R1, so that the seven most significant bits displayed on the screen are 0's and the least significant bit is toggling between 0 and 1.
5. On channel 0 (channel pair 0^+, 0^- if in differential input mode) apply a signal equal to the full-scale (FS) value minus 1-1/2 LSB's (≈ 2.4853 V for unipolar opeation, ≈ 2.4706 V for bipolar operation).
6. Adjust the gain potentiometer R2 so that the seven most significant bits displayed on the screen are 1's and the least significant bit is toggling between 0 and 1.

Note: For Microboards configured for bipolar operation, it may be necessary to go through the adjustment procedures several times to accurately adjust the Microboard.

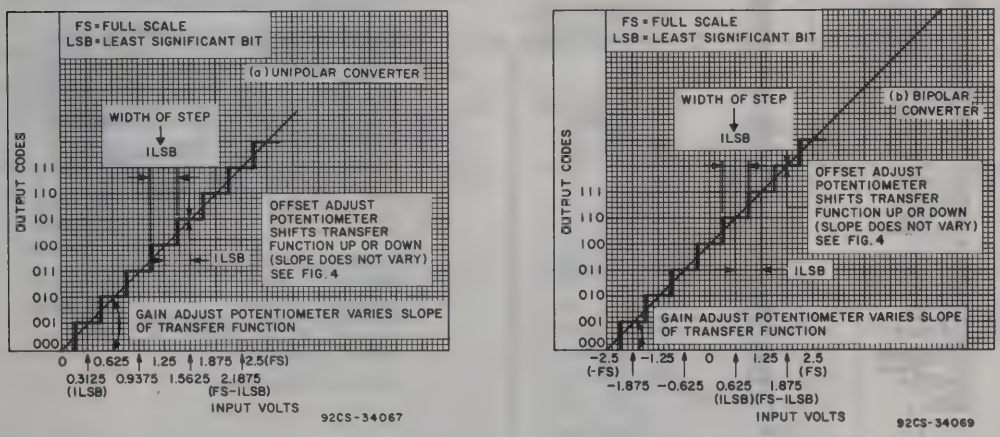

Fig. 3 — Ideal Transfer Function for a 3-Bit A/D Converter.

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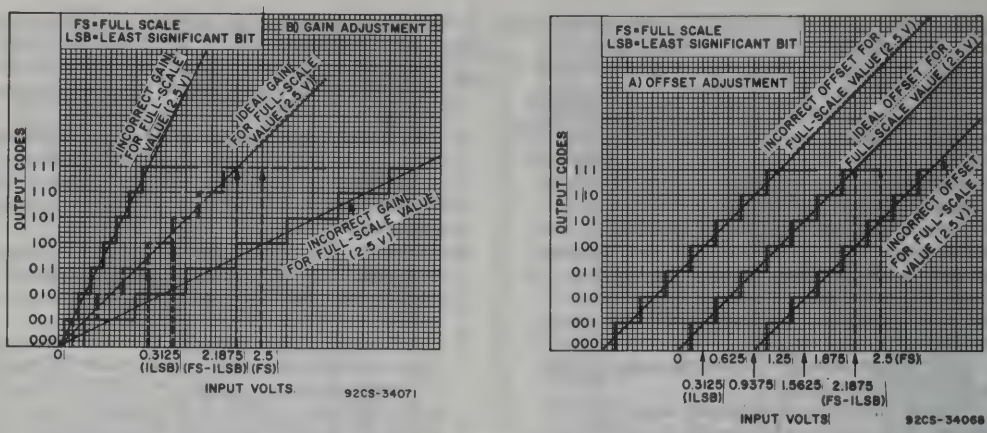

Fig. 4 — Effect of Gain and Offset Adjustments on Transfer Function of 3-Bit A/D Converter

```
IM
0000  ;                0001  . . A/D ADJUSTMENT PROGRAM WRITTEN IN ASM8 ASSEMBLY LANGUAGE
0000  ;                0002  . . THIS PROGRAM ASSUMES THE EXISTENCE OF A COSMAC UTILITY
0000  ;                0003  . . (EX. UT20,UT21,UT60,UT61,UT62) AT LOCATION 8000H
0000  ;                0004  STORE   EQU   07H
0000  ;                0005  PROG    EQU   03H
0000  ;                0006  INIT2   EQU   83F6H
0000  ;                0007  ADVAL   EQU   06H
0000  ;                0008  TYPE    EQU   81A4H
0000  ;                0009  CHAR    EQU   0FH
0000  ;                0010
0000  ;                0011          ORG 4000H          . . LOCATE PROGRAM AT 4000 H (ANY LOCATION WHERE
4000  ;                0012                             . . RAM IS PRESENT MAY BE SUBSTITUTED)
4000  F840B7;          0013          A.1(DUMMY)—>STORE.1  . . SET UP DUMMY STORAGE POINTER
4003  F836A7;          0014          A.0(DUMMY)—>STORE.0
4006  F840B3;          0015          A.1(START)—>PROG.1   . . SET PROGRAM COUNTER (R 3) TO POINT TO
4009  F80FA3;          0016          A.0(START)—>PROG.0   . . BEGINNING OF PROGRAM
400C  C083F6;          0017          LBR INIT2            . . INITIALIZE REGISTERS F OR STANDARD CALL AND
400F  ;                0018                               . . RETURN, ALSO SET UP STACK POINTER
400F  ;                0019  START
400F  E3;              0020          SEX PROG             . . SET X TO PROGRAM COUNTER (R3)
4010  6130;            0021          OUT 1;DC 30H         . . SELECT BOARD (ASSUMES BOARD SELECT IS 30H)
4012  6500;            0022          OUT 5;DC 00H         . . SELECT CHANNEL 0, RESETS THE SERVICE REQUEST
4014  ;                0023                               . . F/F, AND BEGIN A CONVERSION
4014  E7;              0024          SEX STORE            . . SET X TO DUMMY STORAGE POINTER
4015  3C15;            0025          BN1 $                . . WAIT UNTIL CONVERSION IS COMPLETE (ASSUMES
4017  ;                0026                               . . CONVERSION COMPLETE SIGNAL IS LINKED TO EF1)
4017  6B;              0027          INP 3                . . READ DATA AND RESET SERVICE REQUEST F/F
4018  A9;              0028          —>ADVAL.0            . . STORE VALUE IN A/D STORAGE REGISTER (R9)
4019  E3;              0029          SEX PROG             . . SET X TO PROGRAM COUNTER (R3)
401A  6101;            0030          OUT 1;DC 01H         . . SELECT RCA GROUP
401C  F808A8;          0031          08H—>R8.0            . . SET BIT COUNT TO 8
401F  ;                0032  CONTINUE
401F  89FEA9;          0033          ADVAL.0*2—>ADVAL.0   . . SHIFT BIT TO BE OUTPUT INTO DF
4022  F8007C30BF;      0034          00H+"30H—>CHAR.1     . . IF BIT IS A ONE OUTPUT A ONE
4027  ;                0035                               . . ELSE OUTPUT A ZERO
4027  D481A4;          0036          CALL TYPE
402A  28;              0037          DEC R8               . . DECREMENT BIT COUNT
402B  88;              0038          R8.0                 . . LOAD BIT COUNT INTO ACCUMULATOR
402C  3A1F;            0039          BNZ CONTINUE         . . IF ALL 8 BITS HAVE NOT BEEN OUTPUT
402E  ;                0040                               . . CONTINUE WITH OUTPUT
402E  F80DBF;          0041          0DH—>CHAR.1          . . OUTPUT A CARRIAGE RETURN
4031  D481A4;          0042          CALL TYPE
4034  300F;            0043          BR START             . . GO BACK AND DO IT AGAIN
4036  ;                0044  DUMMY
0000
```

Fig. 5 — A/D Converter Adjustment Program

Analog Output (See Figure 2)

The **digital-to-analog converter** used on the CDP18S644 and CDP18S654 essentially contains an 8-bit CMOS latch, CMOS buffers, a precision R-2R ladder network, and output driver circuitry. When a D/A Converter is given a convert command, the digital value that is to be converted and output is present on the data lines. The 8-bit latch is used to latch this information. The latches drive CMOS buffers (used for level shifting) which in turn drive a precision R-2R ladder network. The output of the R-2R ladder goes to the output driver circuitry.

D/A Commands

The two D/A commands discussed below are used to control the D/A section of these Microboards.

OUT 3 (63) instruction — This instruction selects D/A channel 1, latches the digital value present on the data bus (the byte output by this instruction), and begins a conversion.

OUT 4 (64) instruction — This instruction selects D/A channel 2, latches the digital value present on the data bus (the byte output by this instruction), and begins a conversion.

Digital Input/Analog Output

The digital input codes that the CDP18S644 will accept are straight binary (used for unipolar operation) and offset binary (used for bipolar operation). The CDP18S654 is limited to unipolar operation and thus will accept only straight binary. The analog output as a function of the digital input for both codes is given in Table X.

The digital input code and the analog output voltage range are link-selectable. The link connections are summarized in Table XI. The CDP18S654 has both D/A channels prelinked for straight binary input code and an analog output voltage range of 0 V to 2.5 V. The CDP18S644 has both D/A channels prelinked for offset binary input code and an analog output voltage range of –2.5 to 2.5 V.

Table XI — Digital Input/Analog Output Links

D/A Chan.	Input Mode	Output Voltage	Link LK2
1	Straight Binary	0 V to 2.5 V	4:5 Open
	Offset Binary (CDP18S644 only)	–2.5 V to 2.5 V (CDP18S644 only)	4:5 Closed
2	Straight Binary	0 V to 2.5 V	3:6 Open
	Offset Binary (CDP18S644 only)	–2.5 V to 2.5 V (CDP18S644 only)	3:6 Closed

Table X — Analog Output as a Function of the Digital Input for CDP18S644 and CDP18S654

Unipolar Operation, CDP18S644, CDP18S654			Bipolar Operation, CDP18S644		
Digital Input (Straight Binary)	Fraction of Full-Scale Value	Analog Output +2.5 Volts Full Scale	Digital Input (Offset Binary)	Fraction of Full-Scale Value	Analog Output +2.5 Volts Full Scale
1111 1111	+FS–1LSB	2.490234375 V	1111 1111	+FS–1LSB	2.48046875 V
1100 0000	+3/4 FS	1.875 V	1110 0000	+3/4 FS	1.875 V
1000 0000	+1/2 FS	1.25 V	1100 0000	+1/2 FS	1.25 V
0100 0000	+1/4 FS	0.625 V	1010 0000	+1/4 FS	.625 V
0000 0001	+ 1LSB	0.009765625 V	1000 0001	+ ILSB	0.01953125 V
0000 0000	0	0 V	1000 0000	0	0 V
			0111 1111	–1LSB	–0.01953125 V
			0110 0000	–1/4 FS	–0.625 V
			0100 0000	–1/2 FS	–1.25 V
			0010 0000	–3/4 FS	–1.875 V
			0000 0000	–FS	–2.5 V

Note: The analog output values given are theoretical values.

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The analog outputs are available at the right-angle connector P3. The pin assignments are given in Table XII.

Table XII — Analog Outputs — Connector P3 Pin Assignments

Channel 1 Output	P2-2
Channel 2 Output	P2-9
Grounds	P2-1,3,7,8,10
Spares	P2-4,5,6

D/A Adjustment Procedures

Potentiometers are provided on the CDP18S644 and CDP18S654 Microboards for both gain and offset adjustments. For D/A channel 1, potentiometer R5 adjusts the offset and R3 adjusts the gain. For D/A channel 2, R6 adjusts the offset and R4 adjusts the gain.

Selected digital input codes and their corresponding analog output voltages are listed in Table X. To adjust the offset, select the board and execute the appropriate output command with the output byte 0000 0000, then adjust the offset potentiometer to achieve the desired analog output (≈ 0.00 V for unipolar operation, ≈ −2.50 V for bipolar operation). To adjust the gain, select the board and execute the appropriate output command with the output byte 1111 1111, then adjust the gain potentiometer to achieve the desired analog output (≈ 2.49 V for unipolar operation, ≈ 2.48 V for bipolar operation).

Note: D/A adjustments must be made after any A/D adjustment.

Installation in Development Systems

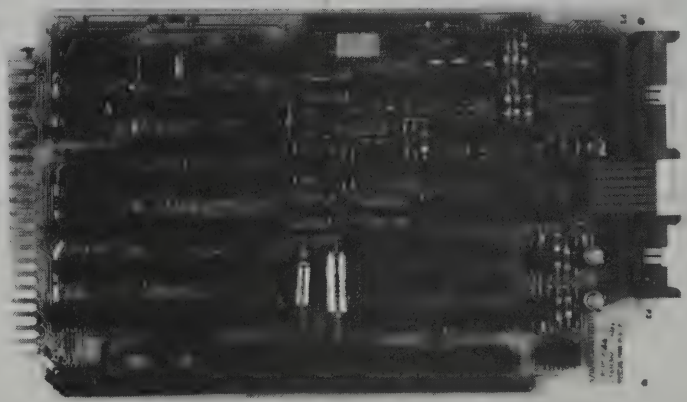
The CDP18S644 and CDP18S654 Microboards may be installed in any of the available I/O slots (14-18 or 21-23) in the COSMAC Development System (CDS II) CDP18S005, COSMAC DOS Development System (CDS III) CDP18S007, and in the Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may be easily allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When either the CDP18S644 or the CDP18S654 Microboard is installed in the COSMAC Development Systems, CDP18S005 or CDP18S007, the system signals indicated in Table XIII must be connected on the backplane to the I/O slot on the CDS selected for the Microboard.

Table XIII — CDS Backplane Connections (CDP18S005 and CDP18S007 only)

Signal	Jumper to Pin
N0-P	P1-14
N1-P	P1-15
N2-P	P1-16
Clear-N	P1-9

The CDP18S644 and the CDP 18S654 Microboards can be installed in the Microboard Computer Development Systems CDP18S693 and CDP18S694 and RCA Prototyping Systems CDP18S691 and CDP18S692 without any modifications.



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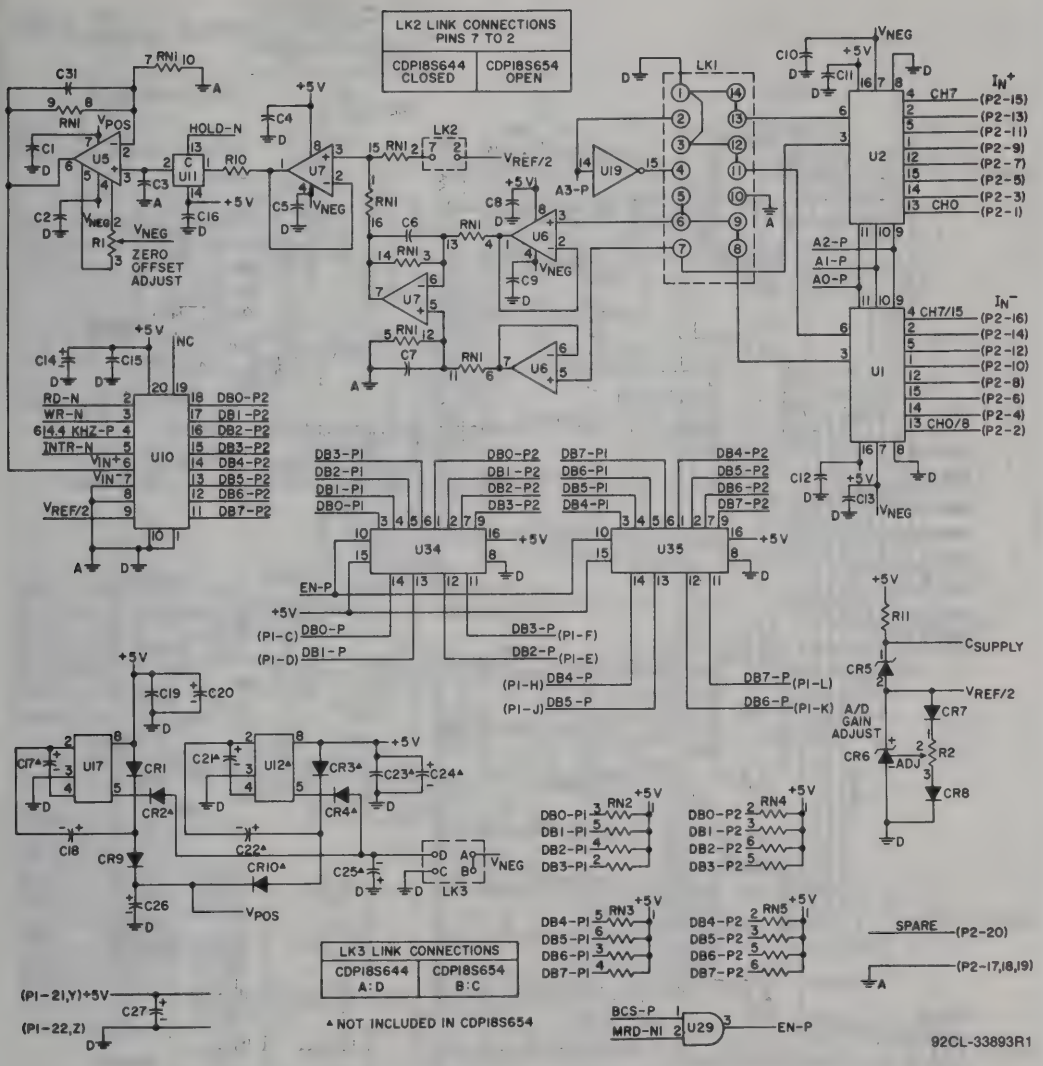

Fig. 6 — RCA COSMAC Microboard A/D and D/A Converters CDP18S644 and CDP18S654 — A/D Converter Portion.

CDP18S644, CDP18S654

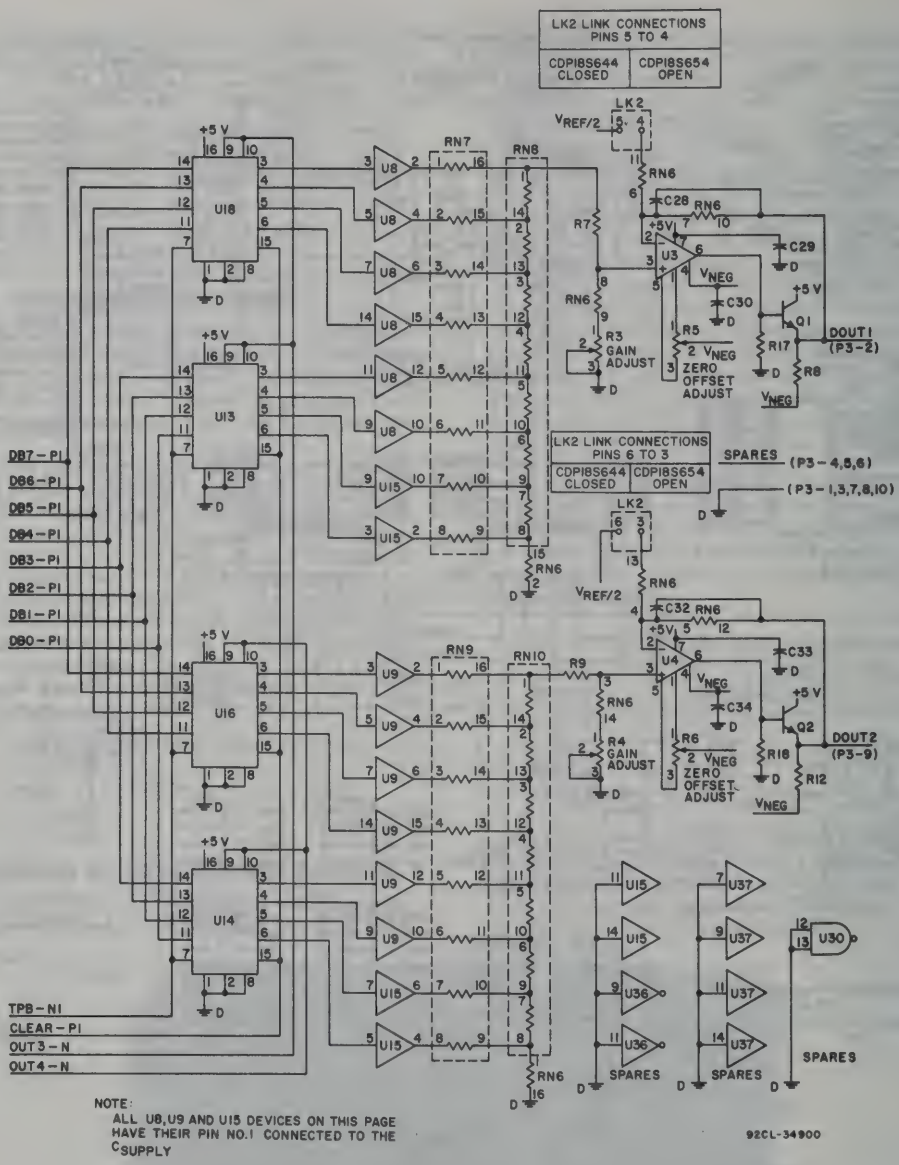

Fig. 7 - RCA COSMAC Microboard A/D and D/A Converters CDP18S644 and CDP18S654 — D/A Converter Portion.

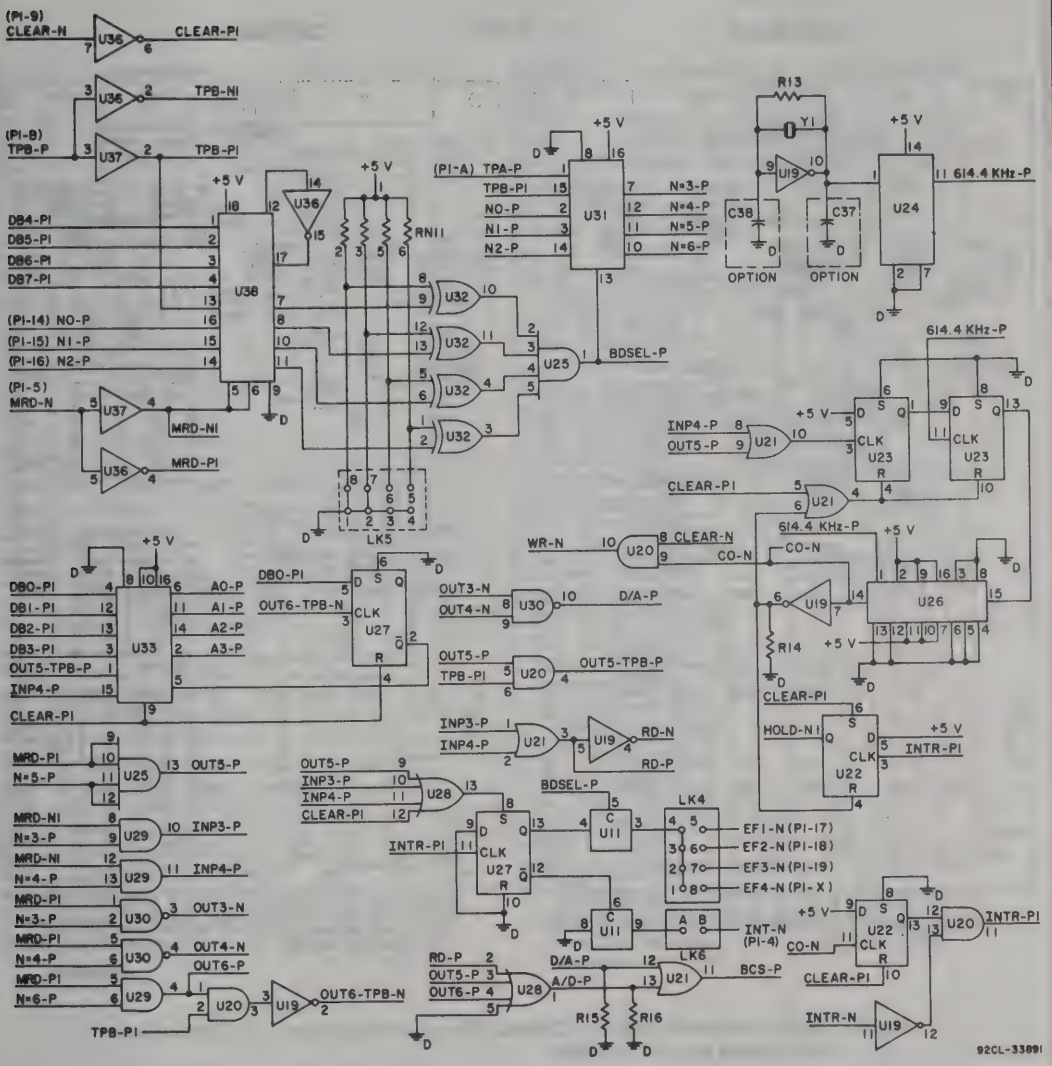

Fig. 8 - RCA COSMAC Microboard A/D and D/A Converters CDP18S644 and CDP18S654 — I/O Select and Control Portion.

CDP18S644, CDP18S654

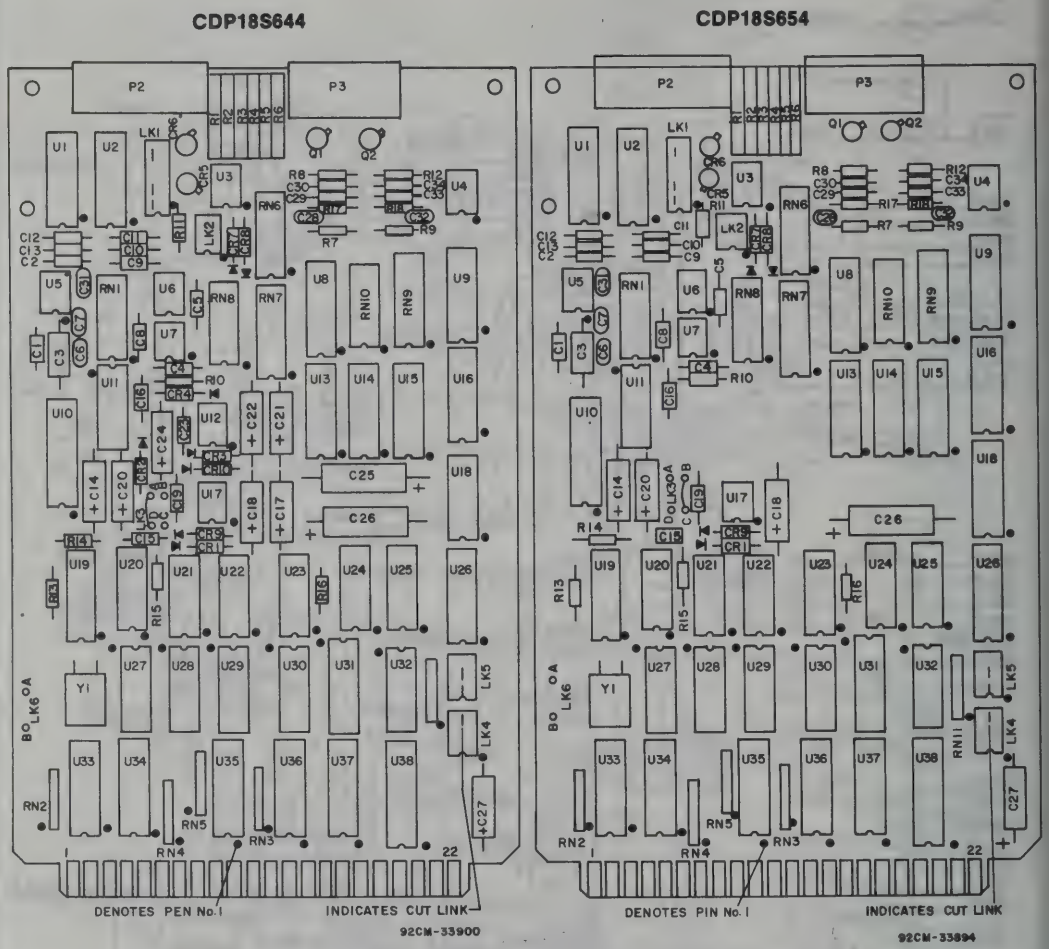

Fig. 9 - Layout Diagrams of RCA COSMAC Microboard A/D and D/A Converters CDP18S644 and CDP18S654.

CDP18S644, CDP18S654

PARTS LIST

C1, C2 = 1.0 μF, 15 V
C3 = 4700 pF. 33 V polystyrene
C4, C5 = 0.1 μF, 15 V
C6, C7 = 22 pF, 100 V
C8-C13 = 0.1 μF, 15 V
C14 = 15 μF. 20 V
C15, C16 = 0.1 μF, 15 V
C17*, C18 = 15 μF, 20 V
C19 = 0.1 μF, 15 V
C20, C21*, C22* = 15 μF, 20 V
C23* = 0.1 μF, 15 V
C24* 15 μF, 20 V
C25* = 100 μF, 10 V
C26, C27 = 15 μF, 20 V
C28 = 22 pF, 15 V
C29, C30 = 0.1 μF, 15 V
C31, C32 = 22 pF, 100 V
C33, C34 = 0.1 μF, 15 V
CR1, CR2*, CR3*, CR4* = 1N270
CR5 - LM113H
CR6 = LM236
CR7, CR8 = 1N914
CR9, CR10* = 1N270
P2 = Connector, 20 position
P3 = Connector, 10 position
Q1, Q2 = 2N2222
R1 = 100 kΩ, variable
R2 = 10 kΩ, variable
R3-R6 = 100 kΩ, variable
R7 = 22 kΩ, 1/4W, 5%
R8 = 10 kΩ, 1/4W, 5%
R9 = 22 kΩ, 1/4W, 5%
R10 = 300Ω, 1/4W, 5%
R11 = 200Ω, 1/4W, 5%
R12 = 10 kΩ, 1/4W, 5%
R13 = 22 MΩ, 1/4W, 5%
R14, R16 22 kΩ, 1/4W, 5%
R17, R18 = 2.7 kΩ, 1/4W, 5%
RN1 = IC Resistor Module, 100 kΩ, 1%, 16-pin
RN2-RN5 = Resistor Module SIP, 22 kΩ, 6-pin
RN6, RN7 = IC Resistor Module, 100 kΩ, 1%, 16-pin
RN8 = IC Resistor Module, 50 kΩ, 1%, 14-pin
RN9 = IC Resistor Module, 100 kΩ, 1%, 16-pin
RN10 = IC Resistor Module, 50 kΩ, 1%, 14-pin
RN11, Resistor Module, SIP, 22 kΩ, 6-pin
U1, U2 = CD4051BE
U3-U5 = CA3160AE
U6, U7 = CA3260AE
U8, U9 = CD4050BE
U10 = ADC0803LCD
U11 = CD4066BE
U12* = ICL7660CPA
U13, U14 = CD4076BE
U15 = CD4050BE
U16 = CD4076BE
U17 = ICL7660CPA
U18 = CD4076BE
U19 = CD4049UBE
U20 = CD4081BE
U21 = CD4071BE
U22, U23 = CD4013BE
U24 = CD4024BE
U25 = CD4082BE
U26 = CD40103BE
U27 = CD4013BE
U28 = CD4072BE
U29 = CD4081BE
U30 = CD4011BE
U31 = CDP1853CE
U32 = CD4070BE
U33 = CD4516BE
U34, U35 = CDP1857CE
U36 = CD4049UBE
U37 = CD4050BE
U38 = CDP1867CE
Y1 = Crystal, 2.4576 HMz

*Not included in CDP18S654

CDP18S646

RCA COSMAC MICROBOARD

Parallel I/O Interface Module

The RCA COSMAC Microboard Parallel I/O Interface Module provides two control and communications channels for I/O peripherals such as a printer or a floppy disk drive system. The CDP18S646 provides these functions in the RCA COSMAC Development System CDS IV (CDP18S008) and can also serve as a byte interface module in CDP18S005 (CDS II) and CDP18S007 (CDS III) Development Systems. It is compatible with all other Microboard modules through the Microboard Universal Backplane. The CDP18S646 communicates with the disk drive system through three CDP1852 byte I/O ports, buffers, and a 50-conductor flat cable. The CDP18S646 communicates with the printer through one CDP1852 I/O port, buffers, two handshaking lines, and a 34-pin conductor cable.

Specifications

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Operating Temperature Range

-40° C to +85° C

Power Requirements

+5 volts at 0.3 milliampere (Standby, nothing connected)
+5 volts at 3 milliamperes (Disk drive and printer connected and reset)
+5 volts at 25 milliamperes (Board selected with disk and printer and either disk or printer operating)

Connectors

System Interface (P1): Edge fingers, 44 pins on 0.156-inch centers
Printer Interface (P2): Edge fingers, 34 pins on 0.100-inch centers
Disk System Interface (J1): Right-angle header, 50 pin.

Features

- **Low-power static CMOS**
- **Operable from 5-volt supply**
- **High noise immunity**
- **Compatible with COSMAC Development Systems**
- **44-pin system interface**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Small board size - 4.5 x 7.5 inches**
- **Member of extensive Microboard family**
- **Assignable I/O address**
- **Two 8-bit input ports**
- **Three 8-bit output ports with data strobe signals**
- **Board-enabled and clear output signals**
- **Pertec-type disk-system interface**
- **Centronics-type parallel printer interface**
- **TTL-compatible inputs**
- **TTL-compatible output (25 mA at 0.4 V)**
- **Link-adjustable I/O capability**
- **Operating temperature range: -40° C to +85° C**

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the RCA COSMAC Microboard CDP18S646. For additional information on these signals, refer to the published data for the CDP1802A COSMAC Microprocessor (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.** These signals are summarized in Table I which lists the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard CDP18S646.

DB7 through DB0 - These eight bidirectional data bus lines are buffered by the CDP1857CE 4-Bit Bus/Buffer Separators (U6 and U7) and then communicate with the CDP1852CE 8-Bit Input/Output Ports (U16, U17, U19, U20, and U21). The direction of transfer through the buffers is determined by the MRD signal. The buffers are enabled by any I/O execution applicable to this Microboard.

N0, N1, N2 - These three primary I/O address lines communicate directly with the CDP1853CE I/O Decoder (U2) which generates the signals N=4, N=5, etc. These signals are combined with the Microboard Select Signal (SEL) to form the signals S4 and S5 etc., which enable the individual I/O ports.

$\overline{\text{MRD}}$- Memory Read - When true, $\overline{\text{MRD}}$ indicates data flow from I/O to memory; when false, from memory to I/O. The $\overline{\text{MRD}}$ signal is buffered by a CD4041UBE Quad True/Complement Buffer (U5) and then is used on the data buffers and the I/O ports to establish the direction of data flow.

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P*	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P*	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P*	In/Out	Data Bus	5	MRD-N*	Out	Memory Read
F	DB3-P*	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P*	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P*	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P*	In/Out	Data Bus	9	CLEAR-N*	In	Clear-Mode Request
L	DB7-P*	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N*	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N*	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N*	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

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*Signals used on RCA COSMAC Microboard CDP18S646.

TPA- Timing Pulse A - This signal is buffered by the CD4041UBE (U5), and then used on the CDP1853CE I/O Decoder (U2) to form the leading edge for signals N=4, N=5, etc.

TPB- Timing Pulse B - This signal is also buffered by the CD4041UBE (U5), and then used on the CDP1853CE I/O Decoder (U2) to form the trailing edge for signals N=4, N=5, etc., and also as the data strobe into the output ports.

$\overline{\text{INT}}$ - This interrupt signal may be connected through link LK1, pins 5 and 10 to provide a system interrupt whenever either input/output port CDP1853CE (U21 or U20) has received a clock signal by way of connector J1.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$ - These external flags are available to the interface through link LK1. They are driven by a CDP1856CE Bus Separator (U1) which is enabled by the Microboard Select Signal (SEL). $\overline{\text{EF1}}$ is the OR'ed combination of BUSY or ACK for printer interface control. $\overline{\text{EF2}}$ and $\overline{\text{EF3}}$ are generated by SR1 and SR2, respectively, and are used to identify the interrupt source when either input/output port CDP1852CE (U21 or U20) has caused an interrupt. $\overline{\text{EF4}}$ is driven by control signal $\overline{\text{CTRL=3}}$ available on connector P2 interface.

$\overline{\text{CLEAR}}$ - This input signal is buffered by the CD4041UBE Buffer (U5) and is used for resetting the CD4013BE "D" Type Flip-Flops (U25 and U14) to establish the proper initial signal conditions: ACK=0, SEL=0, and $\overline{\text{STROBE-C}}$=0.

Two-Level I/O Addressing Conventions

The CDP18S646 uses standard Microboard two-level I/O addressing conventions with the capability of 19 useful group select I/O addresses.

The group number is divided into two parts and is transmitted by the OUT 1 $(61)_{16}$ instruction. The lower four bits are linearly encoded and the upper four bits are binary encoded. For linear and binary encoding of the I/O address, provisions are made to select the Parallel I/O Microboard by the system software issuing an OUT 1 $(61)_{16}$ command whose data is the group number desired. Link LK4 is provided to select the appropriate bit for linear encoding of the lower four bits while link LK3 provides selection for binary encoding of the upper four bits. (Note: Link LK8 is used for selection of binary or linear encoding.) Thus, the number of addresses provided

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for group select by the OUT 1 instruction is 15 binary-encoded plus 4 individual. When the CDP18S646 is addressed, a board-select signal SEL-P is generated and stays selected until it is superseded by another OUT 1 command. This signal enables data transfers by means of CPU I/O instructions and is available as an output signal (SELECT). The N2, N1, and N0 lines from the CPU are decoded on board for control of the transfer of data between it and the data bus.

The 24 output bits are controlled by CPU output instructions 64, 65, and 66 corresponding to DATA OUT bits 0 through 7, 8 through 15, and 16 through 23, respectively. The 16 input lines are controlled by input instructions 6C, 6D, and 6E. Either instruction 6C or 6E (link programmable) can be used for DATA IN 0 through 7. Instruction 6D is used for DATA IN bits 8-15.

Input user control signals to the CPU are CNT=1, CNT=2, CNT=3, BUSY and ACKNLG. Signals CNT=1, CNT=2, CNT=3, and BUSY are read by the CPU through the Data Bus by means of the 6B instruction. Service Request Signals (SR1 and SR2) from the two input data ports (U20 and U21) can each be linked to generate either a CPU Interrupt or an External Flag signal. In addition, ACKNLG, BUSY, or CNT=3 can be linked to provide an External Flag signal to the CPU.

Three separate data output strobe signals are provided for the user. STROBE A, STROBE B, and STROBE C are data output strobe signals for bits 0 through 7, 8 through 15, and 16 through 23, respectively. A control signal (SEL) is generated when the CPU addresses the CDP18S646 Microboard and is available for use as an output to connector J1. A system-generated CLEAR signal is also available as an output to connector P2.

> **Note:** The STROBE C output signal meets the timing requirements of Centronics-type Parallel Printer Interface as shown in Fig. 3. The CDP18S646 Parallel I/O Interface Module is configured for direct use as an I/O interface for Pertec Floppy-Disk System (FD 3012) by means of connector J1, and/or a line printer having a Centronics-type Parallel Printer Interface by means of connector P2.

Two-Level I/O Addressing Conventions

Microboard Select Options

Link LK1, pin positions 6:9, is prelinked at the factory to enable linear decoding of the data bits 0, 1, 2, and 3. Link LK4 selects any one of these four bits (factory set to 0). To enable binary decoding of the Microboard Select Signal (SEL), remove jumper on pin positions 6:9 on link LK1 and install jumper on pin positions 7:8 on link LK1. Binary decoding of data bits 4, 5, 6, and 7 is accomplished by means of link LK3. The appropriate binary configuration of link LK3 will match the actual high bits of the data bus to generate the Microboard Select Signal (SEL).

Connectors J1 and P2 Signal Descriptions

Output Ports (DO-0N to DO-32N) - These active low output signals controlled by the CDP1852CE 8-Bit Input/Output Ports (U16, U17, and U19) are open-collector outputs capable of 25-milliampere drive. (If desired, optional field modification can increase this drive to 50 milliamperes by replacing resistor modules U22, U23, U24, and U26 with Beckman-type 470-ohm networks 898-3-R470) The output data bits are controlled as follows:

Data Byte	Pre-linked Instruction	Output Strobe Signal
0 to 7	65	STROBE A
8 to 15	64	STROBE B
16 to 23	66	STROBE C

Input Ports (DI-0N to DI-15N) - These buffered active low input signals controlled by the CDP1852CE I/O Ports (U20 and U21) are TTL-compatible inputs with pull-up resistors of 3.3 kΩ to 5 volts. The U20 and U21 are configured in a feed-through mode (CLK=1) when CLOCK 1-N and CLOCK 2-N are not used. This mode of operation is desired when the CDP18S646 is used in conjunction with the floppy-disk drive mechanism of the CDP18S008 COSMAC Development System (CDS IV). The input data bits are controlled as follows:

Input Byte	Instruction	Input Strobe Signal
0 to 7	6E (6C optional by means of link LK5)	CLOCK 1-N
8 to 15	6D	CLOCK 2-N

SELECT-N - This active low output signal can be used to determine if the Microboard has been selected by the appropriate output signal.

CLEAR-N - This active low output signal is controlled by the Universal Backplane and is used as a clear signal to external devices.

RESET-P - This active high output signal is used for resetting the CDP1852CE I/O Input/Output Ports (U20 and U21).

CNT=1-N, CNT=2-N, CNT=3-N - These active low input signals are prelinked to connector P2. (Note: As an option these signals can be linked to connector J1 by means of link LK7). These optional handshaking signals can be interrogated by input instruction 6F. They are available at the Data Bus as follows:

Signal	Data Bus
CNT=1-N	0
CNT=2-N	1
CNT=3-N	2

CNT=3-N can also be directly linked to EF4-N by means of link LK1, pin positions 4:7.

BUSY-P - This active high input signal is used as part of the Centronics-type Parallel Printer Interface. This signal can also be used as an optional handshaking signal interrogated by input instruction 6F and is available on Data Bus 3. BUSY-P is factory prelinked to EF1-N (Note: EF1-N is active with BUSY-P or ACKNLG-N).

ACKNLG-N - This active low signal is used in conjunction with the Centronics-type Parallel Printer Interface and is conditioned by input instruction 6E. That is, ACK-P, generated by CD4013BE Dual "D" type Flip-Flop (U14) and prelinked to EF1-N, is set to "1" by means of instruction 6E and reset to "0" by means of ACKNLG-N or the system CLEAR-N signal. ACKNLG-N can be used as a handshaking signal for general applications where the external device receiving output data 16 to 23 can send a return acknowledge signal back to the CPU. The ACK-P signal is available on factory prelinked EF1-N. (Note that BUSY-P is linked to EF1-N (See BUSY-P information on usage).

Control Signals

SEL-P - This Microboard select signal is generated by the Microboard two-level I/O select logic SEL-P prelinked for output instruction 61 with a data field of XXXX XXX1 (01_{16}). The data field can be changed by means of links LK3, LK4, and LK1. (See Two-Level I/O Addressing Conventions, Select Options).

SR1-P, SR2-P - These input-port service-request signals are activated when data is latched into the CDP1852CE 8-Bit Input/Output Port. Data (DATA IN-0 through DATA IN-7) are latched into U21 by the trailing edge of CLOCK 1-N on J1-4, and SR1 is generated. Data (DATA IN-8 through DATA IN-15) are latched into U20 by the trailing edge of CLOCK 2-N on J1-29, and SR2 is generated. Either SR1 or SR2 is cleared when the appropriate port is read or a system clear is generated. The OR'ed condition of SR1 or SR2 can be made available to generate an interrupt to the CPU by means of link LK1, pin positions 5:10. SR1-P is also directly available to EF2-N by means of link LK1, pin positions 2:13; and SR2 is available to EF3-N by means of link LK1, pin positions 3:12.

Link Configurations

LK1

Pin Position	Comments
1:14†	Provides ACK-P or BUSY-P to EF1-N
2:13	Provides SR1-P to EF2-N
3:12	Provides SR2-P to EF3-N
4:11	Provides CNT=3-P to EF4-N
5:10	Provides SR1-P or SR2-P to INTERRUPT
6:9†	Selects linear decode of Microboard Select Signal
7:8	Selects binary decode of Microboard Select Signal

†Factory installed

LK2

Linking pin positions A:B on link LK2 provide CLEAR-N signal to the Microboard for use in COSMAC Development Systems CDP18S005 (CDS II), CDP18-S007 (CDS III), and CDP18S008 (CDS IV).

LK3

Pin Position	Signal	Comments
1:8	DB-4	
2:7	DB-5	Binary Decode of Data Bus
3:6	DB-6	for Microboard Select Signal
4:5	DB-7	

LK4

Linear decode of DB0 through 3.

Pin Position	Signal
5:4	DB-0†
6:3	DB-1
7:2	DB-2
8:1	DB-3

†Factory installed

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LK5		
Pin Position	**Signal**	**Comments**
1:8	DO	To output only
2:7†	DO AND with SR	For use in disk interface
3:6†	Enable 6E	Input instruction for CDP1852CE (U21) - DI 0-7
4:5	Enable 6C	Input instruction for CDP1852CE (U21) - DI 0-7

†Factory installed

LK6		
Pin Position	**Signal**	**Comments**
1:4	$\overline{\text{CLEAR}}$	Microboard Backplane CLEAR-N signal to ports
2:3†	$\overline{\text{CLEAR}}$	External CLEAR-N signal for input ports

†Factory installed

LK7		
Pin Position	**Signal**	**Comments**
1:12†	CNT=3-N	To P2-24
2:11	CNT=3-N	To J1-8
3:10†	CNT=1-N	To P2-22
4:9	CNT=1-N	To J1-21
5:8†	CNT=2-N	To P2-20
6:7	CNT=2-N	To J1-22

†Factory installed

Installation in Development Systems

When a printer interface is required for use in RCA COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III), the CDP18S646 Parallel Interface I/O Module is recommended. To accommodate the CDP18S646, proceed as follows:

1. Remove pin 29 from the 50-pin male connector J1 of the CDP18S646 and install jumper on pin positions A:B on link LK2
2. Remove CDP18S813 Disk Interface Module from slot location 24 of the CDS chassis and insert the CDP18S646 in that slot
3. On the backplane of the CDP18S005, CDP18S007, or CDP18S008, add three jumpers as follows:

From Slot Location 13 Pin No	To Slot Location 24 Pin No	Backplane Signal Name
14	14	N0-P
15	15	N1-P
16	16	N2-P

4. Connect disk cable to connector J2
5. Plug the 34-pin terminal card-edge connector of the 12-inch extension cable CDP18S518 into the 34-pin edge terminal (P2) of the CDP18S646
6. Plug 50-pin female connector of the Floppy Disk System-CDS interface cable into the 50-pin male connector (J1) on the CDP18S646.

For information on the Printer interface software for the CDP18S005, refer to the section "Printer Program" on page 70 of the **RCA COSMAC Floppy Disk System II CDP18S005 Instruction Manual MPM-217.** For similar information on the CDP18S007, refer to the section "Peripheral Devices" on page 11 and the material on the commands COPY and DIR on pages 16, 17, and 18 of the **Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007 MPM-232.**

Disk/Printer Interfacing with The CDP18S646

The CDP18S646 communicates with a floppy disk drive system and with a printer as shown in Figs. 1 and 2.

The block diagram for the disk logic is given in Fig. 1. The first output port, used for commands to the drive units, is written by a 65 output instruction under Group 1 controls (SEL0-P). Seven command bits are sent to the drive unit through the grounded-emitter open-collector transistor driver. The least significant bit is gated by the service request (SR) generated by the output port to provide a clock strobe.

Data is sent to the drive unit through a second output port loaded by a 64 output instruction. All eight bits are transmitted through grounded-emitter open collector transistor drivers. Data or status information from the drive unit is received by an input port, which is read by a 6E input instruction.

The block diagram for the printer-interface logic is given in Fig. 2. When communications between the CPU and a printer or floppy-disk drive unit is required, the system software issues an OUT 1 (61) command whose data is 0000 0010 in order to select the CDP18S646. This

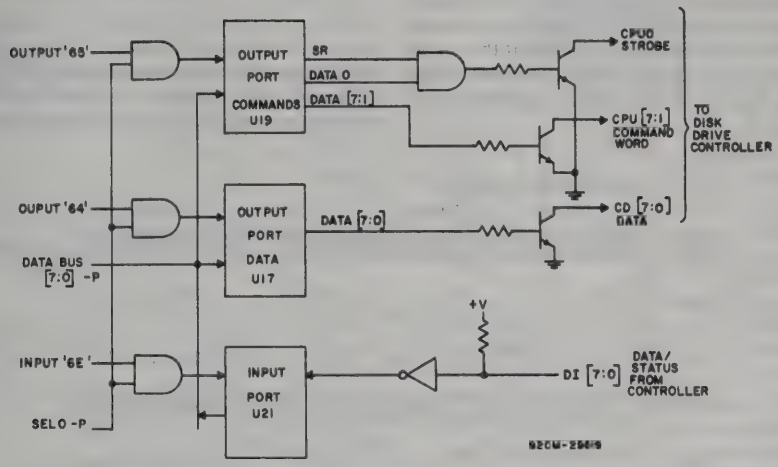


Fig. 1 - RCA COSMAC Microboard Parallel I/O Interface Module - Block Diagram of Disk Interface Logic.

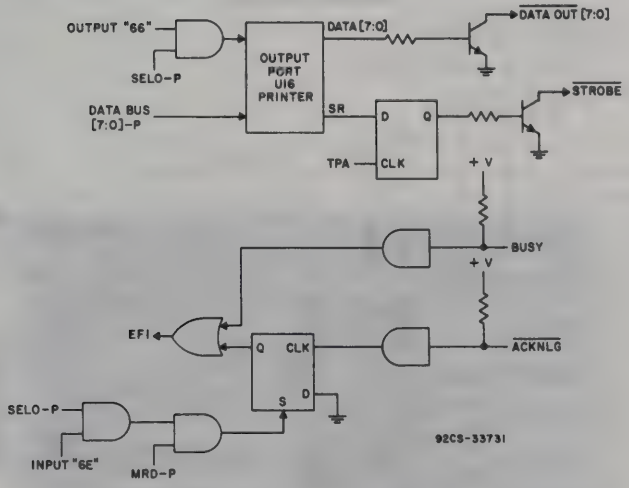


Fig. 2 - RCA COSMAC Microboard Parallel I/O Interface Module - Block Diagram of Printer Interface Logic.

CDP18S646

command generates the SEL0-P signal on board and enables the CDP18S646. For access to the printer, data is written into the printer output port by a 66 output instruction under Group I control (SEL0-P). The service request output is used to set the output strobe line at the end of TPA and is then reset by the next TPA pulse generated by the CPU. This strobe meets the timing requirements for the Centronics-type parallel printer interface and is illlustrated in Fig. 3.

Typical operation between the printer and the CPU is as follows. (1) The CPU tests EF1 to determine if the printer is ready to receive data. (2) If the printer is ready, the CPU sends out a character and tests EF1 for acknowledgement of that character. (3) The CPU then tests EF1 again to determine if the next character may be sent.

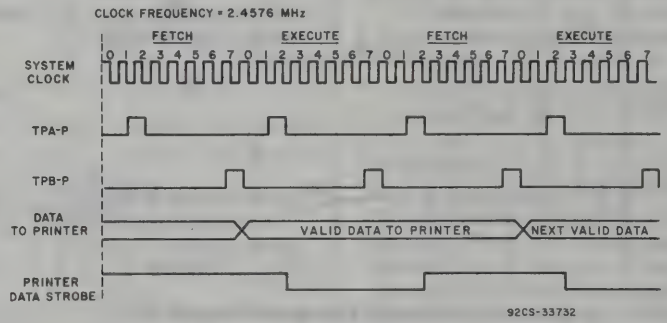
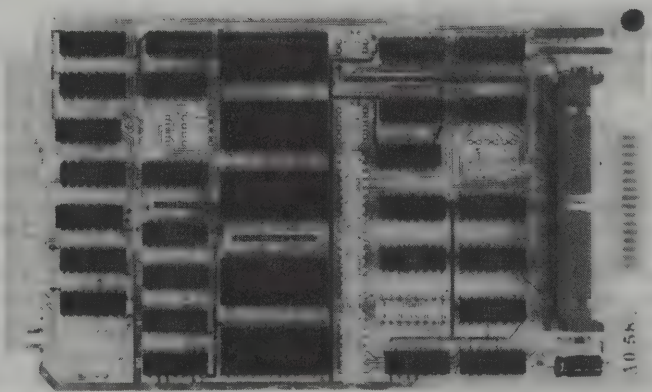


Fig. 3 - RCA COSMAC Microboard Parallel I/O Interface Module - Timing Diagram for the Printer Interface.



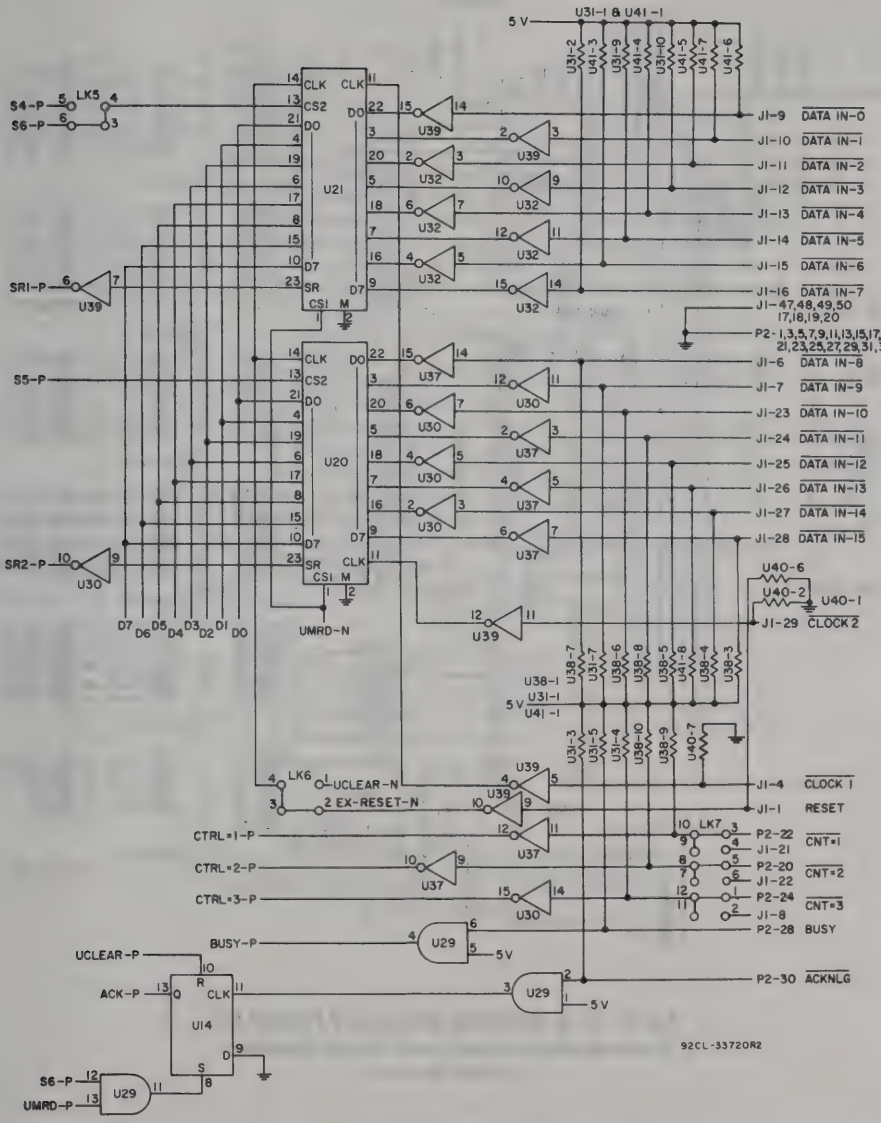


Fig. 4 - RCA COSMAC Microboard Parallel I/O Interface Module Logic and Circuit Diagram - Input Portion.

CDP18S646

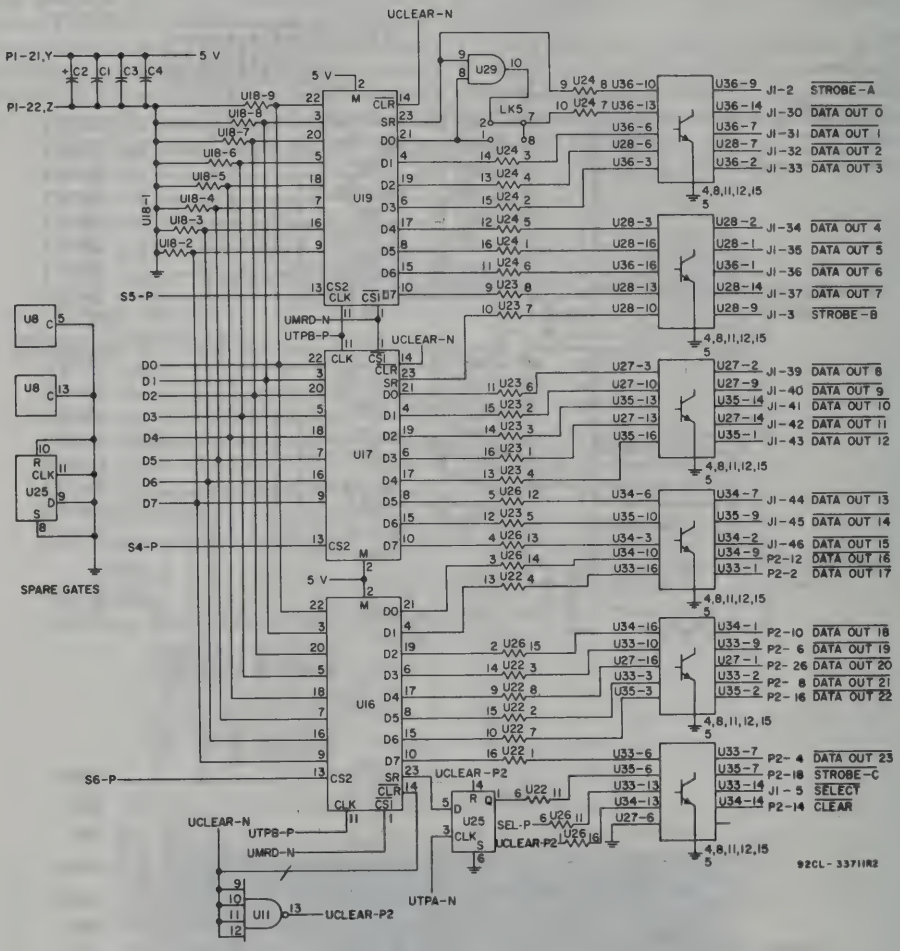


Fig. 5 - RCA COSMAC Microboard Parallel I/O Interface Module Logic and Circuit Diagram - Output Portion.

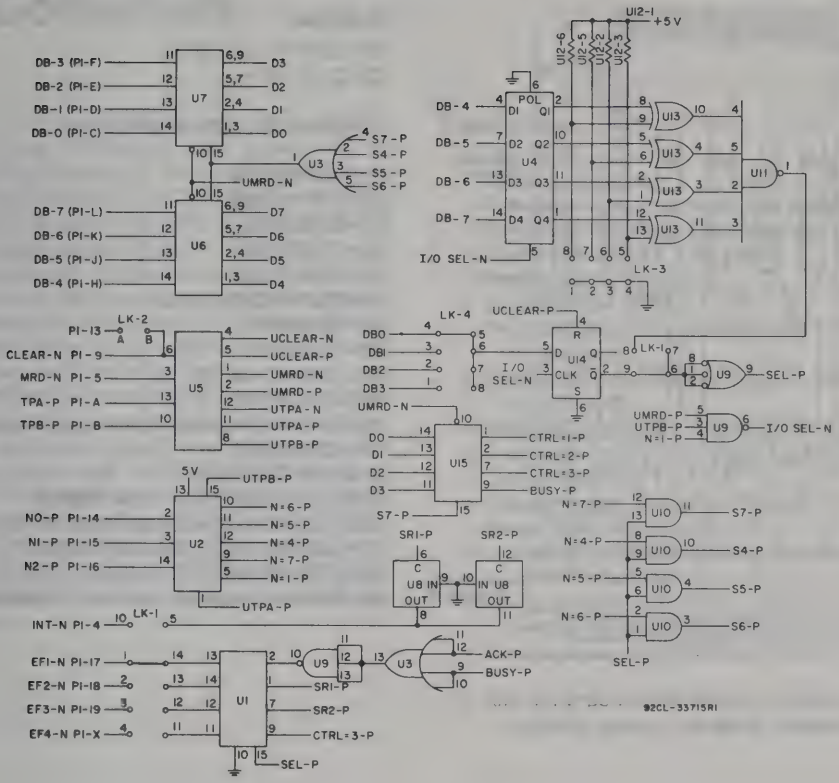


Fig. 6 - RCA COSMAC Microboard Parallel I/O Interface Module Logic and Circuit Diagram - Control Portion.

CDP18S646

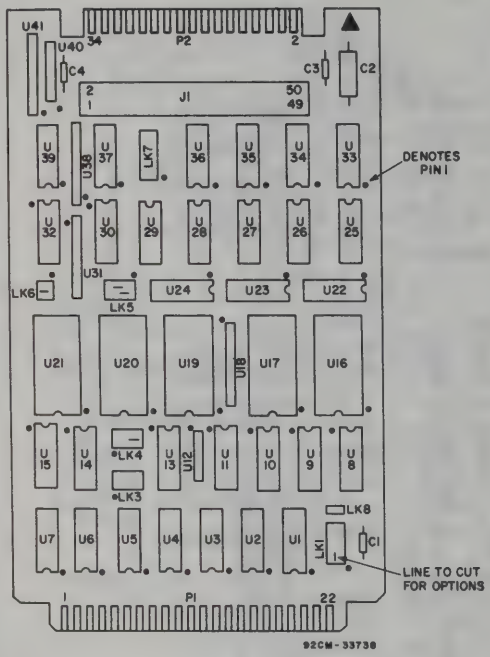


Fig. 7 - RCA COSMAC Microboard Parallel I/O Interface Module - Layout Diagram.

Parts List

C1,C3,C4=0.1 μF, 50 V
C2=22 μF, 25 V

J1=connector, right angle 50 pin

U1=CDP1856CE
U2=CDP1853CE
U3=CD4072BE
U4=CD4042BE
U5=CD4041UBE
U6,U7,U15=CDP1857CE
U8=CD4066BE
U9=CD4023BE
U10,U29=CD4081BE
U11=CD4012BE
U12,U18,U40=resistor network, 22 kilohms
U13=CD4070BE
U14,U25=CD4013BE
U16,U17,U19,U20,U21=CDP1852CE
U22,U23,U24,U26=resistor network, 2.2 kilohms
U27,U28,U33,U34,U35,U36=CA3083
U30,U32,U37,U39=CD4049UBE
U31,U38,U41=resistor network, 3.3 kilohms

CDP18S647, CDP18S657

RCA COSMAC Microboard D/A Converters

The RCA COSMAC Microboard D/A Converters CDP18S647 and CDP18S657 both contain two independent digital-to-analog conversion systems, each having 8-bits of resolution. The CDP18S647 is capable of both unipolar and bipolar operation. The CDP18S657 is capable of unipolar operation only.

These Microboards operate from a single 5-volt power supply, require minimal currents because of their primarily CMOS design, and feature two-level I/O address latching and decoding onboard, with selectable addresses for flexible system configurations.

The CDP18S647 and CDP18S657 are designed for use in a Microboard computer system, are expandable by use of the COSMAC Microboard Universal Backplane, and are plug-in compatible with the RCA Prototyping Systems CDP18S691 and CDP18S692, the RCA COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III), and the RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate hardware and software development.

Features

- Low Power
- High noise immunity
- Operating temperature range -40° C to +85° C
- Operable from a single 5-volt supply
- Small board size (4.5 x 7.5 inches)
- Simple system interface
- Assignable I/O address
- Two independent D/A channels with 8-bits of resolution
- Straight binary or offset binary input codes (CDP18S647)
- Straight binary input codes (CDP18S657)
- Unipolar or bipolar output voltage (CDP18S647)
- Unipolar output voltage (CDP18S657)
- Ribbon cable output connector
- Expandable by use of the COSMAC Microboard Universal Backplane
- Compatible with COSMAC Development Systems
- Member of extensive Microboard family

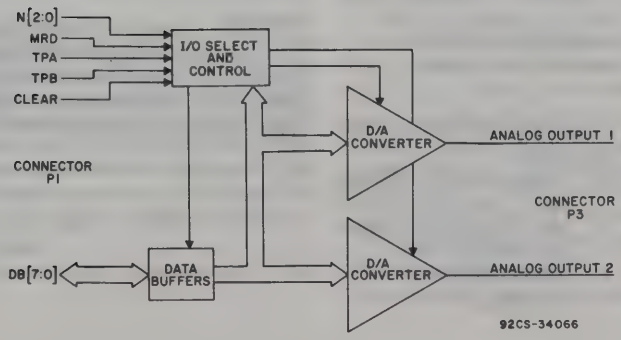


Fig. 1 - Block Diagram of D/A Section of RCA Microboard D/A Converters CDP18S647 and CDP18S657.

CDP18S647, CDP18S657

Specifications

D/A Output

Output Range:
Unipolar operation: 0 V to +2.5 V, 0 V to +2.56 V
Bipolar operation: -2.5 V to +2.5 V, -2.56 V to +2.56 V (CDP18S647)

Output Drive Capability:
Source = 50 mA typical
Sink = 10 kΩ pull-down resistor to V neg.
(V neg. = 0 V on CDP18S657, V neg. ≈ -3.0 V on (CDP18S647)
Output impedance = 2 Ω

D/A Input

Unipolar operation: Straight binary
Bipolar operation: Offset binary (CDP18S647)

D/A Transfer Characteristics

Resolution: 8 bits
Settling time (For any step size to within 1/2 LSB) : 15 μs

D/A Accuracy

Differential Linearity: ± 1/2 LSB
Power Supply Sensitivity: ± 0.08% of full-scale range/% supply volts
Gain Error: Adjustable to zero
Offset Error: Adjustable to zero

Operating Temperature Range

-40°C to +85°C

Dimensions

4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch: 0.5 inch (12.7 mm) minimum

Power Requirements

CDP18S647: + 5V supply @ 22 mA typical
CDP18S657: + 5V supply @ 9 mA typical

Connectors

System interface: Edge fingers, 44 pins on 0.156-inch centers
Analog output interface: Right-angle 10-pin header. Berg part No. 65496-001 or equivalent. Mates with Berg part No. 65847-003/004 or equivalent

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboards, CDP18S647 and CDP18S657. For additional information on these signals, refer to the published data for the CDP1802A COSMAC Microprocessor (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.** These signals are summarized in Table 1 which gives a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on RCA COSMAC Microboards, CDP18S647 and CDP18S657.

DB7 through DB0 - Eight bidirectional data bus lines. Taken directly from the CPU bus, these lines transfer the data from the CPU to the converter and the control logic.

N0, N1, N2 - Taken directly from the CPU pins, these lines indicate that an I/O instruction is being executed. They are derived from the three low-order bits of the N-register and are valid only during an I/O instruction. These lines are decoded to control the transfer of data between the data bus and the RCA Microboards CDP18S647 and CDP18S657.

$\overline{\text{MRD}}$ - Derived from the most significant bit of the N register, this signal defines the direction of the I/O data transfer. A low level indicates a transfer from memory to I/O; and a high level, a transfer from I/O to memory.

TPA, TPB - Timing Pulses generated by the CPU which occur once in each machine cycle. Used primarily for latching the data and N lines.

$\overline{\text{CLEAR}}$ - A low level on this line, indicating a system reset, clears the conversion-complete flip-flop, sets the input mode to fixed channel, selects channel 0, internally resets the D/A Converter, and places the sample-and-hold circuitry in the sample mode.

CDP18S647, CDP18S657

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P *	In/Out	Data Bus	3	RNU-P	—	Run Utility
D	DB1-P *	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Control
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Control
M	A0-P	Out	Multiplexed Address Bus	11	-5 V/ - 15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
Y	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+ 12 V/ + 15 V	—	Auxiliary Power
Y	+5 V *	In	+5 volts dc	21	+5 V *	In	+5 volts dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

* Signals used on RCA COSMAC Microboards CDP18S647 and CDP18S657.

Two-Level I/O Addressing Conventions

During an I/O instruction, the CPU presents the three low-order bits of its N register on the N2, N1 and N0 lines. N3 generates the MRD signal to indicate the direction of the data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In the Microboard system, the following conventions are established:

The OUT 1 (61) instruction is used to transmit a group select number. The output byte is latched and decoded by any Microboard in the system having an I/O function.

The group number is divided into two parts. The lower four bits are linearly encoded and the upper four bits are binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the 6 commands left after reserving the 61 and 69 instructions. The total number of useful I/O addresses is 114.

The INP 1 (69) instruction is reserved for reading the latched output of the 61 instruction. The CDP18S647 and the CDP18S657 do not provide this feature.

The CDP18S647 and the CDP18S657 are pre-assigned by links to group select 30. To enable these Microboards, a 61 instruction followed by the hex data 30 is required.

CDP18S647, CDP18S657

Once the Microboard has been selected, additional I/O instructions establish modes of operation, begin conversion, and read the data (Note: To change group select code see Table II).

Table II - I/O Group Select Code Connections

I/O Group Select Code	Link LK5 Pin Connections
10	1:8
20	2:7
30*	1:8, 2:7
40	3:6
50	1:8, 3:6
60	2:7, 3:6
70	1:8, 2:7, 3:6
80	4:5
90	1:8, 4:5
A0	2:7, 4:5
B0	1:8, 2:7, 4:5
C0	3:6, 4:5
D0	1:8, 3:6, 4:5
E0	2:7, 3:6, 4:5
F0	1:8, 2:7, 3:6, 4:5

*LK5 is pre-linked for group select code 30.

Control Circuit Operation

The **I/O Select and Control** circuitry consists of CMOS gates, latches, buffers and decoders. This circuitry is used to initialize and select the Microboard. Once this Microboard is selected, the I/O Select and Control circuitry decodes and implements commands, and controls data flow between various parts of the Microboard and the backplane.

The **data buffers** consist of a pair of CMOS CDP1857CE (U34, U35) 4-bit bus separators with enable/disable and data in/data out control pins. These types isolate the board from the backplane and thus minimize loading effects on the backplane.

On board CMOS **voltage converters,** two for the CDP18S647 (U12, U17) and one for the CDP18S657 (U17), are used to supply the necessary voltages for bipolar (CDP18S647) and unipolar (CDP18S647, CDP18S657) operation.

Analog Output

The **digital-to-analog converter** used on the CDP18S647 and CDP18S657 essentially contains an 8-bit CMOS latch, CMOS buffers, a precision R-2R ladder network, and output driver circuitry. When a D/A Converter is given a convert command, the digital value that is to be converted and output is present on the data lines. The 8-bit latch is used to latch this information. The latches drive CMOS buffers (used for level shifting) which in turn drive a precision R-2R ladder network. The output of the R-2R ladder goes to the output driver circuitry.

The two D/A commands discussed below are used to control the D/A section of these Microboards.

OUT 3 (63) instruction - This instruction selects D/A channel 1, latches the digital value present on the data bus (the byte output by this instruction), and begins a conversion.

OUT 4 (64) instruction - This instruction selects D/A channel 2, latches the digital value present on the data bus (the byte output by this instruction), and begins a conversion.

Digital Input/Analog Output

The digital input codes that the CDP18S647 will accept are straight binary (used for unipolar operation) and offset binary (used for bipolar operation). The CDP18S657 is limited to unipolar operation and thus will accept only straight binary. The analog output as a function of the digital input for both codes is given in Table III.

CDP18S647, CDP18S657

Table III - Analog Output as a Function of the Digital Input for CDP18S647 and CDP18S657

Unipolar Operation, CDP18S647 and CDP18S657			Bipolar Operation, CDP18S647		
Digital Input (Straight Binary)	**Fraction of Full-Scale Value**	**Analog Output +2.5 Volts Full Scale**	**Digital Input (Offset Binary)**	**Fraction of Full-Scale Value**	**Analog Output +2.5 Volts Full Scale**
1111 1111	+FS-1LSB	2.490234375V	1111 1111	+FS-1LSB	2.48046875V
1100 0000	+3/4 FS	1.875V	1110 0000	+3/4 FS	1.875V
1000 0000	+1/2 FS	1.25V	1100 0000	+1/2 FS	1.25V
0100 0000	+1/4 FS	0.625V	1010 0000	+1/4 FS	0.625V
0000 0001	+1LSB	0.009765625V	1000 0001	+1LSB	0.01953125V
0000 0000	0	0V	1000 0000	0	0V
			0111 1111	-1LSB	-0.01953125V
			0110 0000	-1/4 FS	-0.625V
			0100 0000	-1/2 FS	-1.25V
			0010 0000	-3/4 FS	-1.875V
			0000 0000	-FS	-2.5V

Note: The analog output values shown are theoretical values.

The digital input code and the analog output voltage range are link-selectable. The link connections are summarized in Table IV. The CDP18S657 has both D/A channels prelinked for straight binary input code and an analog output voltage range of 0V to 2.5V. The CDP18S647 has both D/A channels prelinked for offset binary input code and an analog output voltage range of -2.5V to 2.5V.

The analog outputs are available at the right-angle connector P3. The pin assignments are given in Table V.

Table IV - Digital Input/Analog Output Links

D/A Channel	Input Mode	Output Voltage	Link LK2
1	Straight Binary	0V to 2.5V	4:5 Open
	Offset Binary (CDP18S647 only)	-2.5V to 2.5V (CDP18S647 only)	4:5 Closed
2	Straight Binary	0V to 2.5V	3:6 Open
	Offset Binary (CDP18S647 only)	-2.5V to 2.5V (CDP18S647 only)	3:6 Closed

CDP18S647, CDP18S657

Table V - Analog Outputs - Connector P3 Pin Assignments

Channel 1 Output	P3-2
Channel 2 Output	P3-9
Grounds	P3-1,3,7,8,10
Spares	P3-4,5,6

D/A Adjustment Procedures

Potentiometers are provided on the CDP18S647 and CDP18S657 Microboards for both gain and offset adjustments. For D/A channel 1, potentiometer R5 adjusts the offset and R3 adjusts the gain. For D/A channel 2, R6 adjusts the offset and R4 adjusts the gain.

Selected digital input codes and their corresponding analog output voltages are listed in Table III. To adjust the offset, select the board and execute the appropriate output command with the output byte 0000 0000, then adjust the offset potentiometer to achieve the desired analog output (≈ 0.00V for unipolar operation, ≈ -2.50V for bipolar operation). To adjust the gain, select the board and execute the appropriate output command with the output byte 1111 1111, then adjust the gain potentiometer to achieve the desired analog output (≈2.49V for unipolar operation, ≈ 2.48V for bipolar operation).

Installation In The COSMAC Development Systems

The CDP18S647 and CDP18S657 Microboards may be installed in any of the available I/O slots (14-18 or 21-23) in the COSMAC Development System (CDS II) CDP18S005, COSMAC DOS Development System (CDS III) CDP18S007, and in the Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may be easily allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When either the CDP18S647 or the CDP18S657 Microboard is installed in COSMAC Development Systems CDP18S005 or CDP18S007, the system signals indicated in Table VI must be connected on the backplane to the I/O slot on the CDS selected for the Microboard.

Table VI - CDS Backplane Connections (CDP18S005 and CDP18S007 only)

Signal	Jumper to Pin
N0-P	P1-14
N1-P	P1-15
N2-P	P1-16
Clear-N	P1-9

The CDP18S647 and CDP18S657 can be installed in the Microboard Computer Development Systems CDP18S693 and CDP18S694 and RCA Prototyping Systems CDP18S691 and CDP18S692 without any modifications.

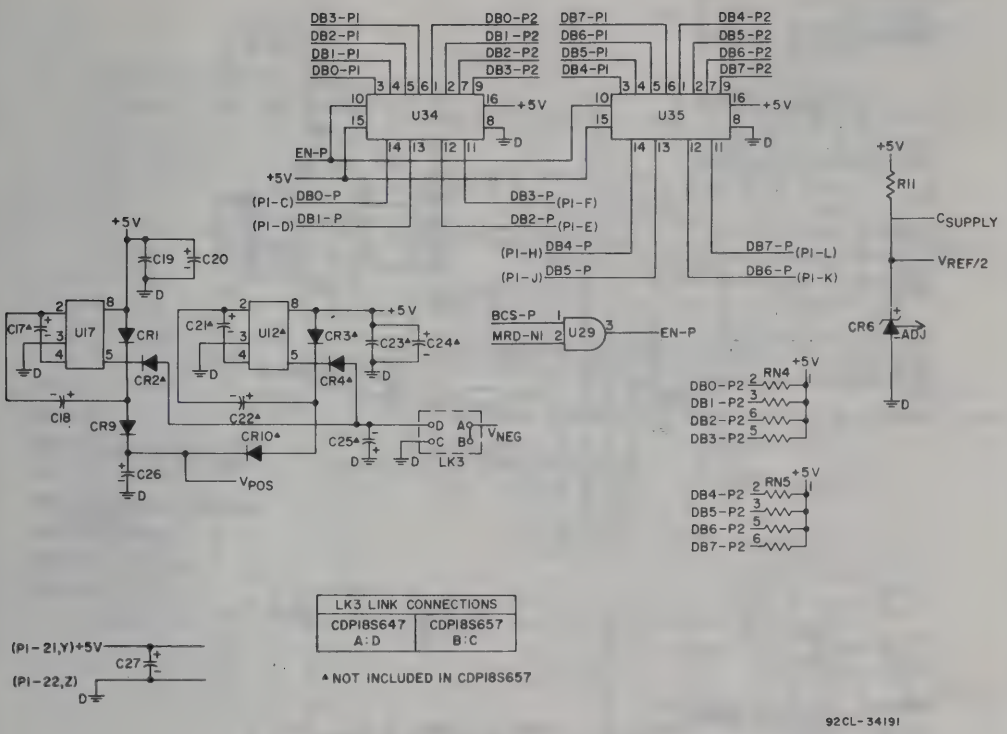


Fig. 2 - RCA COSMAC Microboard D/A Converters CDP18S647 and CDP18S657 -- Voltage Converter, Data Buffer Portion.

CDP18S647, CDP18S657

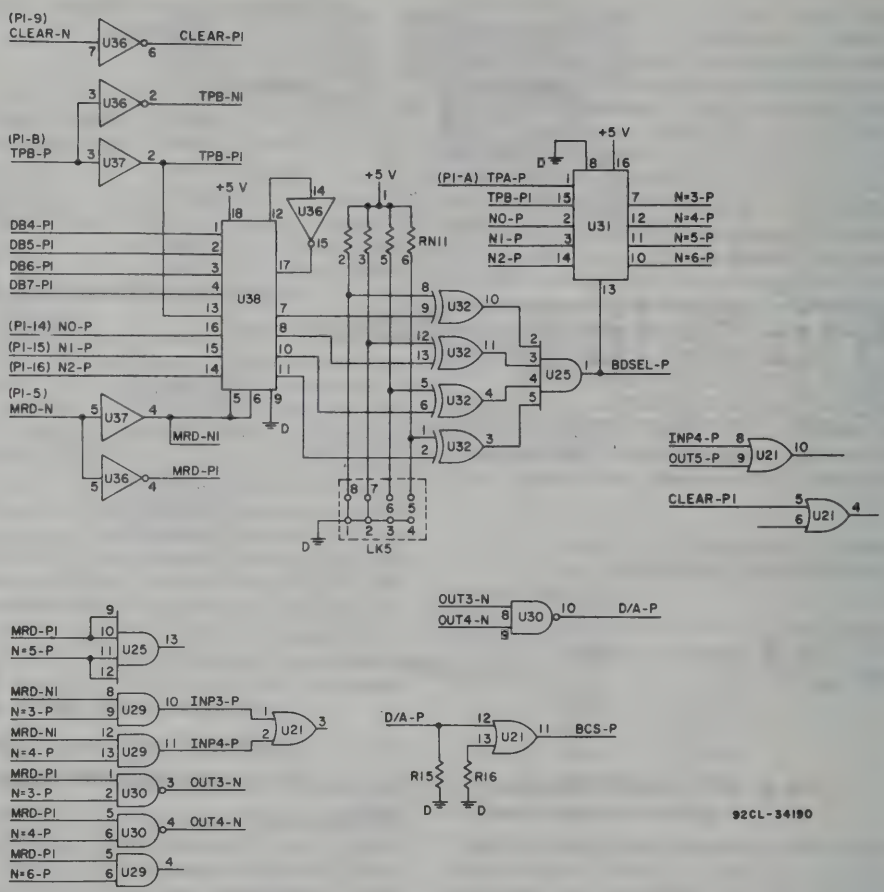


Fig. 3 - RCA COSMAC Microboard D/A Converters CDP18S647 and CDP18S657 -- I/O Select and Control Portion.

CDP18S647, CDP18S657

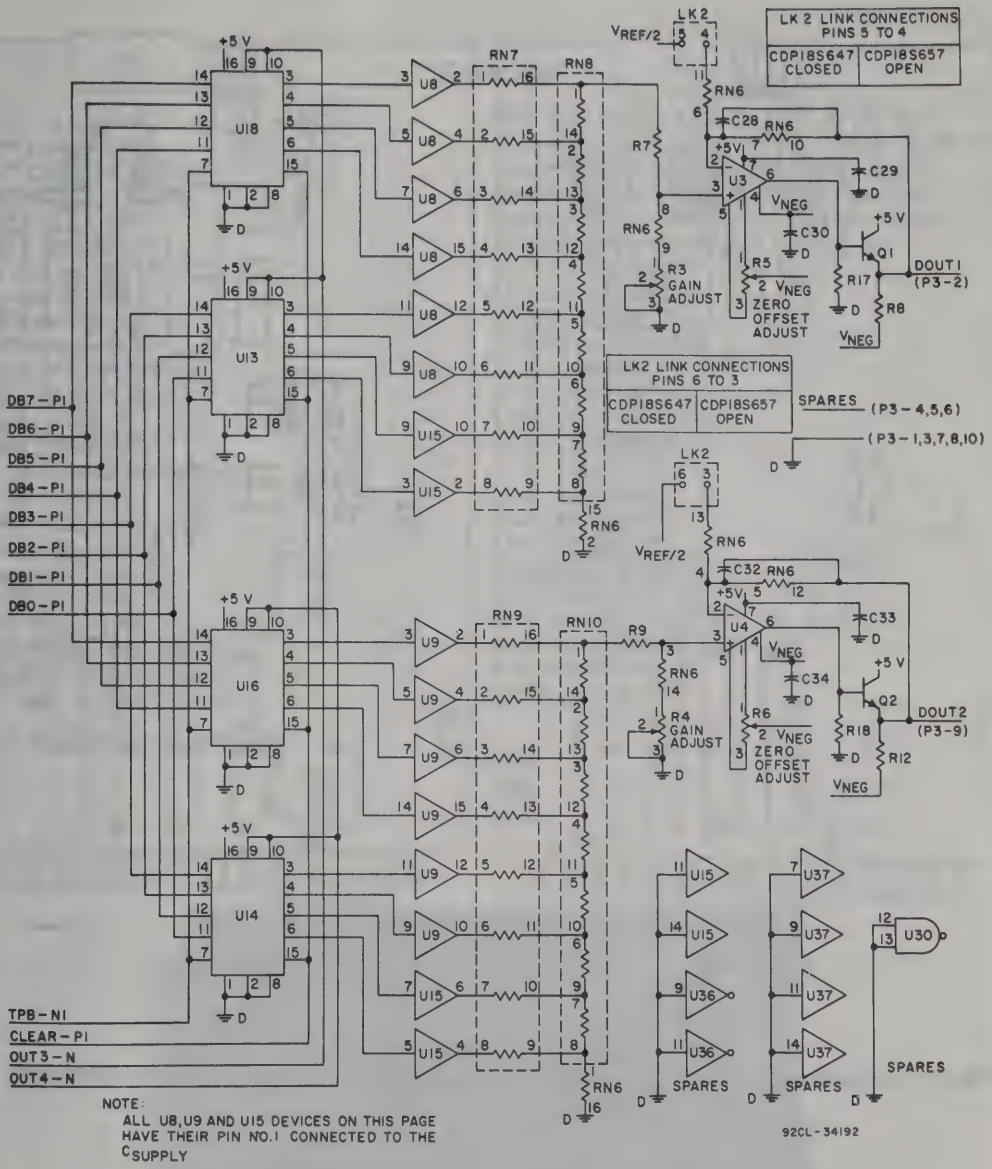


Fig. 4 - RCA COSMAC Microboard D/A Converters CDP18S647 and CDP18S657 -- D/A Converter Portion.

CDP18S647, CDP18S657

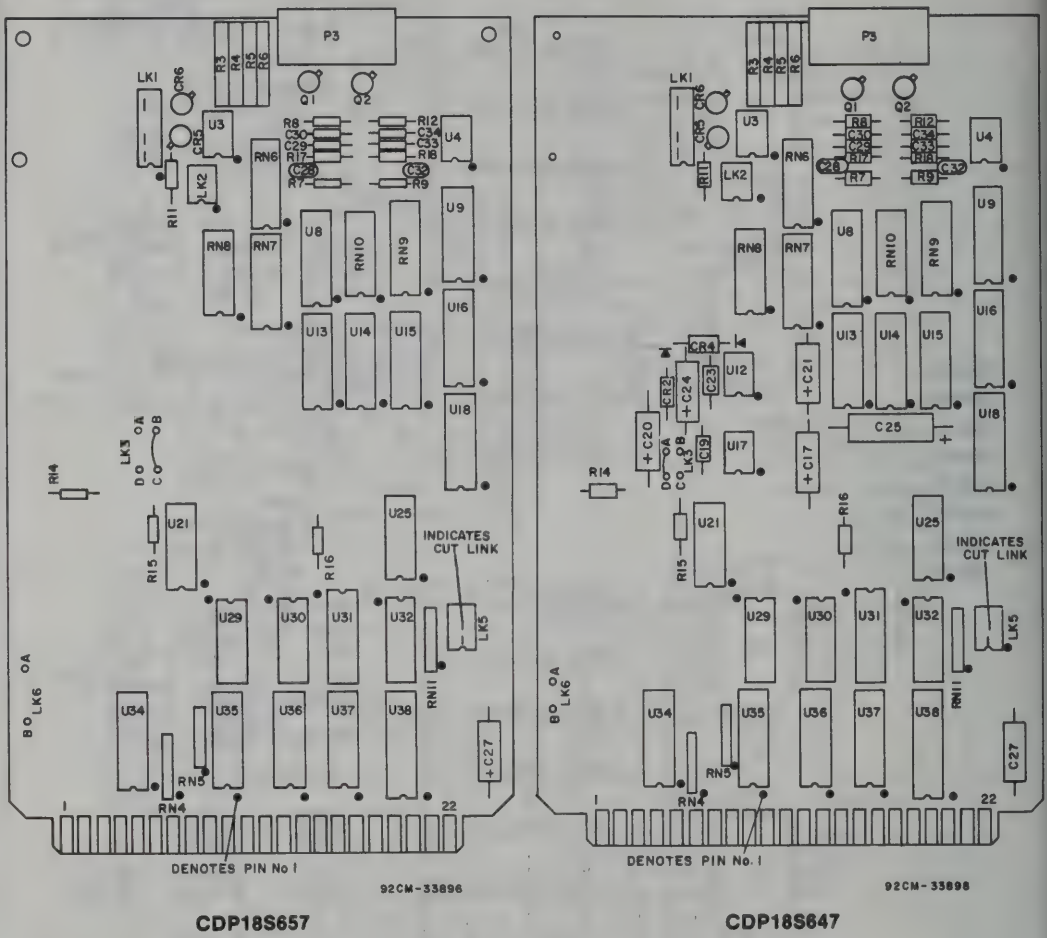


Fig. 5 - Layout Diagram of RCA COSMAC Microboard D/A Converters CDP18S647 and CDP18S657.

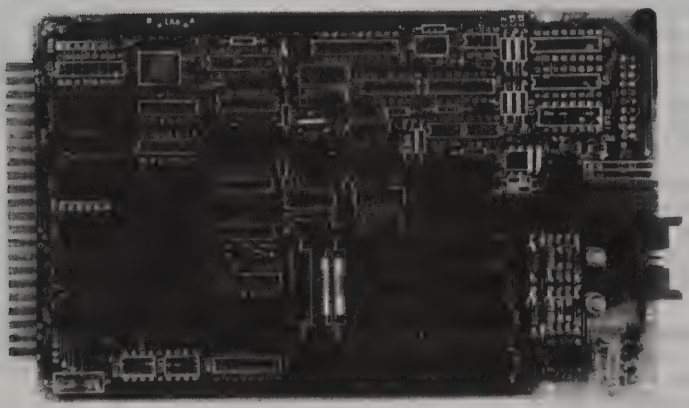
CDP18S647, CDP18S657

Parts List

C17• = 15 μF, 20V
C19• = 0.1 μF 15V
C20•, C21• =15 μF, 20V
C23• = 0.1 μF, 15V
C24• = 15 μF, 20V
C25• = 100 μF, 10V
C27 = 15 μF, 20V
C28 = 22 pF, 15V
C29, C30 = 0.1 μF, 15V
C32 = 22 pF, 100V
C33, C34 = 0.1 μF, 15V
CR2•, CR4• = 1N270
CR5 = LM113H
CR6 = LM236
P3 = Connector, 10 position
Q1, Q2 = 2N2222
R3-R6 = 100 kΩ, variable
R7 = 22 kΩ, 1/4W, 5%
R8 = 10 kΩ, 1/4W, 5%
R9 = 22 kΩ, 1/4W, 5%
R11 = 360 Ω, 1/4W, 5%
R12 = 10 kΩ, 1/4W, 5%
R14, R16 = 22 kΩ, 1/4W, 5%
R17, R18 = 2.7 kΩ, 1/4W, 5%

•Not Included In The CDP18S657

RN4, RN5 = Resistor Module SIP, 22 kΩ, 6-pin
RN6, RN7 = IC Resistor Module, 100 kΩ, 1%, 16-pin
RN8 = IC Resistor Module, 50 kΩ, 1%, 14-pin
RN9 = IC Resistor Module, 100 kΩ, 1%, 16-pin
RN10 = IC Resistor Module, 50 kΩ, 1%, 14-pin
RN11, Resistor Module SIP, 22 kΩ, 6-pin
U3, U4 = CA3160AE
U8, U9 = CD4050BE
U12• = ICL7660CPA
U13, U14 = CD4076BE
U15 = CD4050BE
U16 = CD4076BE
U17• = ICL7660CPA
U18 = CD4076BE
U21 = CD4071BE
U25 = CD4082BE
U29 = CD4081BE
U30 = CD4011BE
U31 = CDP1853CE
U32 = CD4070BE
U34, U35 = CDP1857CE
U36 = CD4049UBE
U37 = CD4050BE
U38 = CDP1867CE



CDP18S648, CDP18S658

RCA COSMAC Microboard A/D Converters

The RCA COSMAC Microboard A/D Converters CDP18S648 and CDP18S658 both contain an analog-to-digital conversion system each having 8-bits of resolution. The CDP18S648 is capable of both unipolar and bipolar operation. The CDP18S658 is capable of unipolar operation only.

These Microboards operate from a single 5-volt power supply, require minimal currents because of their primarily CMOS design, and feature two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations.

The CDP18S648 and CDP18S658 are designed for use in an RCA Microboard computer system, are expandable by use of the COSMAC Microboard Universal Backplane, and are plug-in compatible with the RCA Prototyping Systems CDP18S691 and CDP18S692, the RCA COSMAC Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III), and the RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate hardware and software development.

Features

- **Multiplexed inputs - 16 single-ended or 8 differential**
- **Sample-and-hold circuitry**
- **8-bits of resoltuion**
- **Scanned or fixed channel mode**
- **Straight binary or offset binary output codes (CDP18S648)**
- **Straight binary output codes (CDP18S658)**
- **Unipolar or bipolar input voltage (CDP18S648)**
- **Unipolar input voltage (CDP18S658)**
- **Ribbon-cable input connector**
- **Low power**
- **High noise immunity**
- **Operating temperature range — 40° C to +85° C**
- **Operable from a single 5-volt supply**
- **Small board size (4.5 x 7.5 inches)**
- **Simple system interface**
- **Assignable I/O address**
- **Expandable by use of the COSMAC Microboard Universal Backplane**
- **Compatible with COSMAC Development Systems**
- **Member of extensive Microboard family**

Specifications

A/D Input
No. of Channels: 16 single-ended/8 differential
Input Common Mode Range:
0 V to +2.7 V, (CDP18S658)
–2.7 V to +2.7 V (CDP18S648)
Input Voltage Range:
Unipolar operation 0 V to +2.5 V
Bipolar operation — 2.5 V to +2.5 V (CDP18S648 only)

A/D Output
Unipolar Operation: Straight binary
Bipolar Operation: Offset binary (CDP18S648 only)

A/D Transfer Characteristics
Resolution: 8 bits
Conversion Time: 215 μs max.
Total Common Mode Error Over A/D Input Range (Differential Input): <1/4 LSB

A/D Accuracy
Differential Linearity: ±3/4 LSB
Power Supply Sensitivity: ±0.16% of full-scale range/% supply volts
Gain Error: Adjustable to zero
Offset Error: Adjustable to zero

Operating Temperature Range
–40°C to +85°C

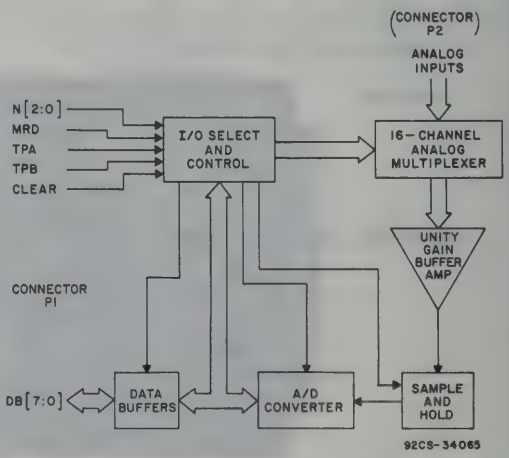


Fig. 1 — Block Diagram of RCA COSMAC Microboard A/D Converters CDP18S648 and CDP18S658.

CDP18S648, CDP18S658

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch: 0.5 inch (12.7 mm) minimum

Power Requirements
CDP18S648: +5 V supply @ 40 mA typical
CDP18S658: +5 V supply @ 13 mA typical

Connectors
System interface: Edge fingers, 44 pins on 0.156-inch centers
Analog input interface: Right-angle 20-pin header. Berg part no: 65496-007 or equivalent. Mates with Berg part no. 65847-021/022 or eqivalent

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard, CDP18S648 and CDP-18S658. For additional information on these signals, refer to the published data for the CDP1802A COS-MAC Microprocessor (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.** These signals are summarized in Table I which gives a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on RCA COSMAC Microboards, CDP18S648 and CDP18S658.

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus, these lines transfer the data from the CPU to the converter and the control logic.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate that an I/O instruction is being executed. They are derived from the three low-order bits of the N-register and are valid only during an I/O instruction. These lines are decoded to control the transfer of data between the data bus and the RCA Microboards CDP18S648 and CDP18S658.

$\overline{\text{MRD}}$ — Derived from the most significant bit of the N register, this signal defines the direction of the I/O data transfer. A low level indicates a transfer from memory to I/O; and a high level, a transfer from I/O to memory.

TPA, TBP — Timing Pulses generated by the CPU which occur once in each machine cycle. Used primarily for latching the data and N lines.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$ — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. One of these lines and/or the **$\overline{\text{INT}}$** line is used to signal the CPU that the conversion is complete and that data is available. The particular line(s) chosen is link-selectable, see Table II. The **$\overline{\text{EF1}}$** connection is preprinted.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connection (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P*	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P*	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P*	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P*	In/Out	Data Bus	4	INT-N*	In	Interrupt Request
E	DB2-P*	In/Out	Data Bus	5	MRD-N*	Out	Memory Read
F	DB3-P*	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P*	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P*	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P*	In/Out	Data Bus	9	CLEAR-N*	In	Clear-Mode Request
L	DB7-P*	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P*	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P*	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P*	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N*	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N*	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N*	In	External Flag
X	EF4-N*	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V*	In	+5 V dc	21	+5 V*	In	+5 V dc
Z	GND*	In	Digital Ground	22	GND*	In	Digital Ground

*Signals used on RCA COSMAC Microboards CDP18S648, CDP18S658.

CDP18S648, CDP18S658

Table II
CPU Lines Available for Conversion — Complete Signal

CPU Line	Link LK4	Link LK6
EF1-N	4:5*	—
EF2-N	3:6	—
EF3-N	2:7	—
EF4-N	1:8	—
INT-N	—	A:B

*Preprinted

$\overline{\text{INT}}$ — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited or enabled under software control. If Interrupt Enable (IE) is set, recognition of **$\overline{\text{INT}}$** results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as the program counter.

$\overline{\text{CLEAR}}$ — A low level on this line, indicating a system reset, clears the conversion-complete flip-flop, sets the input mode to fixed channel, selects channel 0, internally resets the A/D Converter, and places the sample-and-hold circuitry in the sample mode.

Two-Level I/O Addressing Conventions

During an I/O instruction, the CPU presents the three low-order bits of its N register on the N2, N1, and N0 lines. N3 generates the **$\overline{\text{MRD}}$** signal to indicate the direction of the data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In the Microboard system, the following conventions are established:

The OUT 1 (61) instruction is used to transmit a group select number. The output byte is latched and decoded by any Microboard in the system having an I/O function.

The group number is divided into two parts. The lower four bits are linearly encoded and the upper four bits are binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the 6 commands left after reserving the 61 and 69 instructions. The total number of useful I/O addresses is 114.

The INP 1 (69) instruction is reserved for reading the latched output of the 61 instruction. The CDP18S648 and the CDP18S658 do not provide this feature.

The CDP18S648 and the CDP18S658 are preassigned by links to group select 30. To enable these Microboards, a 61 instruction followed by the hex data 30 is required. Once the Microboard has been selected, additional I/O instructions establish modes of operation, begin conversion, and read the data. (Note: To change group select code, see Table III).

Table III
I/O Group Select Code Connections

I/O Group Select Code	Link LK5 Pin Connections
10	1:8
20	2:7
30*	1:8, 2:7
40	3:6
50	1:8, 3:6
60	2:7, 3:6
70	1:8, 2:7, 3:6
80	4:5
90	1:8, 4:5
A0	2:7, 4:5
B0	1:8, 2:7, 4:5
C0	3:6, 4:5
D0	1:8, 3:6, 4:5
E0	2:7, 3:6, 4:5
F0	1:8, 2:7, 3:6, 4:5

*LK5 is pre-linked for group select code 30.

Control Circuit Operation

The **I/O Select and Control** circuitry consists of CMOS gates, latches, buffers and decoders. This circuitry is used to initialize and select the Microboard. Once this Microboard is selected, the I/O Select and Control circuitry decodes and implements commands, and controls data flow between various parts of the Microboard and the backplane.

The **data buffers** consist of a pair of CMOS CDP1857CE (U34, U35) 4-bit bus separators with enable/disable and data in/data out control pins. These types isolate the board from the backplane and thus minimize loading effects on the backplane.

On-board CMOS **voltage converters,** two for the CDP18S648 (U12, U17) and one for the CDP18S658 (U17) are used to supply the necessary voltages for bipolar (CDP18S648) and unipolar (CDP18S648, CDP18S658) operation.

A/D Input (See Figure 1)

The **analog multiplexer** stage consists of two CMOS CD4051BE (U1, U2) 1 of 8 multiplexers that can be configured by the use of links to provide 16 single-ended channels or 8 differential input channels. These switches can be sequentially scanned or randomly selected under software control. See Table IV for linking of Input Mode.

Table IV — Input Mode Selection

Input Mode	Link LK1
Single-Ended	2:13, 4:11, 5:10, 7:8
Differential	*1:14, 3:12, 6:9

*Preprinted link connections.

The **unity-gain buffer-amplifier** stage consists of BIMOS CA3260AE (U6, U7) op-amps connected in a unity-gain instrumentation-amplifier configuration. This stage is used to provide differential input capability and high input impedance.

The **sample-and-hold amplifier** CA3160AE (U5) acquires and holds analog signals. When a convert command is given, the sample-and-hold amplifier is switched to the hold mode and when the conversion is complete, it is switched back to the sample mode. A built-in delay allows for amplifier settling times.

The **analog-to-digital converter** is an 8-bit successive-approximation CMOS component (U10). A variable, on-board voltage reference is used to adjust the gain of the converter; a separate potentiometer adjusts the offset.

A/D Commands

The four commands discussed below control the A/D conversion

OUT 5 (65) instruction — This instruction resets the service request flip-flop and begins a conversion cycle. The byte output by this instruction specifies the input channel. When the board is configured for the **single-ended input mode** the four least significant bits provide a binary selection of the input channel (1 to 16 individual channels). When the board is configured for the **differential input mode,** the **three** least significant bits provide a binary selection of the input channel (1 of 8 channel pairs). The remaining bits are ignored by the channel select logic (See Table V). Upon receiving a system reset, channel 0 is selected if in the single-ended mode; channel pair 0^+ 0^- is selected if in the differential mode.

Table V — Channel Selection Code (Byte output with 65 instruction)

Single-Ended Input Mode		Differential Input Mode	
Byte Output	Channel Selected	Byte Output	Channel Pair Selected
XXXX 0000	0	XXXXX 000	0^+, 0^-
XXXX 0001	1	XXXXX 001	1^+, 1^-
XXXX 0010	2	XXXXX 010	2^+, 2^-
XXXX 0011	3	XXXXX 011	3^+, 3^-
XXXX 0100	4	XXXXX 100	4^+, 4^-
XXXX 0101	5	XXXXX 101	5^+, 5^-
XXXX 0110	6	XXXXX 110	6^+, 6^-
XXXX 0111	7	XXXXX 111	7^+, 7^-
XXXX 1000	8		
XXXX 1001	9		
XXXX 1010	10		
XXXX 1011	11		
XXXX 1100	12		
XXXX 1101	13		
XXXX 1110	14		
XXXX 1111	15		

X's are "don't cares", totally ignored by the channel select logic.

OUT 6 (66) instruction — The byte output by this instruction specifies the channel selection mode. The seven most significant bits in the output byte are ignored. When the least significant bit is 0, the fixed channel mode is selected. When the least significant bit is 1, the sequential scan mode is selected. Upon receiving a system reset, the channel selection is set to the fixed channel mode (See Table VI).

Table VI —Channel Selection Mode (Byte output with 66 instruction)

Byte Output	Mode Selected
XXXXXXX 0	Fixed Channel
XXXXXXX 1	Sequential Scan

X's are "don't cares", totally ignored by the channel selection mode logic.

INP 3 (6B) instruction — This instruction inputs the 8 data bits from the A/D converter and resets the service request flip-flop.

INP 4 (6C) instruction — This instruction inputs the 8 data bits from the A/D converter, resets the service request flip-flop, and initiates another conversion. In addition, INP 4 (6C) will incre-

CDP18S648, CDP18S658

Table VII — Digital Output as a Function of Input Voltage for CDP18S648 and CDP18S658

Unipolar Operation, CDP18S648 and CDP18S658			Bipolar Operation, CDP18S648		
Analog Input +2.5V Full Scale	Fraction of Full-Scale Value	Digital Output (Straight Binary)	Analog Input +2.5V Full Scale	Fraction of Full-Scale Value	Digital Output (Offset Binary)
2.490234375 V	FS-1LSB	1111 1111	2.48046875 V	FS-1LSB	1111 1111
1.875 V	+3/4 FS	1100 0000	1.875 V	+3/4 FS	1110 0000
1.25 V	+1/2 FS	1000 0000	1.25 V	+1/2 FS	1100 0000
0.625 V	+1/4 FS	0100 0000	0.625 V	+1/4 FS	1010 0000
0.3125 V	+1/8 FS	0010 0000	0.3125 V	+1/8 FS	1001 0000
0.009765625 V	+1 LSB	0000 0001	0.01953125 V	+1 LSB	1000 0001
0 V	0	0000 0000	0 V	0	1000 0000
			-0.01953125 V	-1 LSB	0111 1111
			-0.3125 V	-1/8 FS	0111 0000
			-0.625 V	-1/4 FS	0110 0000
			-1.25 V	-1/2 FS	0100 0000
			-1.875 V	-3/4 FS	0010 0000
			-2.48046875 V	-FS-1LSB	0000 0001
			-2.5 V	-FS	0000 0000

Note: The analog input voltages given are theoretical center step values.

ment the channel prior to starting another conversion if the sequential scan mode has been enabled.

NOTE: The channels wrap e.g. incrementing channel pair 7^+, 7^-, will select channel pair 0^+, 0^-; incrementing channel 15 will select channel 0 if in the single-ended input mode.

Digital Output/Analog Input

The digital output codes that the CDP18S648 can produce are straight binary (used for unipolar operation) and offset binary (used for bipolar operation). The CDP18S658 is limited to unipolar operation and thus produces only straight binary. The digital output as a function of the input voltage for both codes is given in Table VII.

The digital output code and the analog input voltage range are link selectable. These links are summarized in Table VIII. The CDP18S658 is prelinked for straight binary output code and an input voltage range of 0 V to 2.5 V. The CDP18S648 is prelinked for offset binary output code and an input voltage range of -2.5 V to 2.5 V.

The analog inputs, available at the right angle connector P2, may be configured as 16 single-ended inputs or as 8 differential inputs. The input mode, which is determined by link LK1 (see Table IV), is prelinked for differential inputs. The pin assignments for the two modes are listed in Table IX.

Table VIII Digital Output/Analog Input Links

Output Mode	Input Voltage Range	Link LK2
Straight Binary	0 V to 2.5 V	2:7 Open
Offset Binary (CDP18S648 only)	-2.5 V to 2.5 V	2:7 Closed

Table IX Pin Assignments for Connector P2

Pin	Channel	
	Single-Ended	Differential
1	0	0+
2	8	0-
3	1	1+
4	9	1-
5	2	2+
6	10	2-
7	3	3+
8	11	3-
9	4	4+
10	12	4-
11	5	5+
12	13	5-
13	6	6+
14	14	6-
15	7	7+
16	15	7-
17	GND	GND
18	GND	GND
19	GND	GND
20	SPARE	SPARE

A/D Adjustment Procedures

Potentiometers are provided on the CDP18S648 and the CDP18S658 Microboards for both gain and offset A/D adjustments. Adjusting the offset potentiometer, R1, moves the transfer function either up or down. Adjusting the gain potentiometer R2, varies the slope of the transfer function (see Fig. 4). The objective of this adjustment procedure is to approach the ideal transfer function for an 8-bit A/D converter.

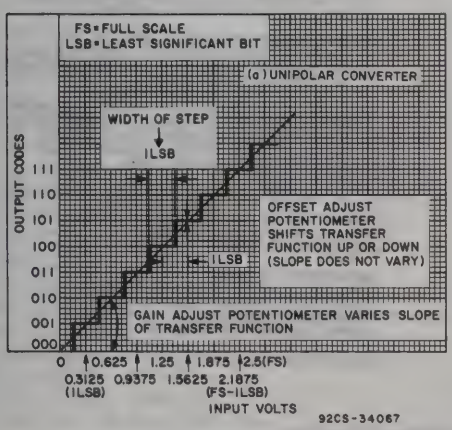
For a 3-bit converter operating in the unipolar mode, see Figs. 2 and 3, the ideal transfer function is achieved when the width of each step is equal to 1 LSB or 1/8 of 2.5 V (2.5 V-0 V) and the slope of the curve passes through the (0 V, 000) point; and for operation in the bipolar mode, when the width of each step is equal to 1 LSB or 1/8 of 5 V (2.5 V — −2.5 V) and the slope of the curve passes through the (0 V, 100) point.

An 8-bit converter operates in a similar fashion. For an 8-bit converter operating in a unipolar mode, the ideal transfer function is achieved when the width of each step is equal to 1 LSB or 1/256 of 2.5 V (2.5 V — 0 V) and the slope of the curve passes through the (0 V, 0000 0000) point; and for bipolar mode operation, when the width of each step is equal to 1/256 of 5 V (2.5 V — −2.5 V) and the slope of the curve passes through the (0 V, 1000 0000) point.

A recommended way to accurately adjust the A/D converter is by loading and running the program in Fig. 4. This program will select channel 0 (channel pair $0^+, 0^-$ if in the differential input mode) and do repeated conversions, displaying each of the eight bits on the CRT terminal. The latest value will overlay the previous value. The full procedure is as follows:

1. Set up the desired board configuration (unipolar or bipolar operation, single-ended or differential input).
2. Install Microboard in system, load and run program. Before continuing, allow a few minutes for settling.
3. On channel 0 (channel pair 0^+, 0^- if in differential input mode) apply a signal equal to the lowest acceptable analog input value plus 1/2 LSB (≈ 4.9 V for unipolar operation, ≈ −2.49 V for bipolar operation).
4. Adjust the offset potentimoter R1, so that the seven most significant bits displayed on the screen are 0's and the least significant bit is toggling between 0 and 1.
5. On channel 0 (channel pair 0^+, 0^- if in differential input mode) apply a signal equal to the full-scale (FS) value minus 1-1/2 LSB's (≈ 2.4853 V for unipolar operation, ≈ 2.4706 V for bipolar operation).
6. Adjust the gain potentiometer R2 so that the seven most significant bits displayed on the screen are 1's and the least significant bit is toggling between 0 and 1.

Note: For Microboards configured for bipolar operation, it may be necessary to go through the adjustment procedures several times to accurately adjust the Microboard.



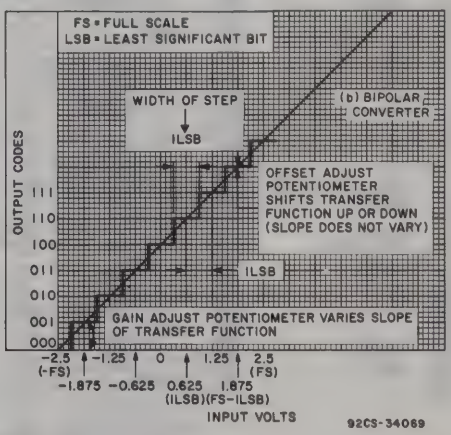


Fig. 2 — Ideal Transfer Function for a 3-Bit A/D Converter.

CDP18S648, CDP18S658

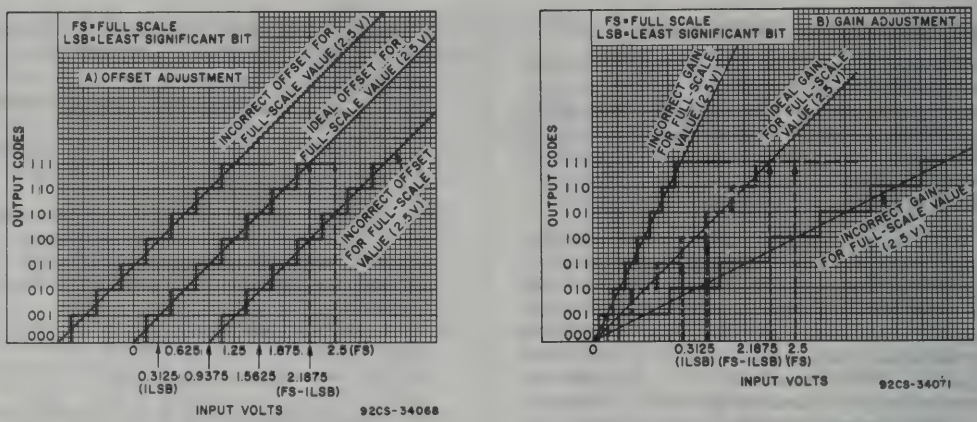


Fig. 3 — Effect of Gain and Offset Adjustments on Transfer Function of a 3-Bit A/D Converter.

```
IM
0000  :                  0001    . . A/D ADJUSTMENT PROGRAM WRITTEN IN ASM8 ASSEMBLY LANGUAGE
0000  :                  0002    . . THIS PROGRAM ASSUMES THE EXISTENCE OF A COSMAC UTILITY
0000  :                  0003    . . (EX. UT20,UT21,UT60,UT61,UT62) AT LOCATION 8000H
0000  :                  0004    STORE   EQU   07H
0000  :                  0005    PROG    EQU   03H
0000  :                  0006    INIT2   EQU   83F6H
0000  :                  0007    ADVAL   EQU   09H
0000  :                  0008    TYPE    EQU   81A4H
0000  :                  0009    CHAR    EQU   0FH
0000  :                  0010
0000  :                  0011            ORG 4000H              . . LOCATE PROGRAM AT 4000 H (ANY LOCATION WHERE
4000  :                  0012                                   . . RAM IS PRESENT MAY BE SUBSTITUTED)
4000  F840B7;            0013            A.1(DUMMY)—>STORE.1    . . SET UP DUMMY STORAGE POINTER
4003  F836A7;            0014            A.0(DUMMY)—>STORE.0
4006  F840B3;            0015            A.1(START)—>PROG.1     . . SET PROGRAM COUNTER (R 3) TO POINT TO
4009  F80FA3;            0016            A.0(START)—>PROG.0     . . BEGINNING OF PROGRAM
400C  C083F6;            0017            LBR INIT2              . . INITIALIZE REGISTERS F OR STANDARD CALL AND
400F  :                  0018                                   . . RETURN, ALSO SET UP STACK POINTER
400F  :                  0019    START
400F  E3;                0020            SEX PROG               . . SET X TO PROGRAM COUNTER (R3)
4010  6130;              0021            OUT 1;DC 30H           . . SELECT BOARD (ASSUMES BOARD SELECT IS 30H)
4012  6500;              0022            OUT 5;DC 00H           . . SELECT CHANNEL 0, RESETS THE SERVICE REQUEST
4014  :                  0023                                   . . F/F, AND BEGIN A CONVERSION
4014  E7;                0024            SEX STORE              . . SET X TO DUMMY STORAGE POINTER
4015  3C15;              0025            BN1 $                  . . WAIT UNTIL CONVERSION IS COMPLETE (ASSUMES
4017  :                  0026                                   . . CONVERSION COMPLETE SIGNAL IS LINKED TO EF1)
4017  6B;                0027            INP 3                  . . READ DATA AND RESET SERVICE REQUEST F/F
4018  A9;                0028            —>ADVAL.0              . . STORE VALUE IN A/D STORAGE REGISTER (R9)
4019  E3;                0029            SEX PROG               . . SET X TO PROGRAM COUNTER (R3)
401A  6101;              0030            OUT 1;DC 01H           . . SELECT RCA GROUP
401C  F808A8;            0031            08H—>R8.0              . . SET BIT COUNT TO 8
401F  :                  0032    CONTINUE
401F  89FEA9;            0033            ADVAL.0*2—>ADVAL.0     . . SHIFT BIT TO BE OUTPUT INTO DF
4022  F8007C30BF;        0034            00H+"30H—>CHAR.1       . . IF BIT IS A ONE OUTPUT A ONE
4027  :                  0035                                   . . ELSE OUTPUT A ZERO
4027  D481A4;            0036            CALL TYPE
402A  28;                0037            DEC R8                 . . DECREMENT BIT COUNT
402B  88;                0038            R8.0                   . . LOAD BIT COUNT INTO ACCUMULATOR
402C  3A1F;              0039            BNZ CONTINUE           . . IF ALL 8 BITS HAVE NOT BEEN OUTPUT
402E  :                  0040                                   . . CONTINUE WITH OUTPUT
402E  F80DBF;            0041            0DH—>CHAR.1            . . OUTPUT A CARRIAGE RETURN
4031  D481A4;            0042            CALL TYPE
4034  300F;              0043            BR START               . . GO BACK AND DO IT AGAIN
4036  :                  0044    DUMMY
0000
```

Fig. 4 — A/D Converter Adjustment Program.

CDP18S648, CDP18S658

Installation in Development Systems

The CDP18S648 and CDP18S658 Microboards may be installed in any of the available I/O slots (14-18 or 21-23) in the COSMAC Development System (CDS II) CDP18S005, COSMAC DOS Development System (CDS III) CDP18S007, and in the Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may be easily allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When either the CDP18S648 or the CDP18S658 Microboard is installed in COSMAC Development Systems CDP18S005 or CDP18S007, the system signals indicated in Table X must be connected on the backplane to the I/O slot on the CDS selected for the Microboard.

Table X — CDS Backplane Connections (CDP18S005 and CDP18S007 only)

Signal	Jumper to Pin
N0-P	P1-14
N1-P	P1-15
N2-P	P1-16
Clear-N	P1-9

The CDP18S648 and the CDP18S658 can be installed in Microboard Development Systems CDP18S693 and CDP18S694 and RCA Prototyping Systems CDP18S691 and CDP18S692 without any modifications.

PARTS LIST

C1, C2 = 0.1 μF, 15 V
C3 = 4700 pF. 33 V polystyrene
C4, C5 = 0.1 μF, 15 V
C6, C7 = 22 pF, 100 V
C8-C13 = 0.1 μF, 15 V
C14 = 15 μF. 20 V
C15, C16 = 0.1 μF, 15 V
C17*, C18 = 15 μF, 20 V
C19 = 0.1 μF, 15 V
C20, C21*, C22* = 15 μF, 20 V
C23* = 0.1 μF, 15 V
C24* 15 μF, 20 V
C25* = 100 μF, 10 V
C26, C27 = 15 μF, 20 V
C31 = 22 pF, 100 V
CR1, CR2*, CR3*, CR4* = 1N270
CR6 = LM236
CR7, CR8 = 1N914
CR9, CR10* = 1N270
P2 = Connector, 20 position
R1 = 100 kΩ, variable
R2 = 10 kΩ, variable
R10 = 300Ω, 1/4W, 5%
R11 = 470Ω, 1/4W, 5%
R13 = 22 MΩ, 1/4W, 5%
R14, R16 = 22 kΩ, 1/4W, 5%
*Not included in CDP18S658

RN1 = IC Resistor Module, 100 kΩ, 1%, 16-pin
RN2-RN5 = Resistor Module SIP, 22 kΩ, 6-pin
U1, U2 = CD4051BE
U5 = CA3160AE
U6, U7 = CA3260AE
U10 = ADC0803LCD
U11 = CD4066BE
U12* = ICL7660CPA
U17 = ICL7660CPA
U19 = CD4049UBE
U20 = CD4081BE
U21 = CD4071BE
U22, U23 = CD4013BE
U24 = CD4024BE
U25 = CD4082BE
U26 = CD40103BE
U27 = CD4013BE
U28 = CD4072BE
U29 = CD4081BE
U31 = CDP1853CE
U32 = CD4070BE
U33 = CD4516BE
U34, U35 = CDP1857CE
U36 = CD4049UBE
U37 = CD4050BE
U38 = CDP1867CE
Y1 = Crystal, 2.4576 MHz

CDP18S648, CDP18S658

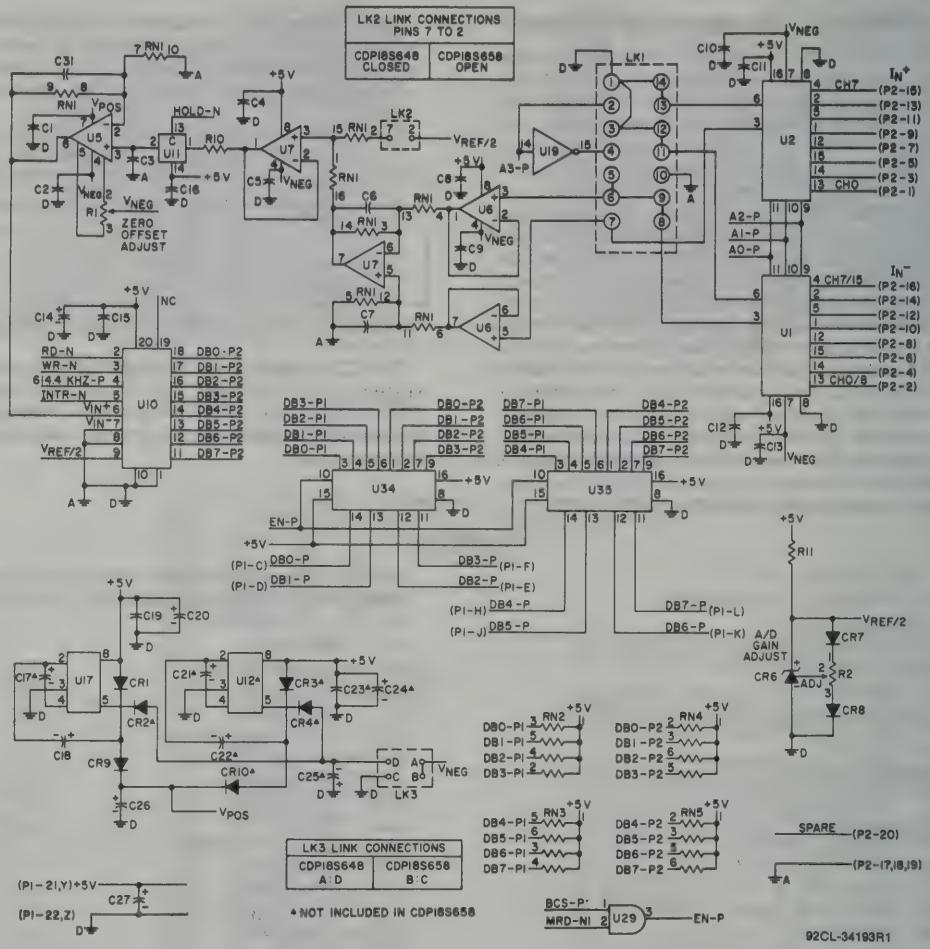


Fig. 5 - RCA COSMAC Microboard A/D Converters CDP18S648 and CDP18S658 - A/D Converter Portion

CDP18S648, CDP18S658

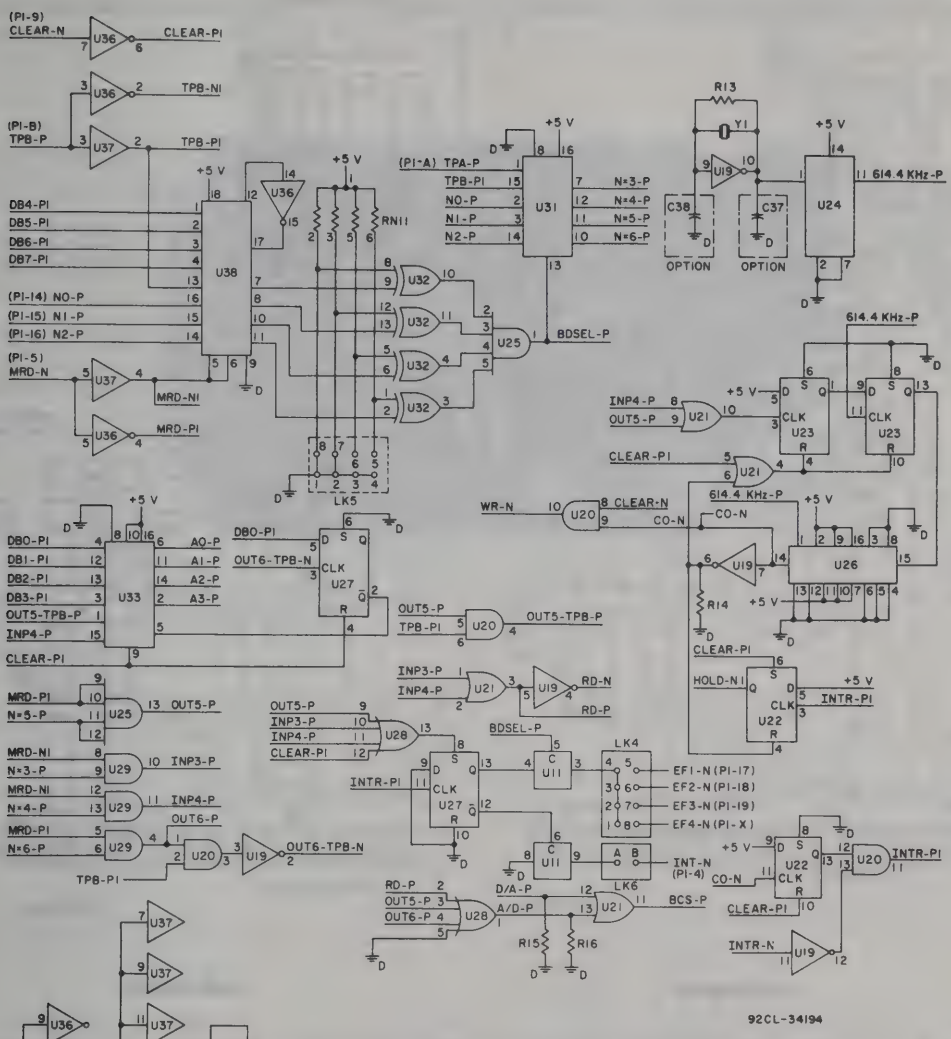
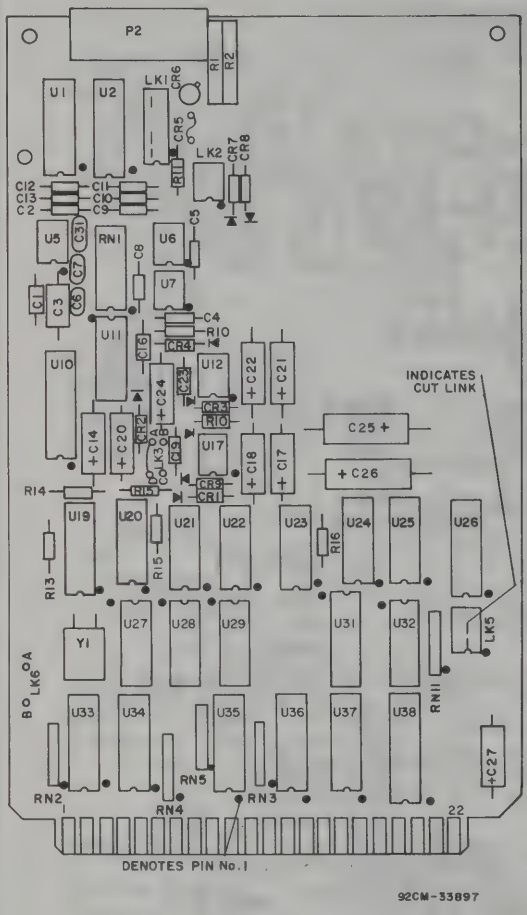
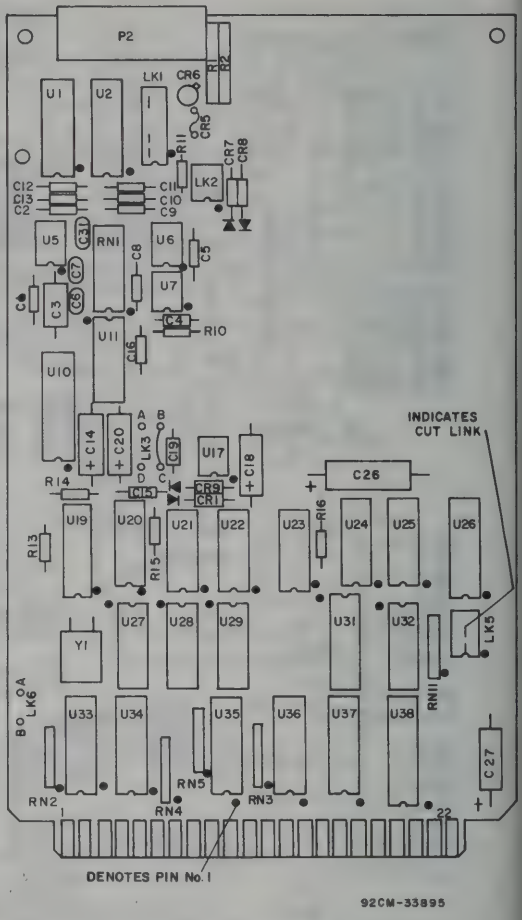


Fig. 6 – RCA COSMAC Microboard A/D Converters CDP18S648 and CDP18S658 – I/O Select and Control Portion

CDP18S648, CDP18S658



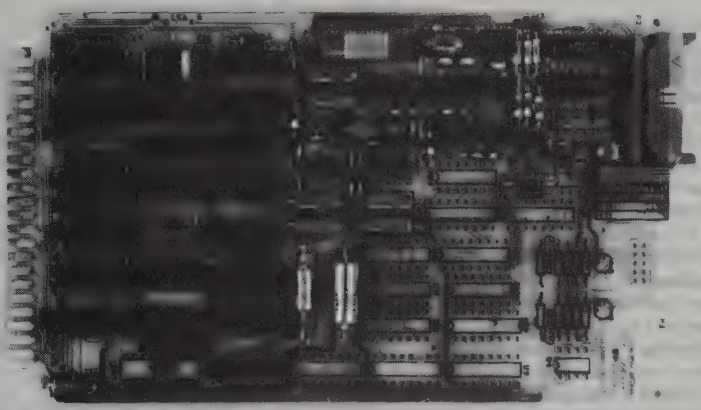
CDP18S648



CDP18S658

Fig. 7 - Layout Diagram of RCA COSMAC Microboard A/D Converters CDP18S648 and CDP18S658.

CDP18S648, CDP18S658



Advance Data

CDP18S650
RCA Microboard Octal Counter-Timer

The RCA Microboard Octal Counter-Timer CDP-18S650 provides eight independent counter-timer circuits using four CDP1878 Dual Counter-Timer IC's. Each counter-timer can be programmed to function in any of five modes allowing the design of a wide variety of gate-controlled counting time-base generators and variable-duty-cycle pulse generators. Each counter has independent clock and gate inputs as well as both true and inverted outputs on the external interface connector.

A stable 2-MHz crystal clock reference frequency is provided on the external interface for generating time bases. The crystal oscillator has a trimmer to allow precise calibration of the reference frequency at the desired operating temperature.

The external interface is made through a 36-pin header that allows interconnection by means of discrete wires using crimp-on pins in a plastic housing, or a variety of mass-terminated ribbon-cable assemblies. This arrangement permits convenient interconnection between the counter-timers and the reference clock thus allowing the cascading of multiple counters for longer word lengths.

Features

- **8 counter-timer circuits using RCA CDP1878 Dual Counter-Timer IC's**
- **On-board 2-MHz adjustable reference oscillator**
- **Discrete wire or ribbon cable input/output connector**
- **Easy interconnection for cascading**
- **Software controlled interrupts**
- **Fits RCA Industrial Series Chassis and is compatible with RCA Development Systems**
- **Wide-operating temperature range -40°C to +85°C**
- **Low-power CMOS static logic**
- **High-noise immunity**
- **Operable from single 5-volt power supply**
- **Small board size - 4.5 x 7.5 inches**
- **Assignable I/O address**
- **Simple system interface**
- **Expandable by use of RCA Microboard Universal Backplane**
- **Eight Independent Counter-Timer Circuits**
- **On-Board 2-MHz Timing Standard**

Specifications

Operating Temperature Range
-40°C to +85°C
Input Switching Threshold Voltage
Input high: 3.5 volts max.
Input low: 1.5 volts min.
Power Requirements
+5 volts at 10 milliamperes (typical)
Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board Pitch 0.5 inch (12.7 mm) minimum
Connectors
System interface: Edge fingers, 44 pins on 0.156-inch centers
External interface: Male header, 36 pins on 0.1-inch centers

Advance Data

CDP18S651

RCA Microboard Floppy Disk Controller

The RCA Microboard Floppy Disk Controller CDP-18S651 utilizes the LSI Floppy Disk Controller IC uPD765. This Microboard contains the circuitry and control functions for interfacing directly with up to 4 industry-standard 8-inch, 5-1/4-inch mini or 3-1/2-inch micro floppy disk drives. It is specially suited for the RCA MS1M 50 Micro Floppy-Disk Drive Module.

The CDP18S651 features phase-locked loop circuitry for readback tracking and write precompensation circuitry, data transfers by DMA for high-speed operation, handshaking with a system CPU via interrupt and/or flag lines, and multiple-sector transfers in both read and write with a single command. The DMA capability is available from the CPU of any RCA Microboard Computer. It also features IBM system compatibility in both single- and double- density recording formats (IBM 3740 single density format FM, or IBM system 34 double-density format MFM, single or double sided).

The CDP18S651 Microboard Floppy Disk Controller permits the user to program the track stepping rate, head load time, and head unload time. In addition, this Microboard provides the following, powerful built-in commands to simplify system control software.

Read Data
Read ID
Read Deleted Data
Read a Track
Scan Equal
Scan High or Equal
Scan Low or Equal
Specify
Write Data
Format a Track
Write Deleted Data
Seek
Recalibrate (Restore to Track 0)
Sense Interrupt Status
Sense Drive Status
Read CRC

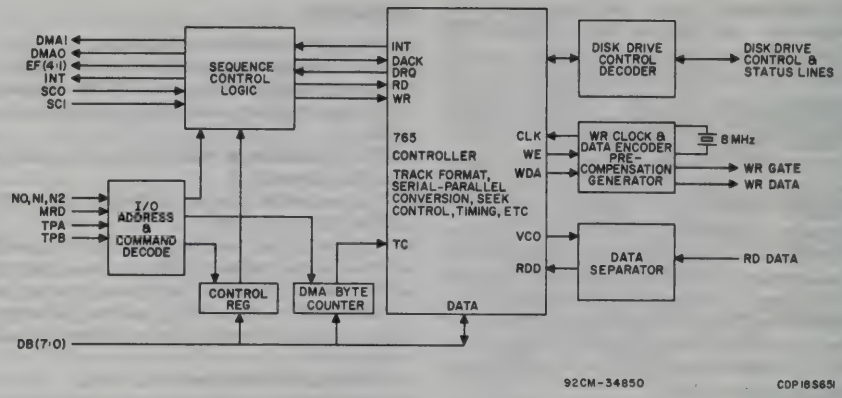
Features

- **Interrupt or non-interrupt modes**
- **Direct high-speed transfer of data by DMA**
- **Linkable outputs on board for disk interface so that disk-to-controller cable can be one-to-one for any disk drive**
- **IBM compatible in both single-and double-density recording formats**
- **Programmable data record lengths: 128, 256, 512, or 1024 bytes per sector**
- **Multi-sector and multi-track transfer capability**
- **Drives up to four floppy disks - standard, mini, or micro**
- **Data Scan Capability - Scans a single sector or an entire disk's worth of data fields, and compares byte-by-byte data in the processor's memory with data read from the disk**
- **16 commands including Read CRC**
- **Parallel seek operations on up to four drives**
- **Operates from single +5-volt supply**
- **Assignable I/O group select**
- **Compatible with RCA Microboard Universal Backplane**

Specifications

Operating Temperature Range:
0° to 70°C
Output Drive Current:
Output low @ 0.4 volt; 48 mA min.
Output high (open-drain leakage); 250 uA max.
Inputs from Disk:
Terminated in 150-ohm pull-up resistor to V_{dd}; inputs buffered by a 74LS04 Hex Inventer IC
Power Requirements:
+5 V @ 300 mA (typ)
Dimensions:
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board Pitch 0.5 inch (12.7 mm) minimum

CDP18S651



Block Diagram of RCA Microboard Floppy Disk Controller.

CDP18S652

RCA COSMAC Microboard Combination Memory and Tape I/O Module

The RCA CDP18S652 Microboard is available primarily as a replacement part for RCA COSMAC Microboard Computer Development Systems (MCDS) CDP18S693, CDP18S694, and CDP18S695. Logic and layout diagrams, a parts list, and other user information are supplied in the **User Manual for the RCA COSMAC Microboard Computer Development System (MCDS) CDP18S693 and CDP18S694**, MPM-293 and in the **User Manual for the RCA COSMAC Color Microboard Computer Development System (CMCDS) CDP18S695**, MPM-295.

Advance Data

CDP18S653V1, CDP18S653V2

RCA Microboard CMOS Direct-Connect Auto MODEMS (Bell Compatible)

The CMOS Direct-Connect Auto MODEMS CDP-18S653V1 and CDP18S653V2 are members of a new family of Microboards designed to add data communications capabilities over the switched dial-up network (DDD) to the RCA Microboard Computer line.

These Microboards provide an interface that enables any Microboard computer system to send data to or receive data from a remote location over the phone lines. The Microboard system can be fully automated from dialing, connect, and data transfer to disconnect. Operation can be simply initiated by a prompt command from the users application program.

The CDP18S653 contains two modem modules: (1) an LSI CMOS frequency-shift-keying (FSK) phase-coherent modem with all digital filtering (LSM), and (2) an FCC-approved direct-connect phone-line interface (PLI). Connected to the modem is the CMOS digital logic required to control and monitor fully auto-connect and auto-dial operation. An on-board UART, which can be run in interrupt mode, sends digital data to the LSM modem or receives digital data from it.

Typically, the CDP18S653, in conjunction with the Microboard Computer CDP18S602, forms a compact, 2-board communications system because the CDP-18S602 also has an on-board UART for user terminal interaction and sufficient memory for a wide variety of applications. Other Microboards can be added for additional I/O and/or memory capacity.

Microboards in the CDP18S653 family are available for use at 300 bits per second (Bell 103 compatible) for full-duplex operation, type CDP18S653V1, and at 1200 bits per second (Bell 202 compatible) for half-duplex operation, type CDP18S653V2. Both Microboards feature auto answer and auto originate, and dial-tone and busy-tone detection.

Features

- **All CMOS design including CMOS LSI modem**
- **FCC-approved Direct connect to phone line**
- **Auto Answer**
- **Auto Originate**
- **Manual Answer**
- **Manual Originate**
- **Self Test**
- **Dual-Tone-Multi-Frequency (DTMF) Dialing or Pulse-Dialing options**
- **Dial-tone detection for optimum speed and reliable tandem dialing**
- **Busy-tone detection for repeat dialing**
- **OFF-HOOK LED indicator**
- **Users link options for abort timers, disconnect and carrier detect**
- **Low-power-static CMOS design assures minimal power supply and cooling requirements**
- **Operating temperature range: -40°C to +85°C**
- **High noise immunity**
- **Small board size: 4.5 x 7.5 inches**
- **Member of extensive Microboard family**
- **Expandable by use of RCA Microboard Universal Backplane**
- **CDP18S653 options:**
  Type CDP18S653V1 - 300 bps for full-duplex operation. Bell 103 compatible
  Type CDP18S653V2 - 1200 bps for half-duplex operation. Bell 202 compatible

CDP18S653V1, CDP18S653V2

SPECIFICATIONS

Operating Modes:

Auto Answer: When enabled, automatically answers call at end of first ring. Programmable to answer at two or more rings.

Manual Answer: Trailing edge of manually generated input pulse from user option digital interface causes the modem to answer without incoming ring. Used when voice contact is established before entering the data mode.

Manual Originate: Manually generated input pulse from user option digital interface causes connection to line. Used in systems with external telephone set after number is dialed.

Auto Dialing: Allows DTMF (Dual-Tone Multi-Frequency) dialing and pulse dialing.

Line Busy: Digital control input sets PLI (Phone Line Interface) OFF-HOOK but opens audio path to or from telephone line. Used to prevent incoming calls during test or out-of-service modes.

Timing:

Coupler-Cut-Through($\overline{CCT}$): Audio path to or from telephone line connected 2.7 seconds ± 20% after initial line connection.

Overload Detector: 152 milliseconds @ 1 kHz. Resets $\overline{CCT}$ if line input to modem exceeds - 9 dBm.

Abort Timer Options:

Long - 18 seconds ± 20%
Short - 10 seconds ± 20%
No disconnect.
PLI will disconnect if modem carrier digital input is off.

Loss of Carrier Disconnect:

Enabled - 0.5 second ± 20%
Disabled - No disconnect.
PLI will disconnect if modem carrier is lost.
Option independent of Abort Timer.

Operating and Mechanical Characteristics:

Operating Temperature Range:

-40° C to +85° C

Power Requirements:

On-board voltage regulator has preprinted links to accept +15 volts for the two modem modules operated at +12 volts
OFF-HOOK Current: 24.5 mA at +12 volts (typical) 38 mA at +12 volts (maximum)
ON-HOOK Current: 29 mA at +12 volts (maximum)
Current for Remaining Logic: 5 mA at +5 volts (typical)
Note: Voltage regulator can be bypassed by links so that CDP18S653 Microboard is operated directly from +5 volts and +12 volts.

Dimensions:

4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Maximum component height (phone jack) 5/8 inch (15.9 mm)

Connectors:

System Interface: Edge fingers, 44 pins on 0.156-inch centers
User Option Interface (J4): Right-angle header 10 pin
Telephone Interface (J5): USOC* RJ11C
*AT&T Universal Service Ordering Code Number

PLI Interface Characteristics:

FCC Regulation:

Part 68

Registration No:

AU 492X-69442-DP-E

Ringer Equivalence:

0.8 B

Telephone Interface:

2-wire, direct connect to telephone network by means of voice jack RJ11C using line cord with modular plug.

Impedance:

ON-HOOK DC: > 20 megohms measured with - or +200 volts dc from tip or ring to ground
ON-HOOK AC: > 40 kilohms measured between tip and ring
OFF-HOOK DC: 200 ohms measured between tip and ring
OFF-HOOK AC: 600 ohms measured between tip and ring 2.7 seconds after OFF-HOOK with 600 ohms external impedance from modem

Insertion Loss:

2 dB difference between signal level measured at modem line and telephone line both terminated with 600 ohms.

Isolation:

1000 volts RMS between telephone line and power or modem interface.

Surge Protection:

1500-volt peak pulses with 10-microsecond rise time and 160-microsecond delay time.

Loop Current Distortion:

-50 dB from 200 Hz to 4000 Hz with 20 to 100 milliamperes of loop current.

Ring Detector:

Signal-frequency range: 16 to 68 Hz.
Signal-level range: 40 to 150 volts RMS

ON Delay:

192 milliseconds ± 20%

OFF Delay:

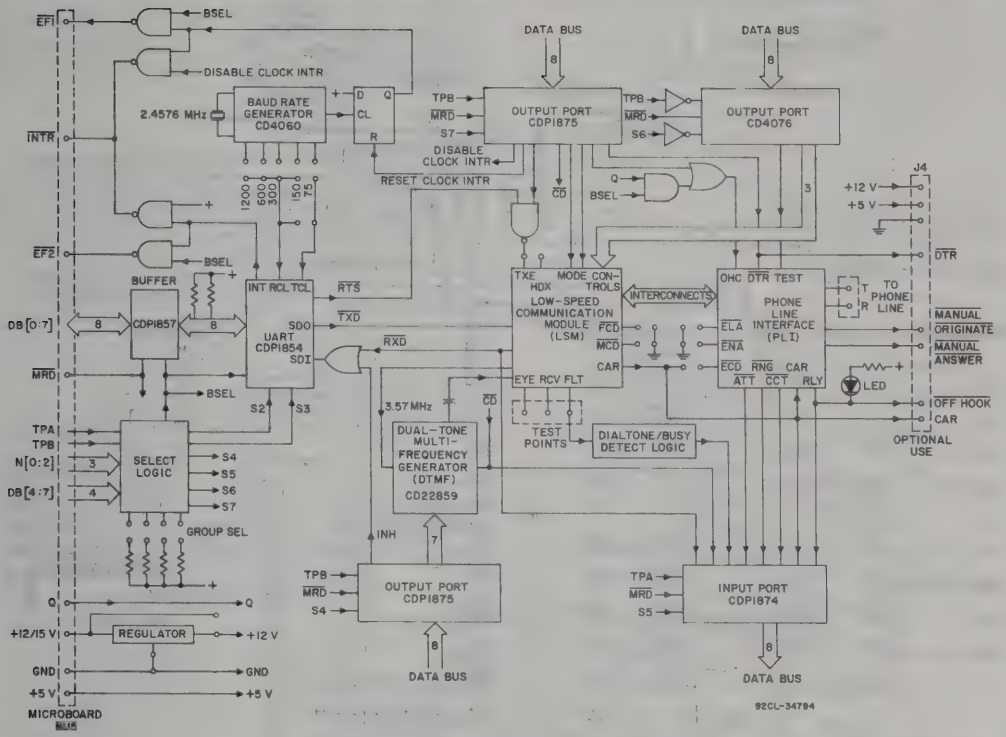
80 milliseconds ± 20%

CDP18S653V1, CDP18S653V2

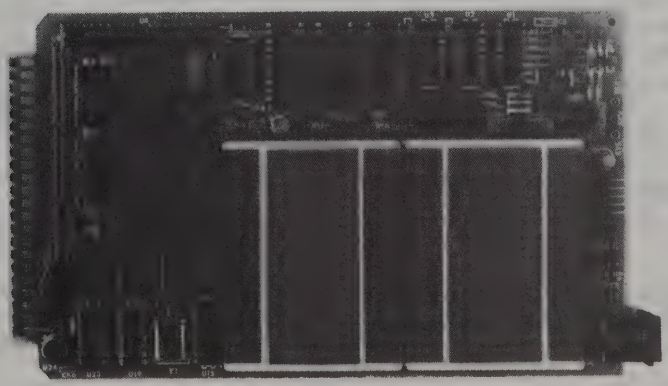
LSM Modem Characteristics

Item	CDP18S653V1	CDP18S653V2
LSM Modem Part No.	30	120
Format	Serial, binary asynchronous	
Modulation	Frequency shift keying (FSK), phase coherent	
Data Rate (bps)	0 to 300	0 to 1200
Analog Interface	2-Wire, 600-ohm	2-Wire, 600-ohm
Operating Modes	Originate/Answer Self test	Transmit/Receive Self test
Communication Mode	Full or half duplex	Half duplex, 2-wire
Modem Compatibility	Bell 103: A through G Bell 113: A,B	Bell 202: C,D,E,R,S
Delay Equalizer	Not applicable	Fixed statistical equalizer
Transmit Frequencies (Hz)	Originate: Mark: 1270 Space: 1070 Answer: Mark: 2225 Space: 2025	Mark: 1300 Space: 2100 Answer Tone: 2025 Soft Carrier: 900
Transmitter Tolerance (%)	± 0.2	±0.2
Receive Frequencies (Hz)	Originate: Mark: 2225 Space: 2025 Answer: Mark: 1270 Space: 1070	Mark: 1300 Space: 2100
Transmit Level (dBm)	-10 Includes PLI Insertion Loss	-10
Receive Level (dBm)	0 to 45	0 to 45
Carrier Detect Level (dBm)	OFF with noise levels from 0 to -60	ON with signal level range of 0 to -45
	ON with signal level range of 0 to -45	
Carrier Detect Timing (ms ±30%)	Normal Mode: ON: 150 OFF: 50	Normal Mode: ON: 38 OFF: 13
(ms max)	Fast Mode: ON: 9 OFF: 9	Fast Mode: ON: 9 OFF: 9
Receive Data: Jitter (%) Typical	7	7
Bias Distortion %	±5 with degradation of 0.6%/°C from +60 to +85°C, and -0.3%/°C from -10 to -40°C	±5

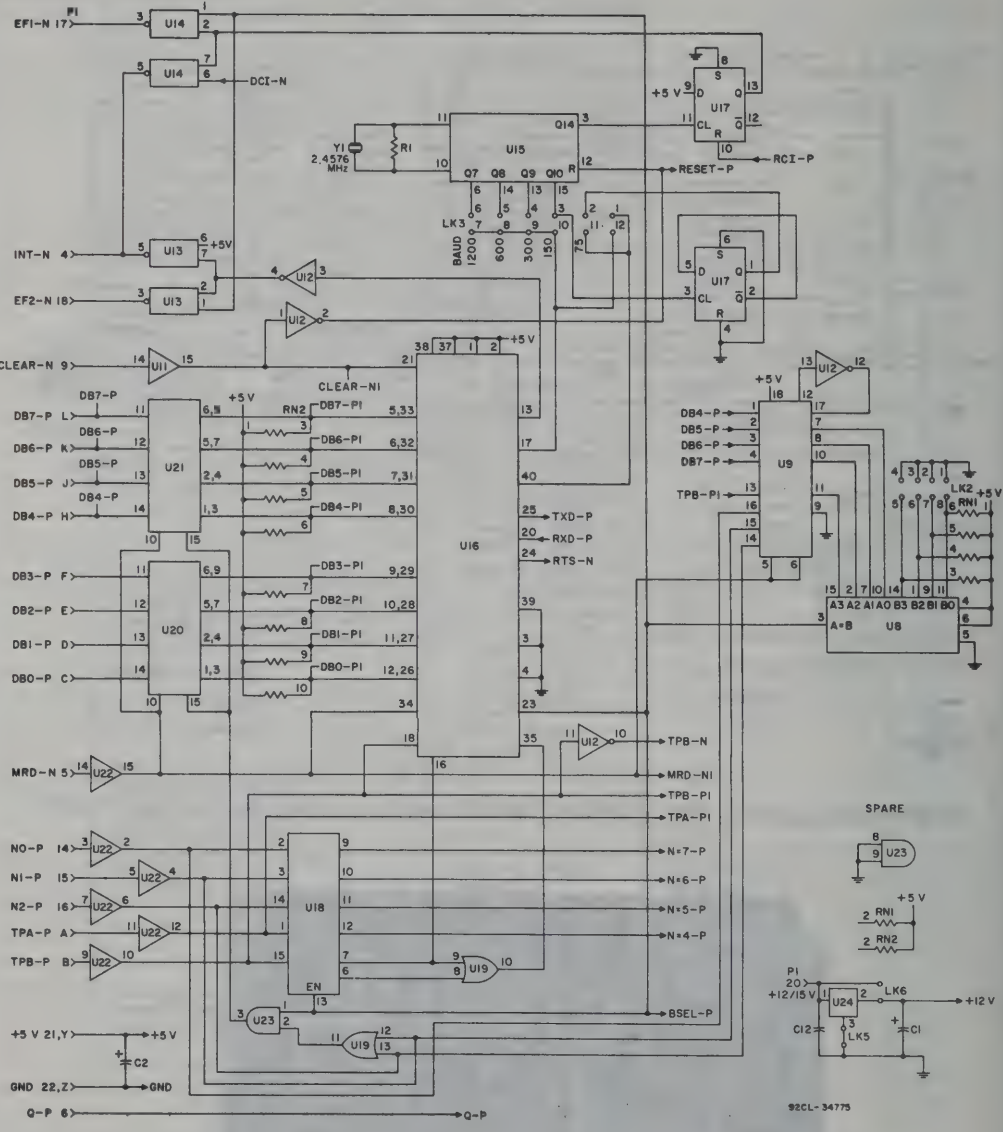
CDP18S653V1, CDP18S653V2



System Block Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653.

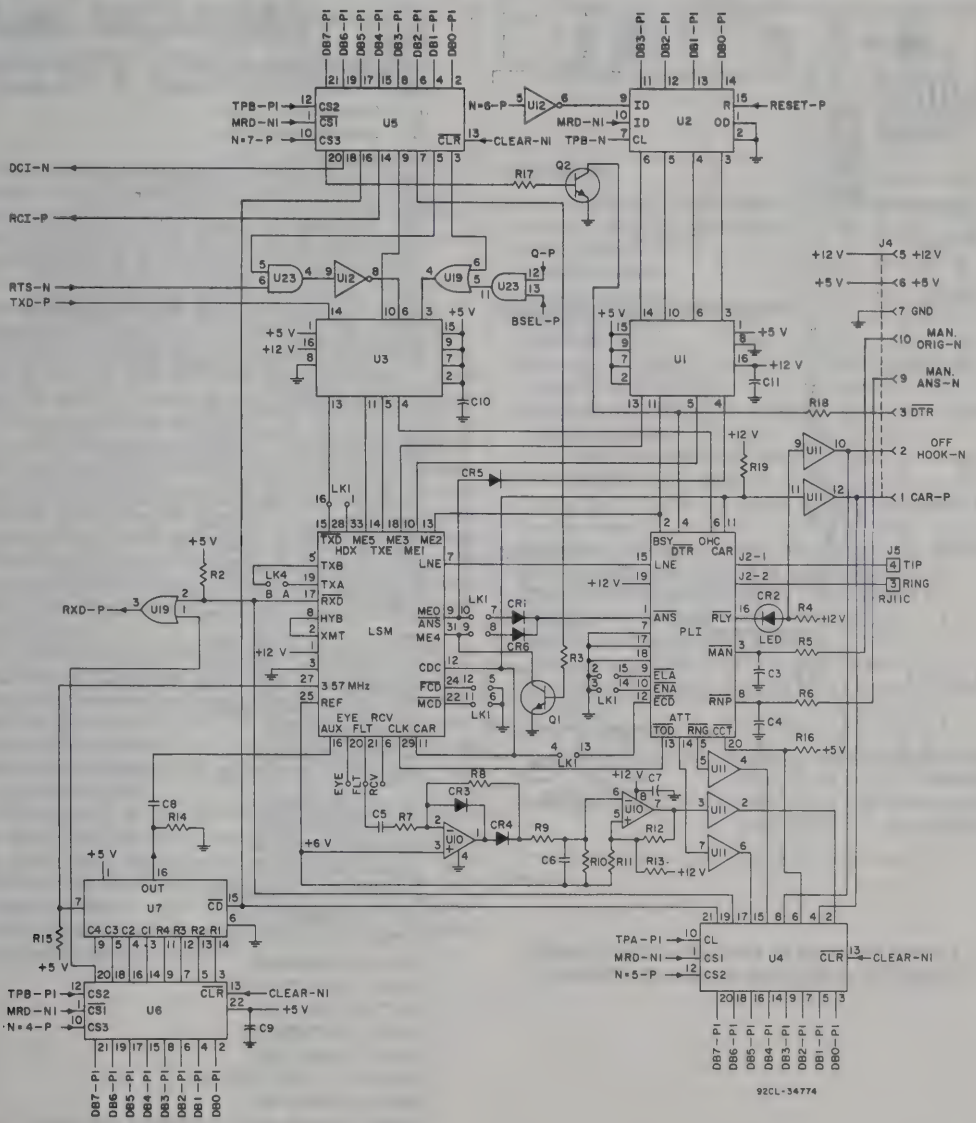


CDP18S653V1, CDP18S653V2



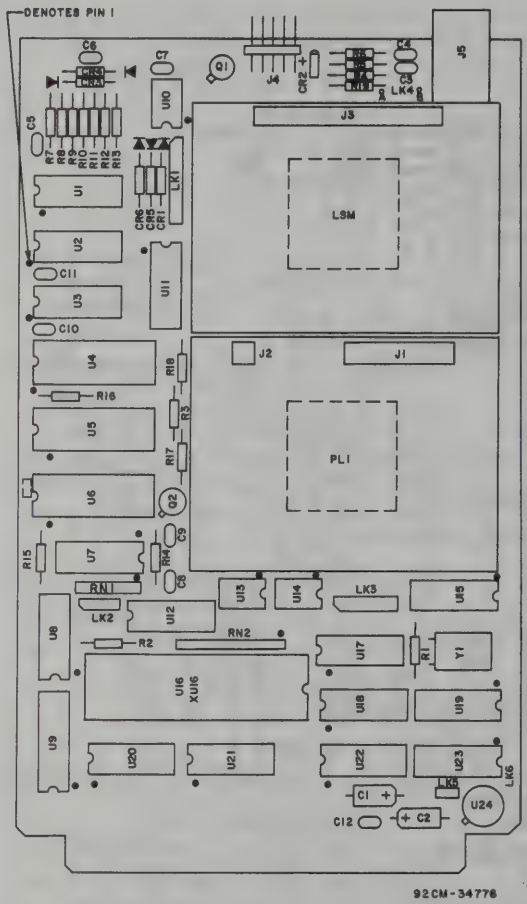
Logic Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653 - Select Logic and UART Interfaces.

CDP18S653V1, CDP18S653V2



Logic Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653 - Phone Line Interface and Modem Modules with Control Logic.

CDP18S653V1, CDP18S653V2



Layout Diagram of RCA Microboard CMOS Direct-Connect Auto Modem CDP18S653.

PARTS LIST

C1, C2 = 15 μF, 25 V
C3-C12 = 0.1 uF, 50 V
CR1, CR3-CR6 = 1N914B
CR2 = LED
J1 = connector, 20-pin
J2 = connector, 4-pin
J3 = connector, 34-pin
J4 = connector, right angle, 10-pin
J5 = connector, phone jack, RJ11C
LK1 = connector, double-row 8-position
LK2 = connector, double-row, 4-position
LK3 = connector, double-row, 6-position
LK6 = connector, single-row, 2-position
LSM = modem, 30 LSM, Part No. 490280-1-T
LSM = modem, 120 LSM, Part No. 490280-2-T
PLI = phone line interface, Part No. 490278-T
Q1,Q2 = 2N2222
R1 = 22 MΩ, 1/4W, 5%
R2 = 4.7 kΩ, 1/4W, 5%
R3,R5,R6,R17 = 2.2 kΩ, 1/4W, 5%
R4 = 12 kΩ, 1/4W, 5%
R7,R10 = 100 kΩ, 1/4W, 5%
R8 = 2.2 MΩ, 1/4W, 5%
R9,R16 = 47 kΩ, 1/4W, 5%
R11 = 8.2 kΩ, 1/4W, 5%
R12 = 430 kΩ, 1/4W, 5%
R13 = 91 kΩ, 1/4W, 5%
R14 = 1 kΩ, 1/4W, 5%
R15 = 470Ω, 1/4W, 5%
R18,R19 = 10 kΩ, 1/4W, 5%
U1, U3 = CD40109BE
U2 = CD4076BE
U4 = CDP1874CE
U5,U6 = CDP1875CE
U7 = CD22859CE
U8 = CD4585BE
U9 = CDP1867CE
U10 = CA3240AE
U11,U22 = CD4050BE
U12 = CD4069UBE
U13,U14 = CD40107BE
U15 = CD4060BE
U16 = CDP1854ACE
U17 = CD4013BE
U18 = CDP1853CE
U19 = CD4071BE
U20,U21 = CDP1857CE
U23 = CD4081BE
U24 = LM140LAH-12, voltage regulator, 12 V
XU16 = 40-pin socket
Y1 = crystal 2.4576 MHz

Advance Data

CDP18S653V3, CDP18S653V4

RCA Microboard CMOS Direct-Connect Auto MODEMS (CCITT Compatible)

The CMOS Direct-Connect Auto MODEMS CDP-18S653V3 and CDP18S653V4 are members of a new family of Microboards designed to add data communications capabilities over the switched dial-up network (DDD) to the RCA Microboard Computer line.

These Microboards provide an interface that enables any Microboard computer system to send data to or receive data from a remote location over the phone lines. The Microboard system can be fully automated from dialing, connect, and data transfer to disconnect. Operation can be simply initiated by a prompt command from the users application program.

The CDP18S653 contains two modem modules: (1) an LSI CMOS frequency-shift-keying (FSK) phase-coherent modem with all digital filtering (LSM), and (2) a direct-connect phone-line interface (PLI). Connected to the modem is the CMOS digital logic required to control and monitor fully auto-connect and auto-dial operation. An on-board UART, which can be run in interrupt mode, sends digital data to the LSM modem or receives digital data from it.

Typically, the CDP18S653 in conjunction with the Microboard Computer CDP18S602, forms a compact, 2-board communications system because the CDP18S602 also has an on-board UART for user terminal interaction and sufficient memory for a wide variety of applications. Other Microboards can be added for additional I/O and/or memory capacity.

Microboards in the CDP18S653 family are available for use at 300 bits per second (CCITT V.21 compatible) for full-duplex operation, type CDP18S653V3, and at 1200 bits per second (CCITT V.23 compatible) for half-duplex operation, type CDP18S653V4. Both Microboards feature auto answer and auto originate, and dial-tone and busy-tone detection.

Features

- **All CMOS design including CMOS LSI modem**
- **Direct connect to phone line**
- **Auto Answer**
- **Auto Originate**
- **Manual Answer**
- **Manual Originate**
- **Self Test**
- **Dual-Tone-Multi-Frequency (DTMF) Dialing or Pulse-Dialing options**
- **Dial-tone detection for optimum speed and reliable tandem dialing**
- **Busy-tone detection for repeat dialing**
- **OFF-HOOK LED indicator**
- **Users link options for abort timers, disconnect and carrier detect**
- **Low-power-static CMOS design assures minimal power supply and cooling requirements**
- **Operating temperature range: -40° C to +85° C**
- **High noise immunity**
- **Small board size: 4.5 x 7.5 inches**
- **Member of extensive Microboard family**
- **Expandable by use of RCA Microboard Universal Backplane**
- **CDP18S653 options:**
  Type CDP18S653V3 - 300 bps for full-duplex operation. CCITT V.21 compatible
  Type CDP18S653V4 - 1200 bps for half-duplex operation. CCITT V.23 compatible

CDP18S653V3, CDP18S653V4

SPECIFICATIONS

Operating Modes:

Auto Answer: When enabled, automatically answers call at end of first ring. Programmble to answer at two or more rings.

Manual Answer: Trailing edge of manually generated input pulse from user option digital interface causes the modem to answer without incoming ring. Used when voice contact is established before entering the data mode.

Manual Originate: Manually generated input pulse from user option digital interface causes connection to line. Used in systems with external telephone set after number is dialed.

Auto Dialing: Allows DTMF (Dual-Tone Multi-Frequency) dialing and pulse dialing.

Line Busy: Digital control input sets PLI (Phone Line Interface) OFF-HOOK but opens audio path to or from telephone line. Used to prevent incoming calls during test or out-of-service modes.

Timing:

Coupler-Cut-Through ($\overline{\text{CCT}}$):

Audio path to or from telephone line connected 2.7 seconds ± 20% after initial line connection.

Abort Timer Options:

Long - 18 seconds ± 20%
Short - 10 seconds ± 20%
No disconnect.
PLI will disconnect if modem carrier digital input is off.

Loss of Carrier Disconnect:

Enabled - 0.5 second ± 20%
Disabled - No disconnect.
PLI will disconnect if modem carrier is lost.
Option independent of Abort Timer.

Operating and Mechanical Characteristics:

Operating Temperature Range:

-40°C to +85°C

Power Requirements:

On-board voltage regulator has preprinted links to accept +15 volts for the two modules operated at +12 volts

OFF-HOOK Current:
24.5 mA at +12 volts (typical) 38 mA at +12 volts (maximum)

ON-HOOK Current:
29 mA at +12 volts (maximum)

Current for Remaining Logic: 5 mA at +5 volts (typical)

Note: Voltage regulator can be bypassed by links so that CDP18S653 Microboard is operated directly from +5 volts and +12 volts.

Dimensions:

4.5 inches x 7.5 inches (114.3 x 190.5 mm) Maximum component height (phone jack) 5/8 inch (15.9 mm)

Connectors:

System Interface: Edge fingers, 44 pins on 0.156-inch centers

User Option Interface (J4): Right-angle header 10 pin

Telephone Interface (J5): USOC* RJ11C

*AT&T Universal Service Ordering Code Number

PLI Interface Characteristics:

Telephone Interface:

2-wire, direct connect to telephone network by means of voice jack RJ11C using line cord with modular plug.

Impedance:

ON-HOOK DC: > 20 megohms measured with - or +200 volts dc from tip or ring to ground

ON-HOOK AC: < 40 kilohms measured between tip and ring

OFF-HOOK DC: 200 ohms measured between tip and ring

OFF-HOOK AC: 600 ohms measured between tip and ring 2.7 seconds after OFF-HOOK with 600 ohms external impedance from modem

Insertion Loss:

2 dB difference between signal level measured at modem line and telephone line both terminated with 600 ohms.

Isolation:

1000 volts RMS between telephone line and power or modem interface.

Surge Protection:

1500-volt peak pulses with 10-microsecond rise time and 160-microsecond delay time.

Loop Current Distortion:

-50 dB from 200 Hz to 4000 Hz with 20 to 100 milliamperes of loop current.

Ring Detector:

Signal-frequency range: 16 to 68 Hz.
Signal-level range: 40 to 150 volts RMS

ON Delay:

192 milliseconds ± 20%

OFF Delay:

80 milliseconds ± 20%

CDP18S653V3, CDP18S653V4

LSM Modem Characteristics

Item	CDP18S653V3	CDP18S653V4
LSM Modem Part No.	V.21	V.23
Format	Serial, binary asynchronous	
Modulation	Frequency shift keying (FSK), phase coherent	
Data Rate (bps)	0 to 300	0 to 1200
Analog Interface	2-Wire, 600-ohm	2-Wire, 600-ohm
Operating Modes	Originate (Channel 1) Answer (Channel 2) Self test	Transmit/Receive Self test
Communication Mode	Full or half duplex	Half duplex, 2-wire
CCITT Compatibility	V.21	V.23 (See Note 1)
Delay Equalizer	Not applicable	Fixed statistical equalizer
Transmit Frequencies (Hz)	Originate (Channel 1): Mark: 980 Space: 1180	Mark: 1300 Space: 2100
	Answer (Channel 2): Mark: 1650 Space: 1850	
Transmitter Tolerance (%)	±0.2	±0.2
Receive Frequencies (Hz)	Originate (Channel 1): Mark: 1650 Space: 1850	Mark: 1300 Space: 2100
	Answer (Channel 2): Mark: 980 Space: 1180	
Transmit Level (dBm)	0 to 15 Adjustable by external resistor	
Receive Level (dBm)	0 to 45	0 to 45
Carrier Detect Level (dBm)	OFF with noise levels from 0 to -60	ON with signal level range of 0 to -45
	ON with signal level range of 0 to -45	

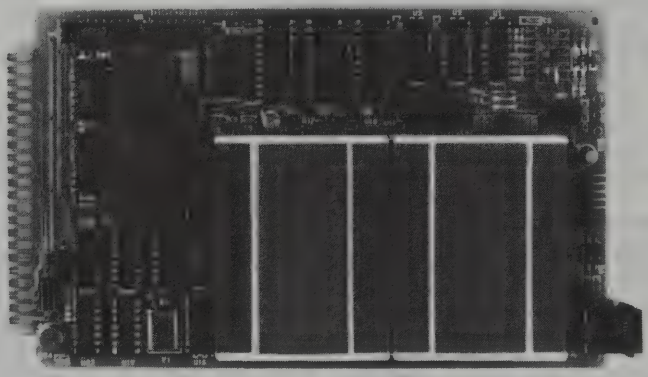
Note 1: Compatible with CCITT V.23 without backward channel or 600 baud (1300/1700 Hz) mode.

CDP18S653V3, CDP18S653V4

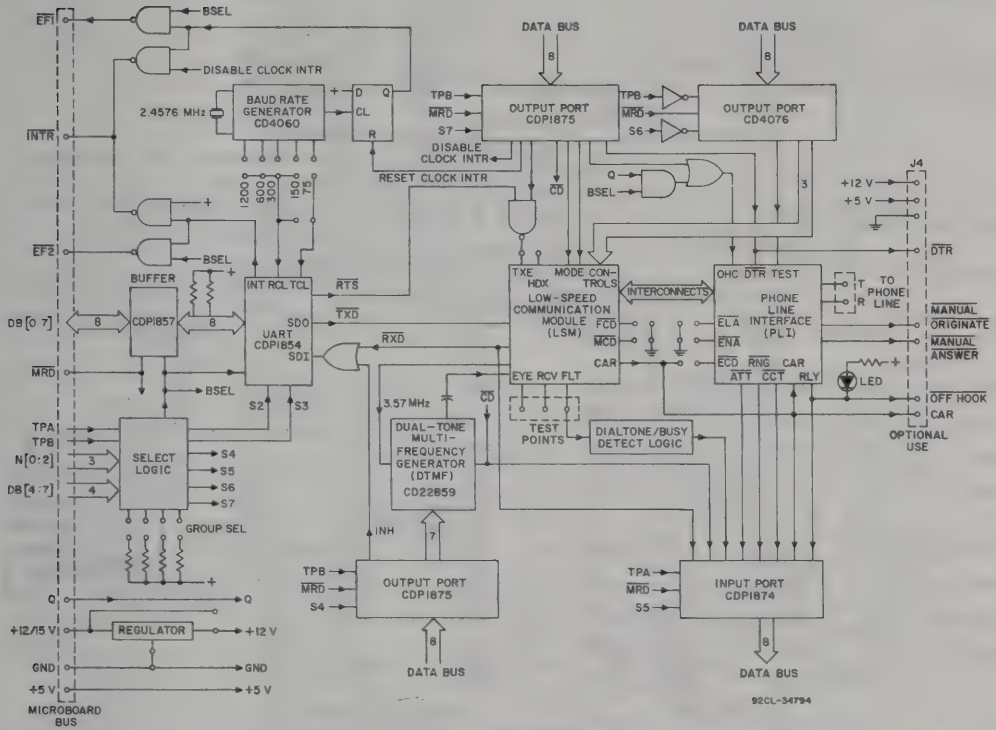
LSM Modem Characteristics (Cont'd)

Item	CDP18S653V3	CDP18S653V4
Carrier Detect Timing (ms ± 30%)	Normal Mode: (See Note 2) ON: 150 OFF: 50	Normal Mode: ON: 38 OFF: 13
(ms max)	Fast Mode: ON: 9 OFF: 9	Fast Mode: ON: 9 OFF: 9
Receive Data: Jitter (%) Typical	7	7
Bias Distortion %	±5 with degradation of 0.6%/°C from +60 to +85°C, and -0.3%/°C from -10 to -40°C	±5

Note 2: Carrier detect (circuit 109) ON time is shorter than that specified by CCITT V.21 for switched telephone network operation (300-700 milliseconds). External delay must be added to extend ON time. The OFF time does not require delay. For leased line applications, the Fast Mode can be enabled and the OFF time extended by external delay to meet CCITT V.21 specifications, (20-80 milliseconds). The ON time does not require delay.

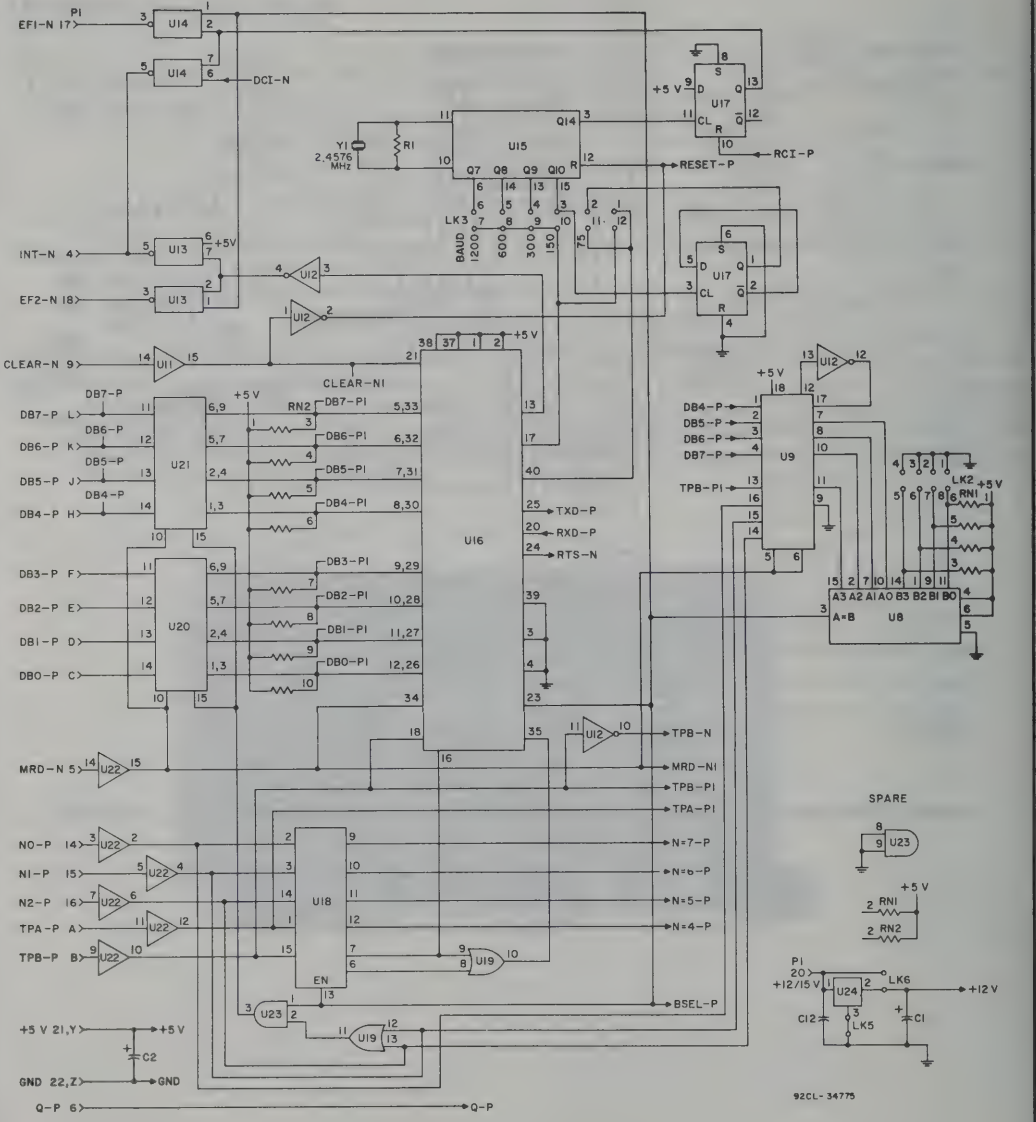


CDP18S653V3, CDP18S653V4



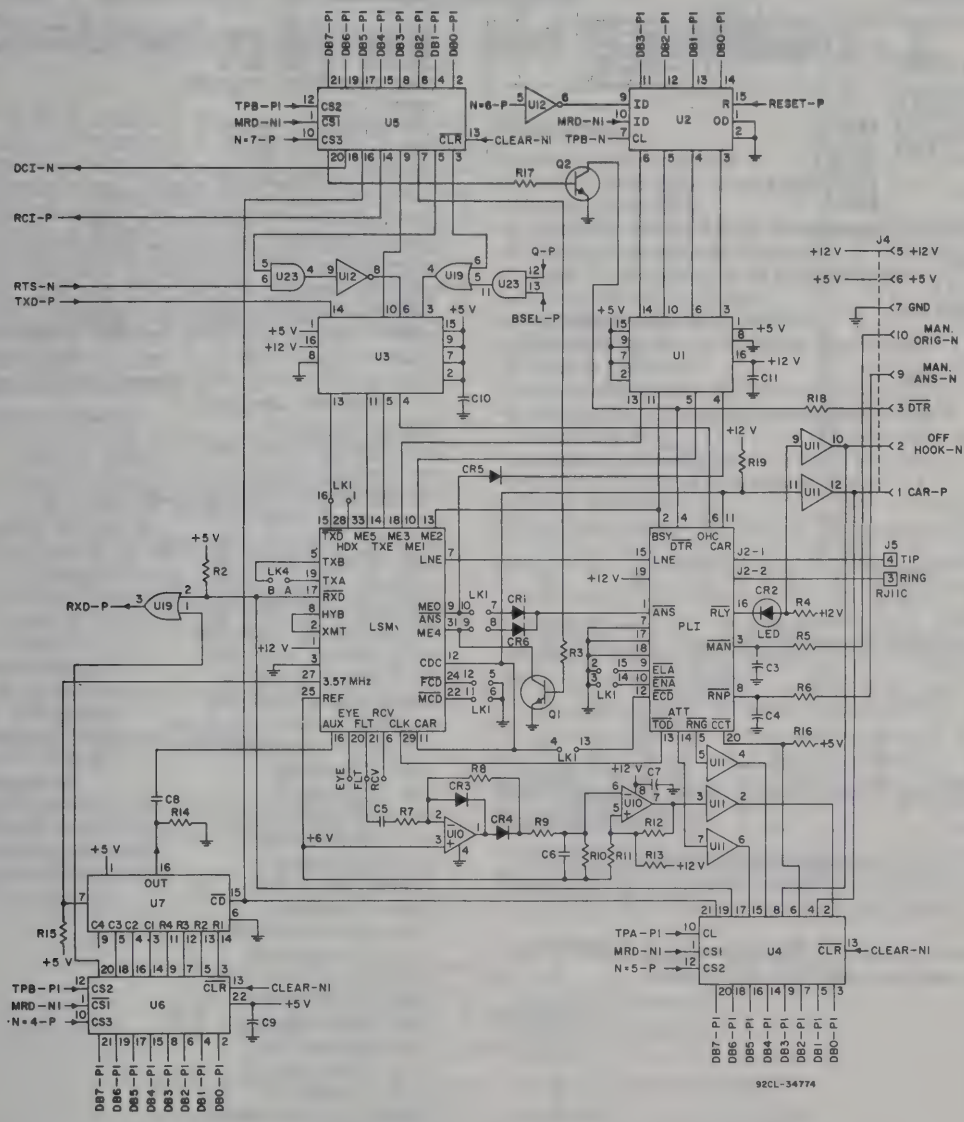
System Block Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653.

CDP18S653V3, CDP18S653V4



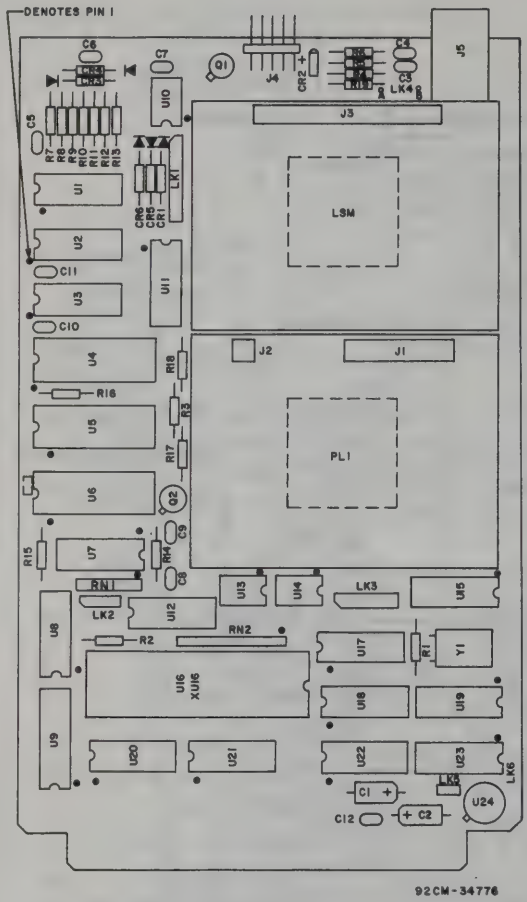
Logic Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653 - Select Logic and UART Interfaces.

CDP18S653V3, CDP18S653V4



Logic Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653 - Phone Line Interface and Modem Modules with Control Logic.

CDP18S653V3, CDP18S653V4



Layout Diagram of RCA Microboard CMOS Direct-Connect Auto MODEM CDP18S653.

PARTS LIST

C1, C2 = 15 μF, 25 V
C3-C12 = 0.1 μF, 50 V
CR1, CR3-CR6 = 1N914B
CR2 = LED
J1 = connector, 20-pin
J2 = connector, 4-pin
J3 = connector, 34-pin
J4 = connector, right angle, 10-pin
J5 = connector, phone jack, RJ11C
LK1 = connector, double-row, 8-position
LK2 = connector, double-row, 4-position
LK3 = connector, double-row, 6-position
LK6 = connector, single-row, 2-position
LSM = modem, V.21 LSM, Part No. 490281-1-T
LSM = modem, V.23 LSM, Part No. 490281-2-T
PLI = CCITT compatible phone line interface, Part No. 490278-1-T
Q1,Q2 = 2N2222
R1 = 22 MΩ, 1/4W, 5%
R2 = 4.7 kΩ, 1/4W, 5%
R3,R5,R6,R17 = 2.2 kΩ, 1/4W, 5%
R4 = 12 kΩ, 1/4W, 5%
R7,R10 = 100 kΩ, 1/4W, 5%
R8 = 2.2 MΩ, 1/4W, 5%
R9,R16 = 47 kΩ, 1/4W, 5%
R11 = 8.2 kΩ, 1/4W, 5%
R12 = 430 kΩ, 1/4W, 5%
R13 = 91 kΩ, 1/4W, 5%
R14 = 1 kΩ, 1/4W, 5%
R15 = 470 Ω, 1/4W, 5%
R18,R19 = 10 kΩ, 1/4W, 5%
U1, U3 = CD40109BE
U2 = CD4076BE
U4 = CDP1874CE
U5,U6 = CDP1875CE
U7 = CD22859CE
U8 = CD4585BE
U9 = CDP1867CE
U10 = CA3240AE
U11,U22 = CD4050BE
U12 = CD4069UBE
U13,U14 = CD40107BE
U15 = CD4060BE
U16 = CDP1854ACE
U17 = CD4013BE
U18 = CDP1853CE
U19 = CD4071BE
U20,U21 = CDP1857CE
U23 = CD4081BE
U24 = LM140LAH-12, voltage regulator, 12 V
XU16 = 40-pin socket
Y1 = crystal 2.4576 MHz

CDP18S660

RCA COSMAC Microboard Combination Memory and I/O Module

The RCA COSMAC Microboard Memory and I/O Module CDP18S660 is a versatile expansion module combining RAM, ROM, and I/O lines. It contains two kilobytes of static CMOS RAM (4 MWS5114's), four on-board sockets for read-only memory (up to 8 kilobytes of EPROM or mask-programmable ROM), two CMOS programmable interfaces (CDP1851's), plus address latches and decoders and I/O latches and decoders. Address and data lines are buffered to minimize loading of the Microboard bus interface.

Specifications

Memory Capacity
On-board RAM: 2 kilobytes (4 CMOS static RAM's, 1024 x 4, MWS5114)
On-board ROM/EPROM: 4 sockets for up to 8 kilobytes (CDP1834, 2708, 2758, 2716)

Memory Address Map
On-board RAM: Any two 1-kilobyte blocks within any even 4-kilobyte block
On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block

I/O Capacity
40 parallel lines programmable as input, output, or bidirectional

Operating Temperature Range
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
With CMOS ROM's: +5 V at 8 mA, typical operating

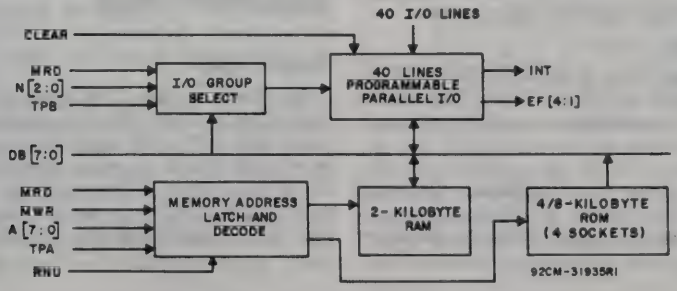
Features

- Low-power static CMOS
- Operable from single 5-volt supply
- High noise immunity
- Compatible with COSMAC Development Systems
- 2 kilobytes of read-write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- 40 programmable I/O lines
- 44-pin system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Small board size: 4.5 x 7.5 inches
- RAM and ROM independently assignable within memory space
- Assignable I/O addresses
- Member of extensive Microboard family
- Simple system interface
- Temperature range: 0 °C to 70 °C

Connectors
System Interface: Edge fingers, 44 pins on 0.156-inch centers
I/O: Edge fingers, 50 pins on 0.100-inch centers

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660. For further information on



Block diagram of RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660.

CDP18S660

these signals, refer to the data sheet for the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

DB7 through DB0

Eight bidirectional data bus lines. Taken directly from the Microboard Universal Backplane to the CDP1851 I/O devices, but buffered from the ROM and RAM memories by CDP1856's, these lines are used to transfer data between memory, CPU, and I/O devices.

A7 through A0

Eight memory address lines on which the high and low address bytes are multiplexed. The high-address byte is latched at the TPA trailing edge and used by the on-board decoders to select the appropriate block of memory.

TPA, TPB

Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

$\overline{\text{MWR}}$

A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$

A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. $\overline{\text{MRD}}$ must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of $\overline{\text{MWR}}$ must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while $\overline{\text{MRD}}$ is false before $\overline{\text{MWR}}$ appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless $\overline{\text{MRD}}$ is properly used to condition data output.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$, $\overline{\text{EF4}}$

Four external flags taken to the CPU by way of the Microboard Universal Backplane. These flags can be tested in software by conditional branch instructions.

N0, N1, N2

Taken directly from the Microboard Universal Backplane, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from the I/O to memory; when low, from memory to I/O.

$\overline{\text{INT}}$

Connected to the Microboard Universal Backplane via optional links and driven by transmission gates, $\overline{\text{INT}}$ originates in the CDP1851 I/O devices. Interrupt causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{\text{INT}}$ results in a completion of execution of the current instruction followed by an S3 machine state during which designators X and P are stored in CPU register T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as the program counter.

RNU

Run Utility Software. This signal is supplied to force the most significant address bit true. As a result, the program start is at memory location 8000 instead of 0000.

CLEAR

This input signal is used on the RCA COSMAC Microboard Module CDP18S660 to reset the ports on both CDP1851's to the input mode and to reset the status register, A RDY, B RDY, and interrupt enable (disabling interrupts).

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. As an alternative, DIP switches can be readily installed in place of links that may require frequent changing.

RAM Address

The RAM on the CDP18S660 is two kilobytes of static CMOS RAM. The four high-order address bits (A15, A14, A13, A12) are latched and decoded, and a set of eight links is provided so that RAM can be positioned in any even 4-kilobyte block. The next two address bits (A11, A10) are further decoded, and a set of four links is provided to allow RAM to occupy any two

1-kilobyte blocks within the selected 4-kilobyte block. The board is shipped prelinked with RAM occupying 2 kilobytes of contiguous memory from 9000 to 97FF. To alter this configuration, the user should cut connections 6:11 and 3:14 in link LK33 and connections 4:5 and 3:6 in link LK16 and then install jumpers in accordance with Tables I and II.

ROM Address

Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). the CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM devices may be used.

Two types of links are provided to select the desired ROM configuration. The first link type is for accommodating the type of ROM selected. The second link type is for selecting the memory address space to be occupied by ROM.

Links LK24 and LK39 are 10-pin and 8-pin dual-in-line arrangements, respectively, with preprinted links to accommodate the CDP1834 or 2708 ROM's. Table III gives the connections required for each ROM type.

Links LK34 and LK35 are 16-pin dual-in-line arrangements. Link LK34 provides the high-order four address bits decoded so that two links or jumpers place sockets XU22 and XU23 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK35 does the same for sockets XU20 and XU21. Links LK34 and LK35 are prelinked so that ROM occupies 4 kilobytes of contiguous memory from 1000 to 1FFF. To alter the ROM address configuration, the user should cut pin connections 1:16 and 6:11 in links LK34 and LK35 and install jumpers in accordance with Table I.

To avoid having floating inputs to the gates, both links LK34 and LK35 should always have two jumpers. For example, if sockets XU20 and XU21 are unused, LK35 may be jumpered the same as LK34. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK34 and LK35 should be jumpered identically in accordance with Table I. Then, ROM's should be installed in sockets XU23, XU21, XU22, and XU20, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK34 and LK35 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then, socket XU23 is the low 2 kilobytes and socket XU22 is the high 2 kilobytes of the 4-kilobyte block as set in LK34. Similarly, socket XU21 is the low 2 kilobytes and socket XU20 is the high 2 kilobytes of the 4-kilobyte block set in LK35.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with 2-kilobyte ROM type

Table I — 4-Kilobyte Link Connections

4-Kilobyte Address Space	Link LK33, LK34 or LK35 Pin Connections
0000-0FFF	1:16, 5:12
†1000-1FFF	1:16, 6:11
2000-2FFF	1:16, 7:10
3000-3FFF	1:16, 8:9
4000-4FFF	2:15, 5:12
5000-5FFF	2:15, 6:11
6000-6FFF	2:15, 7:10
7000-7FFF	2:15, 8:9
8000-8FFF	3:14, 5:12
‡9000-9FFF	3:14, 6:11
A000-AFFF	3:14, 7:10
B000-BFFF	3:14, 8:9
C000-CFFF	4:13, 5:12
D000-DFFF	4:13, 6:11
E000-EFFF	4:13, 7:10
F000-FFFF	4:13, 8:9

LK33 is associated with the 2-kilobyte RAM
LK34 is associated with ROM sockets XU23 and XU22
LK35 is associated with ROM sockets XU21 and XU20
†Prewired ROM location on LK34 and LK35
‡Prewired RAM location on LK33

Table II — RAM 1-Kilobyte Link Connections (2 required)

1-Kilobyte Address Space	Link LK16 Pin Connections	RAM Locations
X000-X3FF	*4:5	U12, U14
X400-X7FF	*3:6	U13, U15
X800-XBFF	2:7	U12, U14
XC00-XFFF	1:8	U13, U15

X denotes any one 4-kilobyte block (X = 0 to F), as fixed by link LK33
*Prewired links

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with 2-kilobyte ROM type

CDP18S660

Table III — ROM Type Selection Links

Link LK24 Pins	CDP1834*	2708*	2758	2716
1:10	X	OPEN	SHORTED	SHORTED
2:9	X	SHORTED	OPEN	OPEN
3:8	X	OPEN	SHORTED	OPEN
4:7	X	OPEN	OPEN	SHORTED
5:6	X	SHORTED	OPEN	OPEN
Link LK39 Pins				
1:8	OPEN	OPEN	OPEN	SHORTED
2:7	SHORTED	SHORTED	SHORTED	OPEN
3:6	OPEN	OPEN	OPEN	SHORTED
4:5	SHORTED	SHORTED	SHORTED	OPEN

*X = don't care; Links LK24 and LK39 are prewired to accept CDP1834 or 2708.

2716. If all links are set up for the 2-kilobyte ROM's as shown in Table III for LK24 and LK39, and if LK34 and LK35 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU23 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU22, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU23 or socket XU22 while the other is occupied by a 1-kilobyte ROM. Socket XU21 (low 2 kilobytes) and socket XU20 (high 2 kilobytes) may be used in the same manner.

Note: When 2708 ROM's are used, the Microboard Universal Backplane must supply +12 volts on pin P1-20 and −5 volts on pin P1-11.

I/O Operation

Two-Level I/O Addressing Conventions

During the I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

1. The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard module in the system having an I/O function.
2. The group number is divided into two parts, the lower four bits being a one-of-four encoding and the higher four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the six commands left after reserving the 61 and 69. The total of useful I/O addresses is 114.
3. The 69 instruction is reserved for reading the latched output of the 61 instruction. The CDP18S660, however, does not provide this feature.

The use of the two halves of the group number must be independent and exclusive. That is, the high-order bits must be zero when any of the low-order bits is used, and the low-order bits must be zero when the high-order bits are used. Once a group is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by the devices assigned to that group number.

The CDP18S660 encodes the high four bits of the transmitted group number to select both CDP1851 programmable I/O interfaces. Each CDP1851 is assigned its own unique group number by jumpering the pin connections in link LK25 as shown in Table IV. The board is shipped prelinked with group number 10 assigned to U1 and group number 20 assigned to U2.

Table IV — I/O Group Selects

Group Number	LK25 Pin Connections	
	U1	U2
10	*1:16	1:15
20	2:16	*2:15
30	3:16	3:15
40	4:16	4:15
50	5:16	5:15
60	6:16	6:15
70	7:16	7:15
80	8:16	8:15
90	9:16	9:15
A0	10:16	10:15
B0	11:16	11:15
C0	12:16	12:15
D0	13:16	13:15
E0	14:16	14:15

*Prewired links

I/O Interface

The I/O interface consists of 40 lines provided on connector P2. Each CDP1851 programmable I/O interface generates 20 lines: 8 lines for port A, 8 lines for port B, and 4 handshaking lines. These lines may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides a logic ground and +5 volts to be used as a reference.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device (File No. 1056).

As previously described, each CDP1851 is assigned to a unique group number by jumpering the proper pin connections in link LK25 (see Table IV). The CDP1851 designated U1 is prelinked for I/O group 10. The CDP1851 designated U2 is prelinked for I/O group 20. Therefore, in order to enable access, a 61 output instruction with data = 10_{16} or 20_{16} is required before read, write, or control I/O may be performed.

Signals 1A RDY, 1B RDY, 2A RDY, and 2B RDY conditioned by the group select can generate flags EF1 through EF4 by jumpering the appropriate pin connections in link LK11 (see Table V). The board is shipped prelinked so that the selection of U1 conditions 1A RDY and 1B RDY, causing the generation of EF1 and EF2, respectively. Similarly, the selection of U2 conditions 2A RDY and 2B RDY, also causing the generation of EF1 and EF2 respectively.

Interrupts can be generated by signals 1 INTA and 1 INTB by jumpering link LK8. Signals 2 INTA and 2INTB can also be used to generate interrupts by jumpering link LK7. If both links are jumpered, any of the signals 1 INTA, 1 INTB, 2 INTA, or 2 INTB will generate an interrupt.

Once the group select is accomplished, N1 and N2 are used to address the selected CDP1851. The following read and write instructions are used to access data, status, and command registers.

62 - Write to control register
64 - Write to Port A data register (if A is an output)
66 - Write to Port B data register (if B is an output)
6A - Read status register
6C - Read Port A data register (if A is an input)
6E - Read Port B data register (if B is an input)

Using the Ready Lines for Data Synchronization

When the group select for U1 is set, Port 1A and Port 1B RDY lines are presented to the CPU EF1 and EF2 lines as prelinked. When the group select for U2 is set, Port 2A and Port 2B RDY lines are presented to the CPU EF1 and EF2 lines as prelinked. For altering the CPU flag selection, see Table V. Note that there is a logic reversal: when RDY is true, the EF is false. A test for RDY true might use the B1 instruction (34) which would take the branch if RDY were false. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU.

When a port designated as an output port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true) and load the next output byte. When a port is designated as an input port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and reads the input byte. In this case, a dummy read after reset is necessary to raise the first RDY.

Table V — CPU Flag Generation (Link LK11)

CDP1851 Signal Causing Flag Generation	Link LK11 Pin Connection			
	EF1	EF2	EF3	EF4
1A RDY	*8:9	—	6:11	—
1B RDY	—	*7:10	—	5:12
2A RDY	*4:13	—	2:15	—
2B RDY	—	*3:14	—	1:16

*Prewired links

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Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the Interrupt Line for Data Synchronization

If links LK7 and LK8 are jumpered, 1 INTA, 1 INTB, 2 INTA, or 2 INTB generates INT to the CPU. INT is not conditioned by the group select. INT is set by the remote sending device STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table VI summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the appropriate group select and then either testing the RDY lines or reading the status byte. Depending on the group select, the low-order two bits of the status byte are:

bit 0 = 1 INTA or 2 INTA; bit 1 = 1 INTB or 2 INTB.

Bidirectional Mode

In each CDP1851, Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, A RDY and A STB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and B STB becomes A OUTPUT STB. Each of the eight lines AD0-AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that data is gated into AD0-AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode

In each CDP1851, both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individuallymasked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Table VI — READY and INTERRUPT Actions for Input and Output Modes

		Output Port	Input Port
READY	Set by	Loading Data	Reading Data
	Reset by	STB leading edge	STB leading edge
INTERRUPT	Set by	STB trailing edge	STB trailing edge
	Reset by	Loading Data	Reading Data

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Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal	
A	TPA-P	*	1	DMAI-N	
B	TPB-P	*	2	DMAO-N	
C	DB0-P	*	3	RNU-P	*
D	DB1-P	*	4	INT-N	*
E	DB2-P	*	5	MRD-N	*
F	DB3-P	*	6	Q-P	
H	DB4-P	*	7	SC0-P	
J	DB5-P	*	8	SC1-P	
K	DB6-P	*	9	CLEAR-N	*
L	DB7-P	*	10	WAIT-N	
M	A0-P	*	11	−5V/−15 V	*
N	A1-P	*	12	SPARE	
P	A2-P	*	13	CLOCK OUT	
R	A3-P	*	14	N0-P	*
S	A4-P	*	15	N1-P	*
T	A5-P	*	16	N2-P	*
U	A6-P	*	17	EF1-N	*
V	A7-P	*	18	EF2-N	*
W	MWR-N	*	19	EF3-N	*
X	EF4-N	*	20	+12 V/+15 V	*
Y	+5 V	*	21	+5 V	*
Z	GND	*	22	GND	*

*Signals used on RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660

Pin Terminals and Signals for the Microboard I/O Connector (P2)

Pin	Signal	Pin	Signal
1	2A STB-P	2	2A RDY-P
3	2AD1-P	4	2AD0-P
5	2AD2-P	6	GND
7	2AD3-P	8	GND
9	2AD4-P	10	2AD5-P
11	2AD7-P	12	2AD6-P
13	2B7-P	14	2B6-P
15	2B5-P	16	2B RDY-P
17	2B4-P	18	2B STB-P
19	2B3-P	20	2B0-P
21	2B2-P	22	2B1-P
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	1B1-P	30	1B2-P
31	1B0-P	32	1B3-P
33	1B STB-P	34	1B4-P
35	1B RDY-P	36	1B5-P
37	1B6-P	38	GND
39	+5 V	40	1B7-P
41	1AD6-P	42	1AD7-P
43	1AD5-P	44	1AD4-P
45	1AD0-P	46	1AD3-P
47	1A STB-P	48	1AD2-P
49	1A RDY-P	50	1AD1-P

NOTE: The signals on connector P2 come from the two CDP1851 Programmable I/O Interfaces. For electrical characteristics refer to the data sheet for the CDP1851 (File No. 1056).

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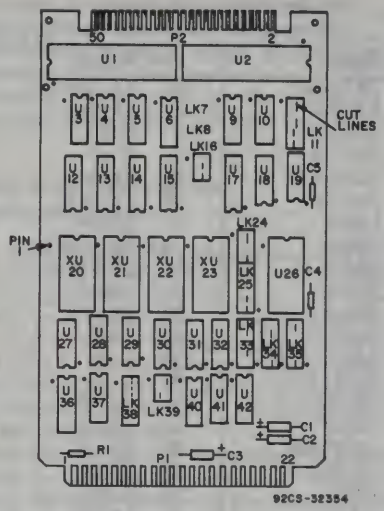

Layout diagram of RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660

Parts List

C1, C2, C3 = 15 μF, 20 V
C4, C5 = 0.1 μF, 50 V
R1 = 22 kΩ, ¼ W
U1, U2 = CDP1851CE
U3 = CD4071BE
U4, U10 = CD4016BE
U5 = CD4011BE
U6, U30 = resistor module 22 kΩ
U9, U19 = CD4001BE
U12-U15 = MWS5114E
U17 = CDP1866CE
U18, U40 = CD4050BE
U26 = CD4514BE
U27, U31 = CDP1856CE
U28, U29 = CD4012BE
U32 = CDP1858CE
U36 = CDP1867CE
U37, U41 = CD4069BE
U42 = CD4073BE
XU1, XU2 = 40-pin socket
XU20-XU23 = 24-pin socket

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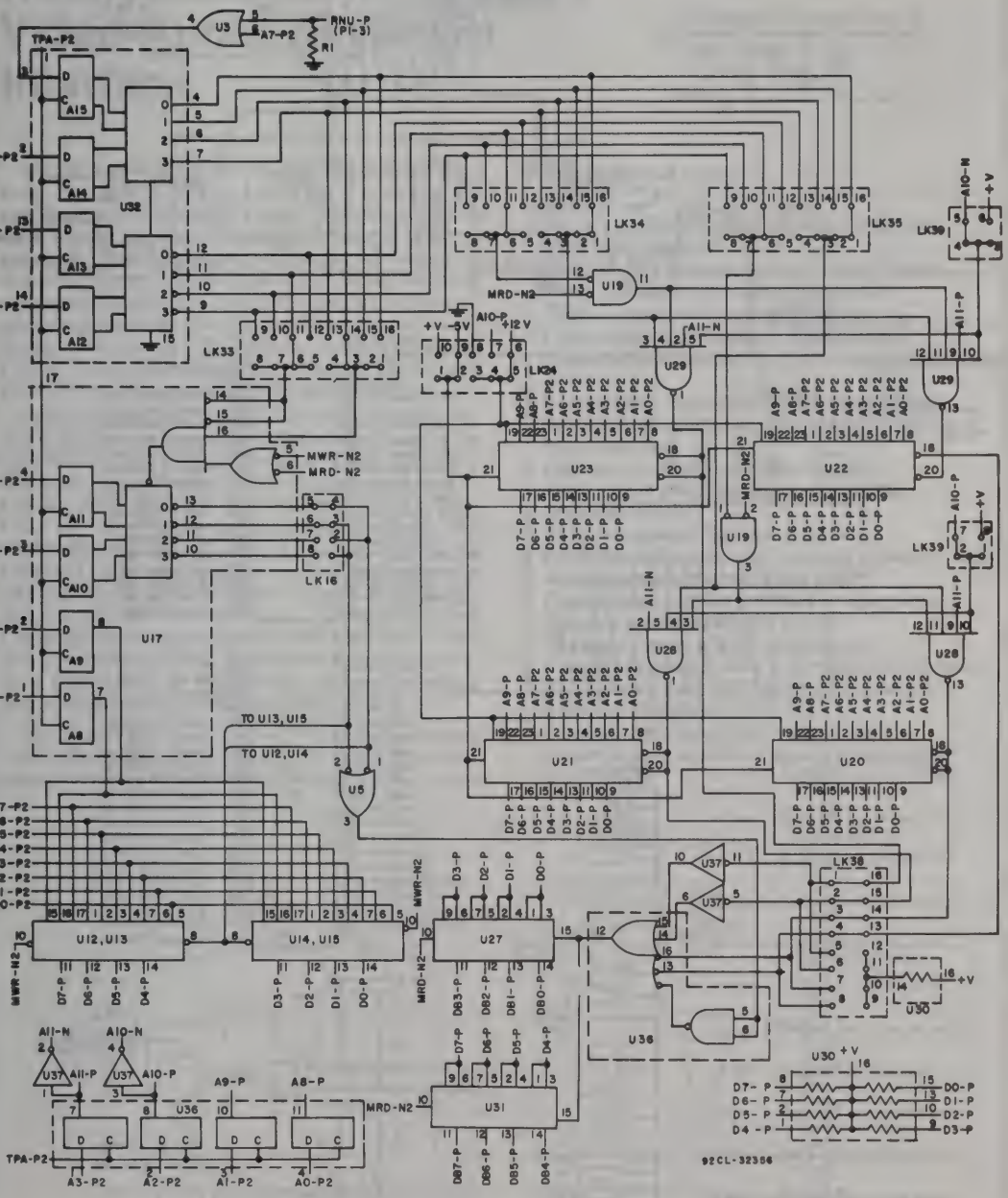

Logic diagram of Microboard Combination Memory and I/O Module CDP18S660 — memory portions.

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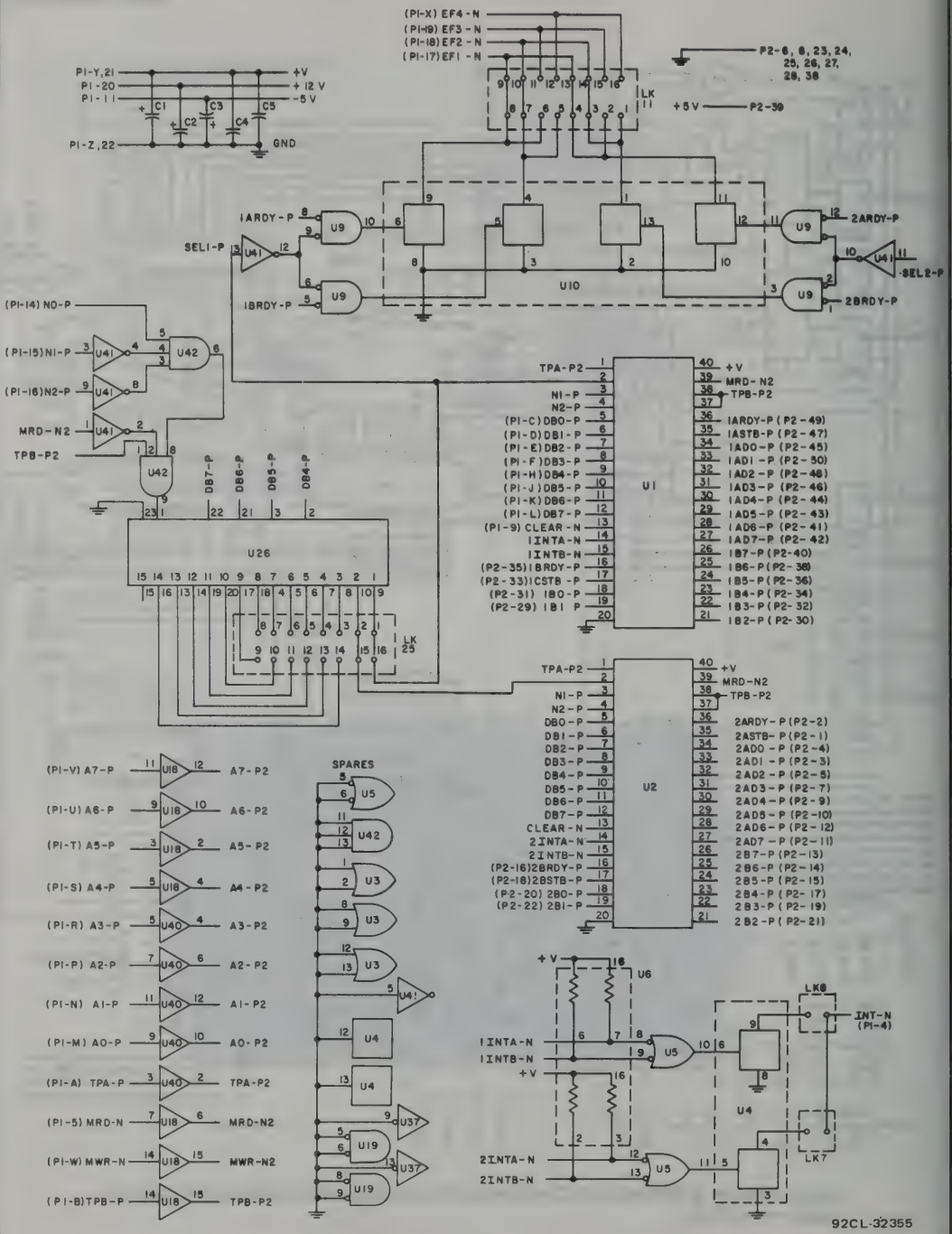

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Logic diagram of Microboard Combination Memory and I/O Module CDP18S660 — I/O portions.

CDP18S661B

RCA COSMAC Microboard Video-Audio-Keyboard Interface

The RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661B is an I/O device for generating and controlling a color or black-and-white video display and for formatting and controlling audio signals. A parallel input port is provided for interfacing with a keyboard or other input device. It has on-board page and character memory and the circuitry required to refresh a cathode-ray tube display. These capabilities are encompassed on a 4.5 by 7.5 inch card containing the CMOS Video Interface System types CDP1869 and CDP1870 as well as memory and logic circuits.

Because of its CMOS design and low current requirements, the power supply and cooling requirements of the CDP18S661A are minimal. It operates from a single 5-volt power supply. It has excellent noise immunity and, as a result, can be used in severe industrial environments. Like all other RCA Microboard products, the CDP18S661B is expandable by use of the 44-pin COSMAC Universal Backplane and is compatible with all RCA COSMAC Development Systems. It can also be plugged into the five-card chassis of the Microboard Computer Development Systems (MCDS) CDP18S693 or CDP18S694 or of the Microboard Prototyping Systems CDP18S691 or CDP18S692, for easy hardware prototyping and rapid software development.

The CDP18S661B is designed for the U.S. standard color video signal (NTSC) and provides a composite signal containing chrominance information and 11 cycles

Features

- **Uses RCA Video Interface System—CDP1869, CDP1870/CDP1876**
- **Video display 40 characters per line x 24 line or 20 x 12 (double size); software selectable**
- **On-board page and character memory**
- **Character set expandable to 256 characters**
- **Character set can be RAM, ROM, or mixed RAM and ROM**
- **Page memory expandable to two display pages**
- **On-board video buffer can drive multiple CRT's or long video lines**
- **Full color or black-and-white capability**
- **Video output either composite or separate sync/luminance**
- **CPU not required for display refresh**
- **8 programmable colors for character or background**
- **Audio output for tone or white noise**
- **Parallel input port for keyboard or other device**
- **Operable from single 5-volt supply**
- **Low-power static CMOS components**
- **Compatible with COSMAC Development Systems**
- **Expandable by use of COSMAC Microboard Universal Backplane**
- **Graphics and motion; hardware scroll**
- **Firmware support with optional VIS Interpreter CDP18S835**

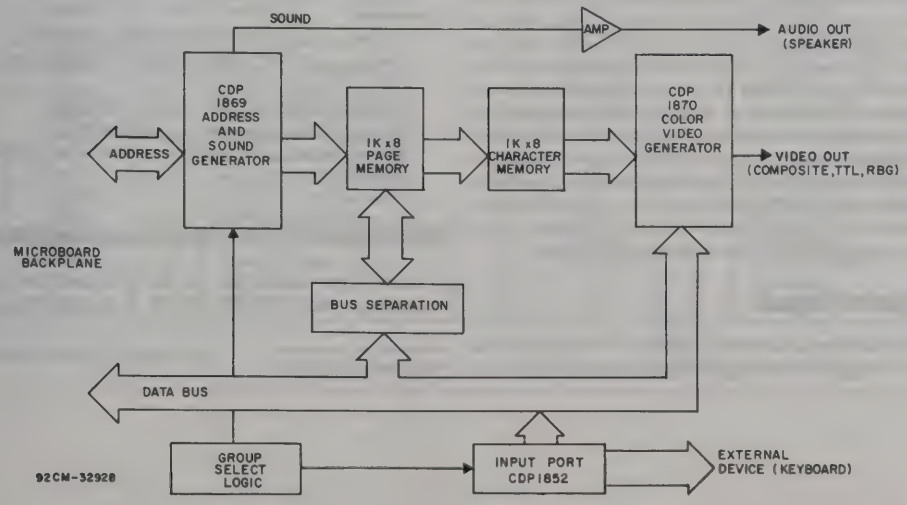

Fig. 1 - Block diagram of RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661B.

CDP18S661B

of the color reference signal. It has a crystal-controlled color oscillator.

Video Output

The video output of the CDP18S661B Microboard Video-Audio-Keyboard Interface provides a composite NTSC signal that can drive a video monitor directly or can be fed to a standard television receiver through an rf modulator. The video signal output is designed for use with a cable or other termination having a 75-ohm impedance. The composite signal contains synchronization, luminance, and chrominance information. The video output terminal is J5. For video overlay applications J3, a 14-pin right-angle connector, provides the control signals required to synchronize the display to an outside source. Connector J3 also provides the TTL level separate-sync video signals for CRT chassis applications requiring a TTL input. The polarities chosen were based on the requirements of popular CRT chassis currently available.

The CDP18S661B is capable of displaying 960 characters of data in a 24-line format having 40 characters per line. It is also capable of a 12-line by 20-character-per-line format thereby providing half the resolution at twice the character height and width.

Audio Output

The audio output (terminal J4) of the CDP18S661B is a software-controlled tone or white-noise signal that can be programmed for frequency, amplitude, and duration. The technical data booklet for the Video Interface System CDP1869, CDP1870, and CDP1876 (File No. 1197) describes how the CDP1869 Address and Sound Generator can be programmed to provide these controls. The frequency range available covers eight octaves. Within each of eight sub-ranges, the input frequency can be divided to produce up to 128 different frequencies. The amplitude is controlled in 16 levels varying from about zero volts to 78 per cent of the dc supply voltage. The buffered audio signal can drive a small speaker (less than 250 milliwatts) directly. An unbuffered signal output is also provided at pin 14 of J3 for amplification by the user. The amplitude and duration of the white-noise output are controlled in a similar fashion. There are eight input frequency selections for the white-noise generator.

Keyboard Input

The input from a keyboard or other control device is carried through a 20-pin right-angle connector J2 to the CDP1852 parallel input port. Link connections are available to support an external CDP1871 Keyboard Encoder or to connect a data available line directly to a CPU flag. The keyboard interface can plug directly into ASCII Keyboards VP601 and VP611.

Specifications

Memory Capacity
- Page memory: 1 kilobyte (two 1K x 4 RAM's) expandable to 2 kilobytes
- Character memory: 1 kilobyte (two 1K x 4 RAM's) expandable to 2 kilobytes; optional 1- or 2-kilobyte ROM or EPROM for up to 256 characters

Memory Address Map*
- Page memory: F800 through FBFF (1-kilobyte RAM)
  FC00 through FFFF (optional 1-kilobyte RAM)
- Character memory: F400 through F7FF

I/O Addressing*
- Two-level group select: 80 through F0 , link selectable
- VIS control: OUT 3 through OUT 7 (63-67)
- Read input port: IN 3 (6B)

Operating Temperature Range
- −40 to +85°C

Dimensions
- 4.5 inches x 7.5 inches (114.3 x 190.5 mm)
- Board pitch: 0.5 inch (12.7 mm) minimum

Power Requirements
- +5 V at 125 mA, typical; 160 mA maximum without optional memory devices

Connectors
- Keyboard connector: 20-pin right angle (J2)
- Overlay and TTL drive interface: 14-pin right angle (J2)
- Buffered audio output: solder pads (J4)
- Composite video output: solder pads (J5)
- System interface: edge fingers, 44 pins on 0.156-inch centers (P1)

Microboard Bus Interface Signals

Table I provides a list of the pins and the signals available at the RCA COSMAC Universal Backplane

*Hexadecimal notation.

CDP18S661B

Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661B; these signals are described below. For further information on the Microboard bus interface signals, refer to the technical data sheet for the CDP1802 (File No. 1023) or the CDP1802A (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor** MPM-201.

DB0 through DB7

Eight bidirectional data bus lines. Taken directly from the Microboard Universal Backplane to the CDP1852 I/O device, but buffered from the RAM memories by CDP1856's, these lines are used to transfer data between memory, CPU, and I/O devices.

A0 through A7

Eight memory address lines on which the high and low address bytes are multiplexed. These lines go directly to the CDP1869 address and sound generator where the high address byte is latched at the TPA trailing edge and used by the decoders to select the appropriate page or character memory.

TPA, TPB

Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used by the CDP1869 to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus in the CDP1870.

$\overline{\text{MWR}}$

A WRITE command from the CPU to the memories. The CDP1869 gates $\overline{\text{MWR}}$ with the high-order address bits and produces page and character memory WRITE signals ($\overline{\text{PMWR}}$ and $\overline{\text{CMWR}}$).

$\overline{\text{MRD}}$

A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the CDP1869, $\overline{\text{MRD}}$ is used with the N0, N1, and N2 bits to decode separation in the page and character memory devices.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$

Three external flags taken to the CPU by way of the Microboard Universal Backplane. These flags can be tested in software by conditional branch instructions.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output Request
C	DB0-P *	In/Out	Data Bus	3	RNU-P	—	Run Utility
D	DB1-P *	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Control
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Control
M	A0-P *	Out	Multiplexed Address Bus	11	-5 V/-15 V	—	Auxiliary Power
N	A1-P *	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P *	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P *	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P *	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P *	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P *	Out	Multiplexed Address Bus	17	EF1-N *	In	External Flag
V	A7-P *	Out	Multiplexed Address Bus	18	EF2-N *	In	External Flag
W	MWR-N*	Out	Memory Write Pulse	19	EF3-N *	In	External Flag
X	EF4-N	In	External Flag	20	+12 V/+15 V	—	Auxiliary Power
Y	+5 V *	In	+ 5 volts dc	21	+ 5 V *	In	+ 5 volts dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

*Signals used on CDP18S661B.

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They are enabled by the group select logic. $\overline{EF1}$ is connected to $\overline{PREDISPLAY}$ of the CDP1870. The EF1 line is used to inform the CPU that the page and character memory will be inaccessible because of CRT screen refresh. The $\overline{EF2}$ line indicates if the input port has data available from the CPU. The $\overline{EF3}$ line is brought out to J2 for user application. If the VP601 or VP611 Keyboard is attached to J2, this line tells the CPU that a key depression has been detected.

N0, N1, N2

Taken directly from the Microboard Universal Backplane, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. The CDP1869 decodes the N bits and gates data from the address bus into terminal latches for I/O control.

The CDP1869 also decodes $\overline{N=3}$ and passes it to the CDP1870 for latching data from the bus.

$\overline{INT}$

Connected to the Microboard Universal Backplane by link, this line allows the CDP1870 to interrupt the CPU during screen display time.

Interrupt Operation

The CDP18S661B can be linked (LK34, 6:11) to provide to the system CPU an interrupt that is generated by the $\overline{PREDISPLAY}$ signal from the CDP1870. The $\overline{PREDISPLAY}$ signal is true (low) one horizontal line prior to display refresh and goes false (high) at the end of the last line of display refresh.

In addition to linking the interrupt line of the Microboard backplane to the CDP18S661B Microboard, other links allow the interrupt to be generated by the leading or trailing edge of $\overline{PREDISPLAY}$. Also, software control can inhibit or enable this interrupt with a CPU output instruction.

Fig. 2 depicts the four linking configurations for the CPU interrupt line, as controlled by link LK4. Modes 3 and 4 can also be controlled in the following manner.

CPU Instruction	M(R(X))	Action
OUT 2	00	Reset current interrupt; disable the interrupt line.
OUT 2	01	Reset current interrupt; allow subsequent interrupts.

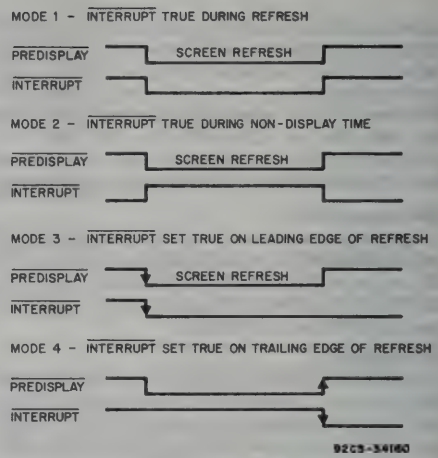


Fig. 2 - Interrupt operation configurations. Link LK4 connections for mode selection are given in Table V.

Installation in Microboard Development or Prototyping Systems

As shipped to the user, the CDP18S661B Microboard Video-Audio-Keyboard Interface is prelinked for operation in the Microboard Universal Backplane. It can, therefore, be plugged directly into a RCA Microboard Computer Development Systems (MCDS) CDP18S693 or CDP18S694, RCA Microboard Prototyping Systems CDP18S691 or CDP18S692, or into any other Microboard Computer System without link changes.

Installation in COSMAC Development Systems

The CDP18S661B may be installed into any of the available memory locations (slots 1 through 7) of the COSMAC Development Systems CDP18S005 and CDP18S007 to facilitate hardware and software development. It is necessary, however, to make link changes in the CDP18S661B and wiring changes on the backplane of the CDS. On the CDP18S661B, the user should cut

connections 7:10 on link LK34 and install jumpers from 8 to 9 of link LK34 and from 5 to 12 of link LK34. In the CDS memory slot location selected for the CDP18S661B, jumper wires should be connected in the backplane as listed in Table II.

Table II - CDS Backplane Jumper Connections

Signal Name	From CPU Slot 12 Pin No.	To Memory Slot Selected Pin No.
N0-P	14	14
N1-P	15	15
EF1-N	17	17
EF2-N	18	18
EF3-N	19	19
TPB-P	B	B
N2-P	16	2
INT-N	4	4

Two-Level I/O Addressing

During the I/O instruction, the CPU presents the low order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

1. The 61 output instruction is reserved to transmit a group number. The output data byte is latched and decoded by any Microboard module in the system having an I/O function.
2. The lower group number is divided into two parts, the lower four bits being a one-of-four encoding and the higher four bits being binary-encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the six commands left after reserving the 61 and 69. The total of useful I/O addresses is 114, and the total of 110 instructions is 228.
3. The 69 instruction is reserved for reading the latched output of the 61 instruction. The CDP18S661B, however, does not provide this feature.

The use of the two halves of the group number must be independent and exclusive. That is, the high-order bits must be zero when any of the low-order bits are used, and the low-order bits must be zero when the high-order bits are used. Once a group is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by the devices assigned to that group number.

The CDP18S661B decodes the high four bits of the transmitted group number as shown in Table III—I/O Group Select Code Connections.

Table III - I/O Group Select Code Connections

I/O Code	Link LK34 Connections
80	None *
90	13:4
A0	14:3
B0	14:3, 13:4
C0	15:2
D0	15:2, 13:4
E0	15:2, 14:3
F0	14:3, 15:2, 13:4

*As shipped.

Character Memory Configurations

As shipped, the character memory is a 1-kilobyte RAM area arranged as 128 characters of 8 bytes each in a 6 by 8 dot matrix space. By means of linking changes, the user can configure the RAM area to provide 64 characters of 16 bytes each on a 6 by 16 dot matrix space.

The 1-kilobyte RAM character memory can be expanded to 2 kilobytes by the installation of appropriate RAM devices in positions U17 and U19. By linking changes this space also can be arranged as 128 characters of 16 lines or 256 characters of 8 lines.

A ROM/EPROM position (U27) can support 64, 128, or 256 characters with or without the RAM area. Thus, the user can have fixed characters or graphics in ROM and variables or graphics in RAM.

The user should refer to Table IV, the Character Memory Table, for the desired character memory configuration and its required linking. The user should also refer to the data sheet (File No. 1197) for the CDP1869, CDP1870, and CDP1876 for detailed operating information on the Video Interface System.

CDP18S661B

Table IV - Character Memory Table

Mode	Characters	Dot Matrix	Memory Type	Link LK15 Connections	Link LK16 Connections	Comments
1	128	6 x 8	RAM	1:16	7:8	As supplied
2	256	6 x 8	RAM	4:13, 8:9, 3:14	All open	RAM's added to U17 and U19
3	128	6 x 16	RAM	7:10	7:8	RAM's added to U17 and U19
4	128	6 x 8	RAM/ROM/ EPROM	5:12	1:14, 5:10, 7:8	2758 type EPROM 1st 64 characters in RAM 2nd 64 in ROM/EPROM
5	128	6 x 8	ROM/EPROM	All open	1:14, 6:9, 7:8	2758 type EPROM On-board RAM deselected
6	256	6 x 8	ROM/EPROM	All open	2:13, 6:9	2316E/2716 type ROM/EPROM
7	128	6 x 16	ROM/EPROM	All open	3:12, 6:9, 7:8	2316E/2716 type ROM/EPROM
8	256	6 x 8	RAM/ROM/ EPROM	4:13	4:11, 1:14	2758 type EPROM 1st 128 characters in RAM 2nd 128 in ROM/EPROM
9	256	6 x 16	RAM/ROM/ EPROM	2:15, 7:10	3:12, 4:11	RAM's added to U17 and U19 2316E/2716 type ROM/EPROM 1st 128 characters in RAM 2nd 128 in ROM/EPROM

Note: Added RAM or ROM/EPROM should have an access time of 350 nanoseconds or faster.

Page Memory Expansion

As shipped, the CDP18S661B Microboard has 1 kilobyte of page memory RAM, enough for a full screen of 40 characters by 24 lines (960 bytes) and 64 scratch bytes for use as character pointers. By linking connections A:B of link LK37 and installing RAM's in positions U29 and U31, the user can expand the page memory to two full screens (1920 bytes). The hardware scroll feature of the CDP1869 and CDP1879 enables this optional page to be scrolled onto the screen. In addition, the optional page can be loaded with an alternate display and exchanged with the primary page on display. It should be noted that the 128 scratch bytes still remain (2 kilobytes minus the 1920 characters). For this double-page feature, the user should merely set the "double-page" bit with a CPU instruction as described in the data sheet (File No. 1197) for the CDP1869, CDP1870, and CDP1876.

Input Port Linking

As supplied to the user, the service request terminal ($\overline{SR}$) of the CDP1852 input port (U14) is tied to $\overline{EF2}$ through terminals 1:12 of link LK8. This line can be broken and tied to an external data available line by cutting the link connection 1:12 of link LK8 and connecting terminals 2:11. These link changes bring the $\overline{EF2}$ line to pin 7 of J2.

The input port signal, STROBE, will enable the port to feed through data when the clock is high ($+V_{DD}$) and latch data when low (V_{SS}). If there is no clock input, the clock line is pulled high by the pull-up resistor, thus allowing the CPU to read the data presented to the CDP1852 data inputs.

Two link positions are provided so that a CDP1871 Keyboard Encoder can be used externally. Link LK8 connection 6:7 brings out $\overline{MRD}$ to pin 5 of J2. Also, $\overline{N=3}$ is brought out to pin 3 of J2 by connecting link 5:8 of link LK8. These two link connections are not preprinted.

Video Drive Applications

The CDP18S661B Microboard Video-Audio-Keyboard Interface when used to drive a cathode-ray tube display can provide a suitable signal in three different forms. A single **composite video signal** containing synchronization, chrominance, and luminance information is available from the video output terminal J5 and can be used to provide a color or black-and-white picture on a video monitor or on a standard television receiver when applied through a user-supplied rf modulator.

For black-and-white monitors requiring a **TTL-level separate-sync video drive**, suitable signals can be derived from pins 10, 11, and 12 of connector J3. Pin 10 provides the luminance information, pin 11 the vertical synchronization (negative polarity), and pin 12 the horizontal synchronization. The polarities available were chosen to be compatible with industry-standard cathode-ray-tube chassis. Fig. 3 gives signal level and polarity information.

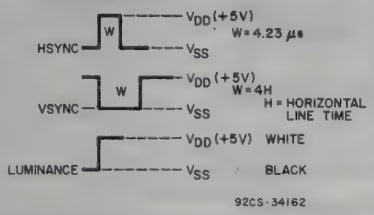


Fig. 3 - Signals available for black-and-white monitors requiring TTL-level, separate-sync video drives.

For color monitors that require **separate red, green, and blue signals** for direct gun control, such signals can be made available by a simple modification. The CDP1870 Color Video Generator in socket U26 (see layout diagram in Fig. 6) should be replaced by a CDP1876 Color Video Generator to provide the signals for this option. When this substitution is made it is also necessary to make some link modifications. On link LK7 the links connecting pins 13:4 and 16:1 should be cut for RBG operation. Then, jumper wires should be connected across pins 15:2 and 14:3 of link LK7. By these changes red, blue, and green drive signals are made available, respectively, at pins 2, 3, and 4 of connector J3. A composite synchronization signal is available at J5 (video out), and TTL-level separate vertical and horizontal signals are available, respectively, at pins 11 and 12.

Video Overlay

The CDP18S661B can be used to overlay text onto an existing video signal. With this technique the user can pass on video line information such as time of day or camera location data in a security system. For overlay operation, the user should cut link LK7 at 8:9 and jumper LK7 at 7:10 and 3:14. These changes allow the user's $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ to synchronize the CDP18S661B with the external video timing.

In Fig. 4, an overlay circuit for **black-and-white characters**, the external $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs are at pins 5 and 6, respectively, of J3. Both inputs are edge-triggered and detect when the input makes the transition from high (V_{DD}) to low (V_{SS}). The luminance signal at pin 2 of J3, when programmed for "white" data, goes high (V_{DD}) at the occurrence of a "dot" during display refresh. This signal can then be used to switch the CD4066 multiplexer and overlay the screen at dot time. The level control permits character brightness adjustment. The voltage applied to the control can be any level within the range of V_{DD} to V_{SS}. The only constraint of this arrangement is that white characters rather than gray-scale characters must be programmed to make sure that the luminance signal is the full voltage swing from V_{DD} to V_{SS}.

Color overlay can be done by modifying the CDP18S661B for RBG operation as described under **Video Drive Applications** and using the circuit shown in Fig. 5. In this circuit, the CD4075 OR gate senses a dot

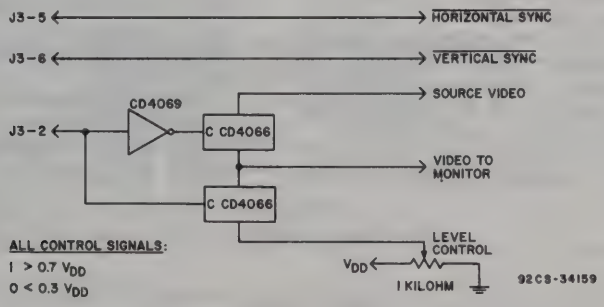


Fig. 4 - Overlay circuit for black-and-white characters.

CDP18S661B

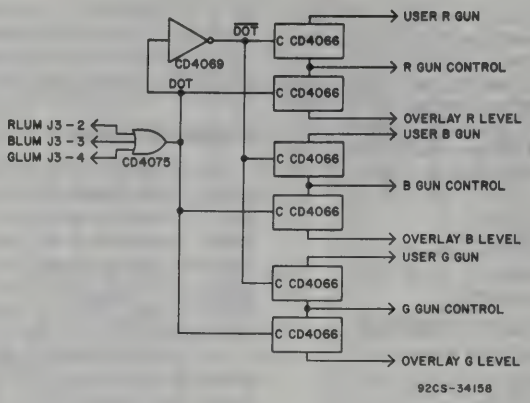


Fig. 5 - Overlay circuit for color characters.

and switches the CD4066 multiplexer away from the external gun control. As in Fig. 4, the voltage level to be provided at the overlay inputs is user defined and should be in the range of V_{DD} to V_{SS}.

VIS Interpreter CDP18S835

The VIS Interpreter, available on diskette CDP18S835 as a user option, is an interpretive language designed to control the CDP1869, CDP1870, and CDP1876 Video Interface System components. The VIS Interpreter is especially supportive of the CDP18S661B Microboard Video-Audio-Keyboard Interface. The interpretive command set provides simple control of text, graphics, and motion on a cathode-ray tube in black and white or in color. Because the Interpreter is open-ended, the user can create his own commands for any purpose. Also, because the source code is supplied with the diskette, unused commands can be deleted from a specific application.

As supplied, the VIS Interpreter is a 3-kilobyte program and requires a minimum of 64 bytes of system RAM. After the user debugs his application, he can put the Interpreter and the program in ROM or EPROM.

Detailed information on the VIS Interpreter is provided in the **User Manual for the VIS Interpreter CDP18S835**, MPM-835. Following is a partial list of the Interpreter routines.

- Write a character to character memory
- Display Interpreter accumulator
- Fill a row in page memory
- Change the color format
- Set screen resolution
- Scroll the screen up or down n lines
- Turn the display off or on
- Move a character in the display
- Move a character bit (dot)
- Test and branch on any of sixteen 1-byte variables
- Test accumulator
- Control tone generator
- Control noise generator
- Handle Interpreter subroutines
- Convert data to ASCII

Table V - List of Links and Their Functions

LK4 Provides for interrupt mode selection	
1:10	Select mode 2, interrupt during non-display
2:9	Select mode 1, interrupt during refresh
*3:8	Select mode 3 or mode 4, edge triggering
*4:7	Select mode 4, trailing edge
5:6	Select mode 3, leading edge
LK7 Provides for optional video control	
*1:16	Connect chrominance (color data) to composite video
2:15	Connect $\overline{\text{RBG}}$ drive option (G control)
3:14	Connect RBG drive option (R control); use luminance for overlay
*4:13	Connect composite sync to composite video
*5:12	Dot clock crystal option
6:11	Not used
7:10	External $\overline{\text{HSYNC}}$ for overlay
*8:9	On-board $\overline{\text{HSYNC}}$
LK8 Provides for input port configuration	
*1:12	Flag for input port $\overline{\text{SERVICE REQUEST}}$
'2:11	Flag for external $\overline{\text{DATA AVAILABLE}}$
3:10	Not used
4:9	J2-7 to EF4 for "BREAK" key
'5:8	$\overline{\text{N=3}}$ for external port select
'6:7	$\overline{\text{MRD}}$ for external port select
LK15 Provides for character memory RAM configuration	
*1:16	Select 1-K RAM, 6 x 8 (mode 1)
"2:15	Select 2-K RAM, 6 x 16 (mode 9)
"3:14	Select 2-K RAM, 6 x 16 (mode 3)
"4:13	Select 2-K RAM, 6 x 8 (mode 2)
5:12	Select 1-K RAM, 6 x 8 (mode 4)
"6:11	Select 2-K RAM, 6 x 16 (mode 9)
"7:10	Select 2-K RAM, 6 x 16 (mode 3)
"8:9	Select 2-K RAM, 6 x 8 (mode 2)
LK16 Provides for character memory ROM/PROM configuration	
1:14	Select 1-K EPROM, 2758 (modes 4, 5, and 8)
2:13	Select 2-K ROM/EPROM, 2316 or 2716 (mode 6)
3:12	Select 2-K ROM/EPROM, 2316 or 2716 (mode 7)
4:11	Select 1-K EPROM, 2758 (mode 8)
5:10	Select 1-K EPROM, 2758 (mode 4)
6:9	Select 1-K EPROM, 2758 (mode 5)
	Select 2-K ROM/EPROM, 2316 or 2716
7:8	Disconnect page color bit for 256 character select

Preprinted links, as shipped.
'Links for supporting use of a CDP1871 Keyboard Encoder.
"Used with optional RAM at U17 and U19.

CDP18S661B

Table V - List of Links and Their Functions (Cont'd)

LK34 Provides for CDS application and group select options
*1:18 PREDISPLAY to EF1-N
2:17 MSB I/O group select
3:16 NSB I/O group select
4:15 LSB I/O group select
5:14 TPA-P from CDS backplane
6:13 INT-N from backplane for all interrupt modes
*7:12 N2-P from Microboard backplane
8:11 N2-P from CDS backplane
9:10 EF4 from J2-7 for "BREAK" key
LK37 Provides for page memory expansion
A:B PMA10 to optional RAM at U29 and U31

*Preprinted links, as shipped.

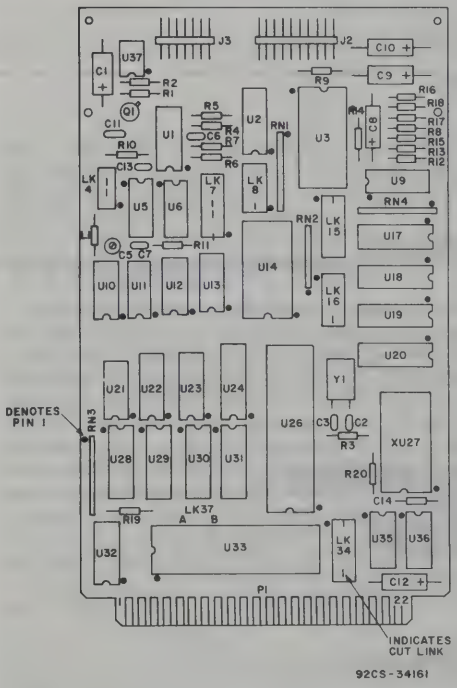


Fig. 6 - Layout diagram of RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661B.

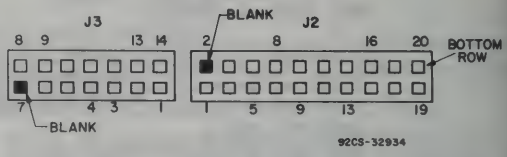


Fig. 7 - Pin location diagram for terminals J2 and J3.

CDP18S661B

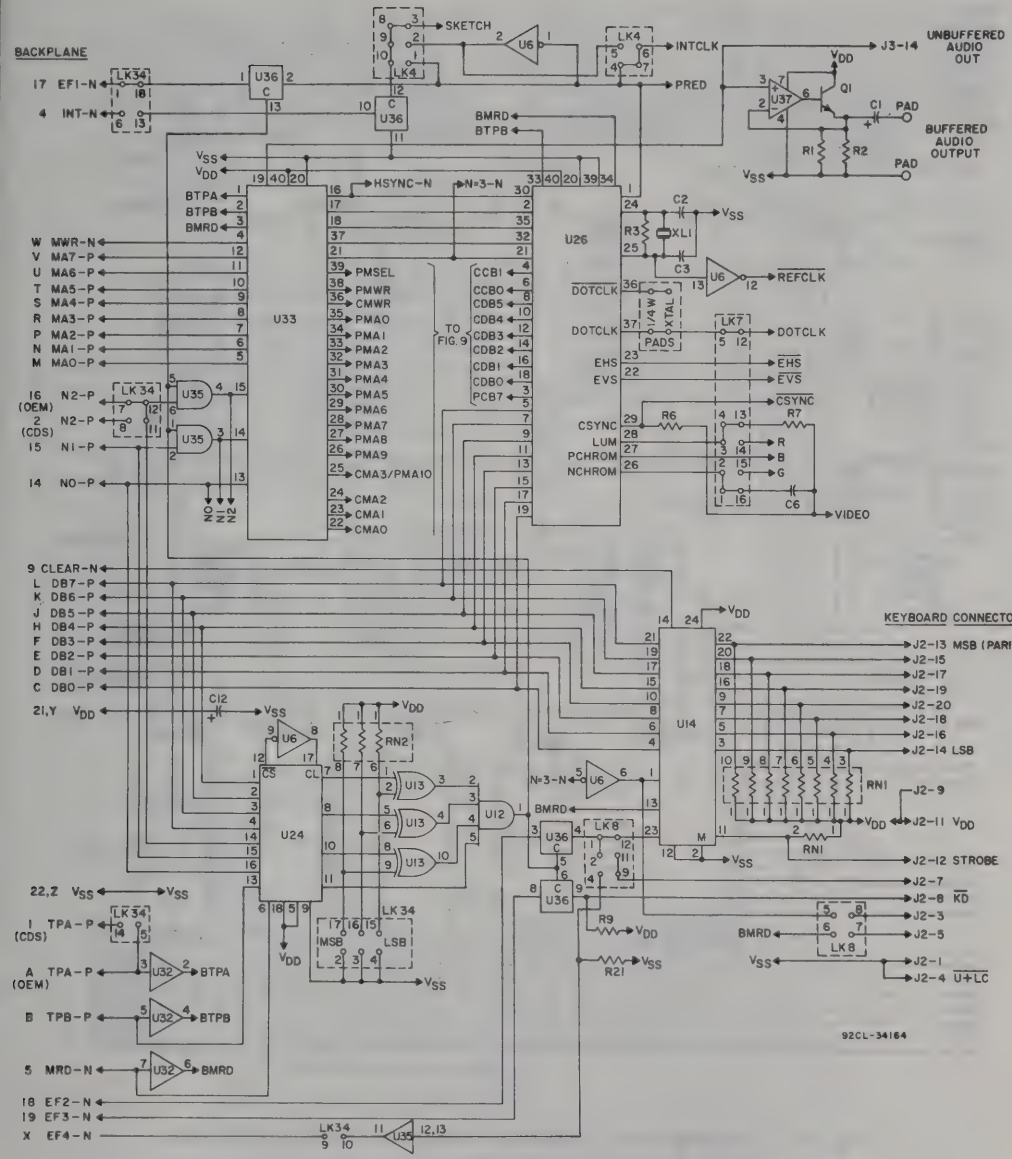


Fig. 8 - Logic diagram of Microboard Video-Audio-Keyboard Interface CDP18S661B-generator and control portions.

CDP18S661B

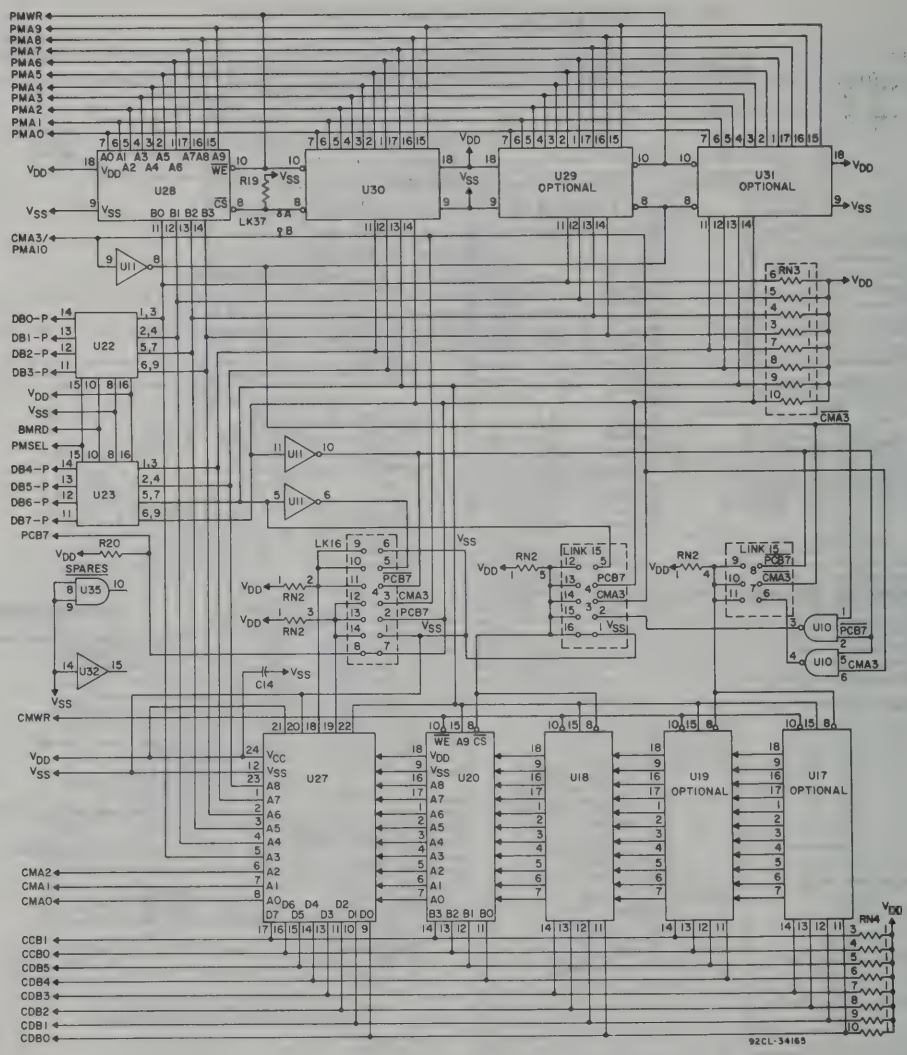


Fig. 9 - Logic diagram of Microboard Video-Audio-Keyboard Interface CDP18S661B-memory portions.

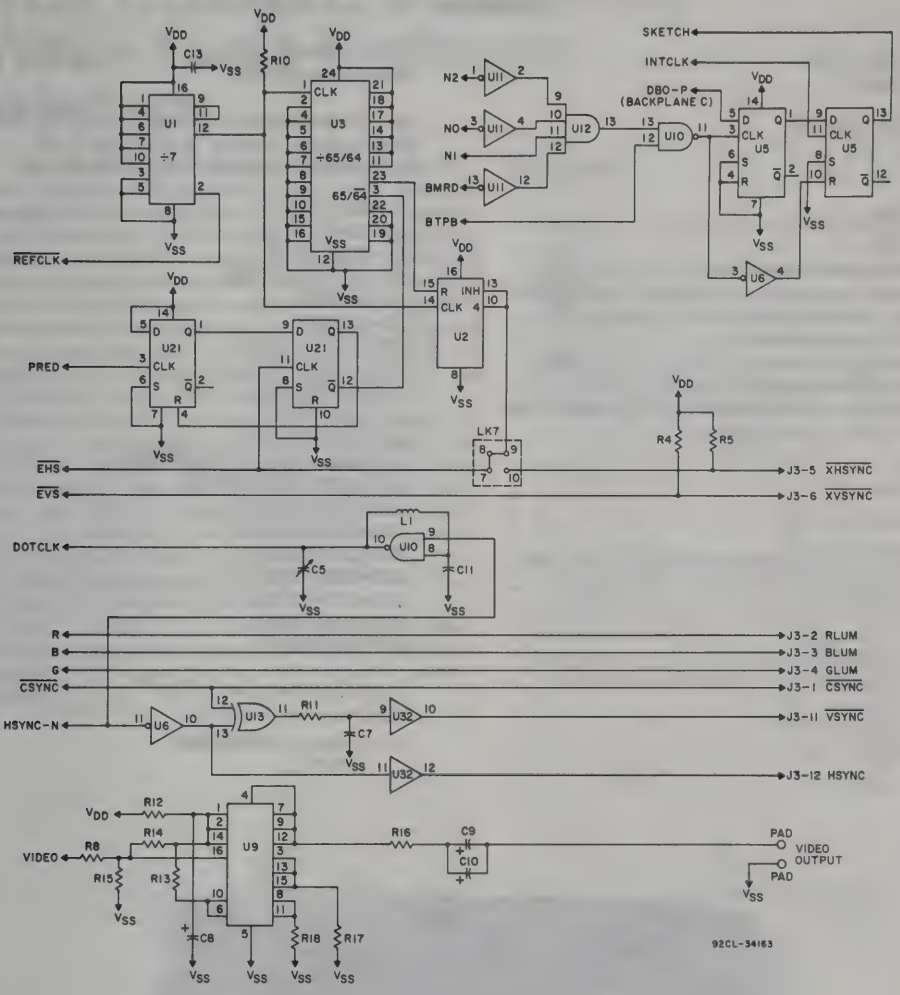


Fig. 10 - Logic diagram of Microboard Video-Audio-Keyboard Interface CDP18S661B-output portion.

CDP18S661B

Parts List

C1, C12=22 μF, 25 V
C2, C11=22 pF
C3=10 pF
C5=variable, 5-25 pF
C6=120 pF, 500 V
C7=0.001 μF, 100 V
C8=47 μF
C9, C10=220 μF, 16 V
C13, C14=0.1 μF

J2=right-angle connector, 20 pin, (mates with connector comprised of housing - AMP 86148-1. contact - AMP 86016-1, keying plug - AMP 87077-1, or equivalent)
J3=right-angle connector, 14 pin, (mates with connector comprised of housing—AMP 1-86148-4, contact - AMP 86016-1, keying plug - AMP 87077-1, or equivalent)

L1=33 μH

Q1=2N2222

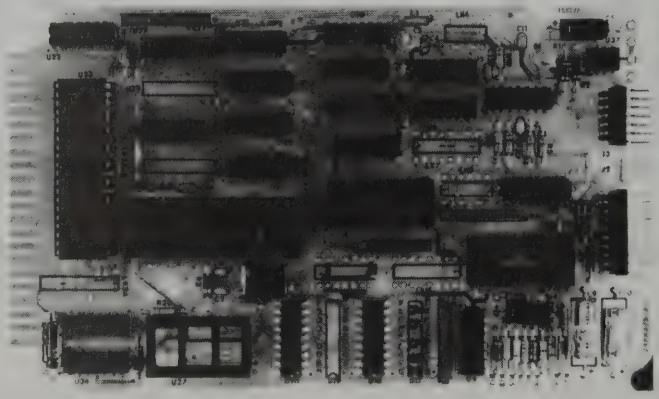
R1, R2=91 ohms, ¼W
R3=22 megohms ¼W
R4, R5, R9, R10, R19, R20, R21=22 kilohms, ¼W
R6=3.9 kilohms, ¼W
R7, R11=1 kilohm, ¼W
R8=5.1 kilohm, ¼W
R12=22 ohms, ¼W
R13=2.7 kilohms, ¼W
R14=6.2 kilohms, ¼W
R15=12 kilohms, ¼W
R16=68 ohms, ¼W
R17=2 kilohms, ¼W
R18=33 ohms, ¼W

RN1, RN3=resistor module, 22 kilohms, 10 pin
RN2=resistor module, 22 kilohms, 8 pin
RN4=resistor module, 10 kilohms, 10 pin

U1=(60-1) 9316
U2=CD4017BE
U3=CD4059AE
U5, U21=CD4013BE
U6=2467887
U9=CA3083
U10=3027714-001
U11=CD4069UBE
U12=CD4082BE
U13=CD4070BE
U14=CDP1852CE
U18, U20, U28, U30=2473352
U22, U23=CDP1856CE
U24=CDP1867CE
U26=CDP1870CE
U32=CD4050BE
U33=CDP1869CE
U35=CD4081BE
U36=CD4016BE
U37=CA3160E

XU26, XU33=socket, 40 pin
XU27=socket, 24 pin

Y1=crystal, 7.15909 MHz



CDP18S661V3

RCA COSMAC Microboard Video-Audio-Keyboard Interface

The RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661V3 is an I/O device for generating and controlling a color or black-and-white video display and for formatting and controlling audio signals. A parallel input port is provided for interfacing with a keyboard or other control device. It has on-board page and character memory and the circuitry required to refresh a cathode-ray tube display. These capabilities are encompassed on a 4.5 by 7.5 inch card containing the CMOS Video Interface System types CDP1869 and CDP1876 as well as memory and logic circuits.

Because of its CMOS design and low current requirements, the power supply and cooling requirements of the CDP18S661 are minimal. It operates from a single 5-volt power supply. It has excellent noise immunity and, as a result, can be used in severe industrial environments. Like all other RCA Microboard products, the CDP18S661 is expandable by use of the 44-pin COSMAC Universal Backplane and is compatible with all RCA COSMAC Development Systems.

The CDP18S661V3 is designed for the European standard color video signal (PAL) and provides a separate RGB signal that can drive a video monitor directly.

Features

- Uses RCA Video Interface System - CDP1869, CDP1876
- Video display 40 characters per line x 24 lines; or 20 x 12 (double size)
- On-board page and character memory
- Up to 128 user-programmable characters, any 6 x 9 figure
- Full color or black and white capability
- Video output either composite or separate sync/luminance
- CPU not required for display refresh
- 8 programmable colors for character or background
- Audio output for tone or white noise
- Parallel input port for keyboard or other device
- 5-volt operation
- Low-power static CMOS components
- Compatible with COSMAC Development Systems
- Expandable by use of COSMAC Microboard Universal Backplane
- Graphics and motion; hardware scroll
- Firmware support with VIS Interpreter CDP18S835

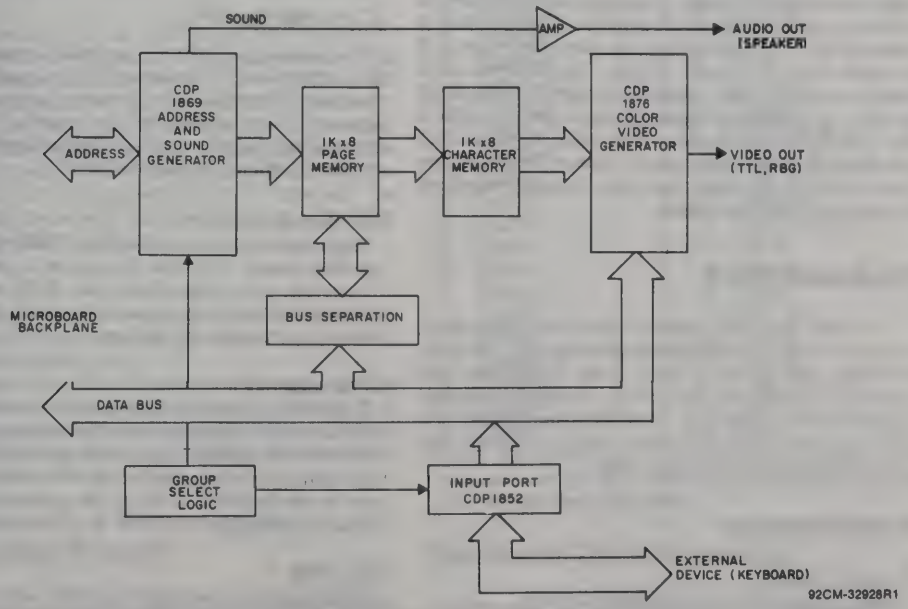


Fig. 1 - Block diagram of RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661.

CDP18S661V3

Video Output

The video output of the CDP18S661V3 Microboard Video-Audio-Keyboard Interface provides an RBG PAL signal that can drive a video monitor directly. For video overlay applications terminal J3, a 14-pin right-angle connector, provides the control signals required to synchronize the display to an outside source. Connector J3 provides the TTL level separate-sync video signals for CRT chassis applications requiring a TTL input. The polarities chosen were based on the requirements of popular CRT chassis currently available.

The CDP18S661V3 is capable of displaying 960 characters of data in a 24-line format having 40 characters per line. It is also capable of a 12-line by 20-character-per-line format thereby providing the same resolution but twice the character height and width.

Audio Output

The audio output (terminal J4) of the CDP18S661V3 is a software-controlled tone or white-noise signal that can be programmed for frequency, amplitude, and duration. The technical data booklet for the Video Interface System CDP1869, CDP1870, CDP1876 (File No. 1197) describes how the CDP1869 Address and Sound Generator can be programmed to provide these controls. The frequency range available covers eight octaves. Within each of the eight sub-ranges, the input frequency can be divided to produce up to 128 different frequencies. The amplitude is controlled in 16 levels varying from about zero volts to 78 per cent of the dc supply voltage. The buffered audio signal can drive a small speaker (less than 250 milliwatts) directly. An unbuffered signal output is also provided at pin 14 of J3 for amplification by the user. The amplitude and duration of the white-noise output are controlled in a similar fashion. There are eight input frequency selections for the white-noise generator.

Keyboard Input

The input from a keyboard or other control device is carried through a 20-pin right-angle connector J2 to the CDP1852 parallel input port. Link connections are available to permit the selection of a clock input of either polarity or to connect a data available line directly to a CPU flag. The keyboard interface can plug directly into ASCII Keyboards VP601 and VP611.

Specifications

Memory Capacity
Page memory: 1 Kilobyte (8 MWS5101's)
Character memory: 1 Kilobyte (8 MWS5101's)

Memory Address Map
Page memory: F800 through FBFF (wraps in FC00 through FFFF)
Character memory: F400 through F7FF

I/O Addressing
Two-level group select: 80 through F0, link selectable
VIS control; OUT 3 through OUT 7 (63 - 67)
Read input port: IN 3 (6B)

Operating Temperature Range
-40°C to 85°C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch: 0.5 inch (12.7 mm) minimum

Power Requirements
Video output only: + 5 V at 10 mA, typical operating
Audio output only: + 5V at 25 mA, maximum

Connectors
Keyboard connector: 20 pin right angle (J2)
Overlay and TTL drive interface: 14 pin right angle (J3)
Buffered audio output: solder pads (J4)
Composite video output: solder pads (J5)
System interface: edge fingers, 44 pins on 0.156-inch centers (P1)

Microboard Bus Interface Signals

(Connector P1)

The following signals are generated or received by the RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661. For further information on these signals, refer to the technical data sheet for the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor** MPM-201.

DB7 through DB0
Eight bidirectional data bus lines. Taken directly from the Microboard Universal Backplane to the CDP1852 I/O device, but buffered from the RAM memories by CDP1856's, these lines are used to transfer data between memory, CPU, and I/O devices.

A7 through A0
Eight memory address lines on which the high and low address bytes are multiplexed. These lines go directly to the CDP1869 address and sound generator where the high-address byte is latched at the TPA trailing edge and used by the decoders to select the appropriate page or character memory.

TPA, TPB
Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used by the

CDP1869 to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus in the CDP1876.

$\overline{MWR}$

A WRITE command from the CPU to the memories. The CDP1869 gates $\overline{MWR}$ with the high-order address bits and produces page and character memory WRITE signals ($\overline{PMWR}$ and $\overline{CMWR}$).

$\overline{MRD}$

A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the CDP1869, $\overline{MRD}$ is used with the N0, N1, and N2 bits to decode the proper I/O instruction. It is also used to direct bus separation in the page and character memory devices.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$

Three external flags taken to the CPU by way of the Microboard Universal Backplane. These flags can be tested in software by conditional branch instructions. They are enabled by the group select logic. $\overline{EF1}$ is connected to $\overline{PREDISPLAY}$ of the CDP1876. This line is used to inform the CPU that the page and character memory will be inaccessible because of CRT screen refresh. The $\overline{EF2}$ line indicates if the input port has data available from the CPU. The $\overline{EF3}$ line is brought out to J2 for user application. If the VP601 or VP611 keyboard is attached to J2, this line tells the CPU that a key depression has been detected.

N0, N1, N2

Taken directly from the Microboard Universal Backplane, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. The CDP1869 decodes the N bits and gates data from the address bus into internal latches for I/O control. The CDP1869 also decodes $\overline{N=3}$ and passes it to the CDP1876 for latching data from the bus.

$\overline{INT}$

Connected to the Microboard Universal Backplane by link, this line allows the CDP1870 to interrupt the CPU during screen display time.

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661.

Installation in a Microboard Prototyping System

As shipped to the user, the CDP18S661 Microboard Video-Audio-Keyboard Interface is prelinked for operation in the Microboard Universal Backplane. It can, therefore, be plugged directly into a RCA Microboard Prototyping System CDP18S691 or CDP18S692 or into any other Microboard Computer System without link changes.

Installation in COSMAC Development System

The CDP18S661 may be installed into any of the available memory locations (slots 1 through 7) of the COSMAC Development Systems CDP18S005 and CDP18S007 to facilitate hardware and software development. It is necessary, however, to make link changes in the CDP18S661 and wiring changes on the backplane of the CDS. On the CDP18S661, the user should cut connections 12:5 on link LK4 and install jumpers from 13 to 4 of link LK4 and from 8 to 9 of link LK4. In the CDS memory slot location selected for the CDP18S661, jumper wires should be connected in the backplane as listed in Table II.

Table I

Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal	
A	TPA-P	*	1	DMAI-N	
B	TPB-P	*	2	DMAO-N	
C	DB0-P	*	3	RNU-P	
D	DB1-P	*	4	INT-N	*
E	DB2-P	*	5	MRD-N	*
F	DB3-P	*	6	Q-P	
H	DB4-P	*	7	SC0-P	
J	DB5-P	*	8	SC1-P	
K	DB6-P	*	9	CLEAR-N	
L	DB7-P	*	10	WAIT-N	
M	A0-P	*	11	-5V/-15 V	
N	A1-P	*	12	SPARE	
P	A2-P	*	13	CLOCK OUT	
R	A3-P	*	14	N0-P	*
S	A4-P	*	15	N1-P	*
T	A5-P	*	16	N2-P	*
U	A6-P	*	17	EF1-N	*
V	A7-P	*	18	EF2-N	*
W	MWR-N	*	19	EF3-N	*
X	EF4-N		20	+12 V/+15 V	
Y	+5 V	*	21	+5 V	*
Z	GND	*	22	GND	*

*Signals used on RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP 18S661.

Two-Level I/O Addressing

During the I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0

CDP18S661V3

Table II - CDS Backplane Jumper Connections

Signal Name	From CPU Slot 12 Pin No.	To Memory Slot Selected Pin No.
N0-P	14	14
N1-P	15	15
EF1-N	17	17
EF2-N	18	18
EF3-N	19	19
TPB-P	B	B
N2-P	16	2
INT-N	4	4

lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

1. The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard module in the system having an I/O function.
2. The lower group number is divided into two parts, the lower four bits being a one-of-four encoding and the higher four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines times the six commands left after reserving the 61 and 69. The total of useful I/O addresses is 114.
3. The 69 instruction is reserved for reading the latched output of the 61 instruction. The CDP18S661, however, does not provide this feature.

The use of the two halves of the group number must be independent and exclusive. That is, the high-order bit must be zero when any of the low-order bits are used, and the low-order bits must be zero when the high-order bits are used. Once a group is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by the devices assigned to that group number.

The CDP18S661 decodes the high four bits of the transmitted group number as shown in Table III - I/O Group Select Code Connections.

Character Memory Font Selection

As supplied to the user, the character memory of the CDP18S661 is arranged as 128 characters with a 6 x 9 dot matrix font for each character where the ninth line is blank. If it is desired to organize character memory as 64 characters with the ninth line not blanked in a 6 x 9 dot matrix font for each character for PAL systems, the user should cut 2:11 and 1:12 of link LK3 and connect 3:10. Refer to the data booklet for the CDP1869, CDP1870, and CDP1876 (File No. 1197) for output instruction information.

Table III - I/O Group Select Code Connections

I/O Code	Link LK4 Connections
80	None *
90	14:3
A0	15:2
B0	14:3; 15:2
C0	16:1
D0	16:1; 14:3
E0	16:1; 15:2
F0	16:1; 14:3; 15:2

*As shipped

Input Port Linking

As supplied to the user, the service request terminal (SR) of the CDP1852 input port (U14) is tied to EF2 through terminals 4:5 of link LK1. This line can be broken and tied to an external data available line by cutting the link connection 4:5 of link LK1 and connecting terminals 3:6. These link changes bring the EF2 line to pin 7 of J2.

The input port signal, as linked, will enable the port to feed through data when the clock is high ($+V_{DD}$) and latch data when low (V_{SS}). If there is no clock input, the clock line is pulled high (feed through) by the pull-up resistor. To change the polarity of the input port clock signal so that the port will latch data when high (V_{DD}), the user should cut connection 8:5 of link LK3 and wire link 9:4.

Two link positions are provided so that a CDP1871 keyboard encoder can be used externally. Link LK1 connection 2:7 brings out MRD to pin 5 of J2. Also, N=3 is brought out to pin 3 of J2 by connecting link 1:8 of link LK1. These two link connections are not preprinted.

Video Drive Applications

The CDP18S661V3 Microboard Video-Audio-Keyboard Interface when used to drive a cathode-ray tube display can provide a suitable signal in three different forms.

For black-and-white monitors requiring a **TTL-level separated-sync video drive,** suitable signals can be derived from pins 10, 11, and 12 of connector J3. Pin 10 provides the luminance information, pin 11 the vertical synchronization (negative polarity), and pin 12 the horizontal synchronization. The polarities available were chosen to be compatible with industry-standard cathode-ray-tube chassis. Fig. 2 gives signal level and polarity information.

The CDP18S661V3 is configured to support color monitors that require **separate red, green, and blue signals** for direct gun control. The red, blue, and green drive signals are available, respectively, at pins 2, 3, and 4 of connector J3. A composite synchronization signal is available at J5 (video out), and TTL-level separate vertical and horizontal signals are available, respectively, at pins 11 and 12.

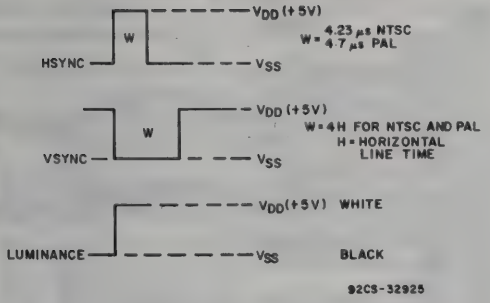


Fig. 2 - Signals available for black-and-white monitors requiring TTL-level, separate-sync video drives.

If it is desired to modify the CDP18S661V3 to support a monitor requiring a composite video input, the following changes should be made.

1. On link LK2, remove connections 2:15, 3:14, and 4:13.
2. On link LK2, install connections 5:12, 7:10, and 8:9.
3. In socket U27, replace the CDP1876CE with a CDP1870CE color video generator.

Video Overlay

Putting a black-and-white picture or text over an existing video display (overlaying) can be accomplished by providing a gated oscillator input to the CDP18S661 along with external horizontal and vertical synchronization signals. Fig. 3 gives a representative circuit that can be provided by the user to supply the gated oscillator signal and the video multiplexing. When an external gated oscillator is used, it is necessary to remove Y2, the dot clock crystal.

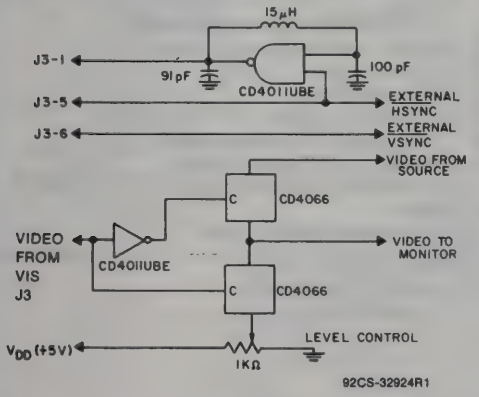


Fig. 3 - Gated oscillator and multiplexing system for black-and-white video overlay.

VIS Interpreter CDP18S835

The VIS Interpreter, a user option available on disk CDP18S835, is an interpretive language that assists the user in the development of programs for screen control. The VIS Interpreter is open ended and allows the user to generate new commands for his application. It is specifically designed to be compatible with the architecture of the RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661.

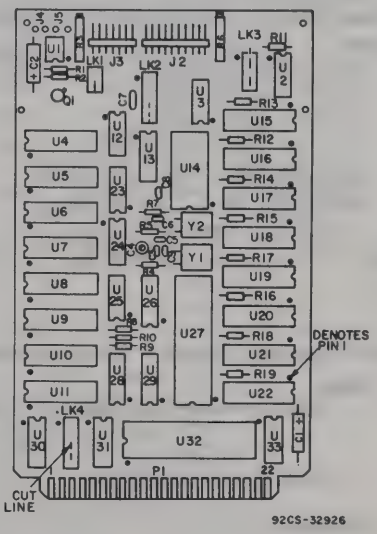


Fig. 4 - Layout diagram of RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661.

CDP18S661V3

Table IV - List of Links and their Functions

LK1 Provides for external CDP1871 keyboard encoder	
1:8	N=3 for input
2:7	MRD-N for chip select
3:6	Flag for DATA AVAILABLE
*4:5	Flag for I/O port SERVICE REQUEST
LK2 Provides for optional video control	
1:16	External dot clock input for overlay
*2:15	Red gun control
*3:14	Blue gun control
*4:13	Green gun control
5:12	PAL chrominance input
6:11	NTSC chrominance input
7:10	Luminance data output
8:9	Composite sync output
LK3 Provides for character formatting and I/O port clock	
*1:12	Blank line nine (PAL)
*2:11	128 characters by 8 lines
3:10	64 characters by 16 lines (9 lines PAL)
4:9	Active low clock
*5:8	Active high clock
6:7	PAL/NTSC mode select
LK4 Provides for CDS application and variable I/O select	
1:16	MSB I/O group select
2:15	NSB I/O group select
3:14	LSB I/O group select
4:13	N2-P from CDS backplane
*5:12	N2-P from Microboard backplane
*6:11	PREDISPLAY from U27 to EF1-N
7:10	PREDISPLAY from U27 to INT-N
8:9	TPA-P from CDS backplane

NOTES * Preprinted or prewired links

Table V - Page and Character Memory Addressing

Page

$F800_{16} \longrightarrow FBFF_{16}$

or

$FC00_{16} \longrightarrow FFFF_{16}$

Character

$F400_{16} \longrightarrow F7FF_{16}$

Table VI - Signals at Terminal J2

Pin	Signal
1	GND
2	Buffered audio output
3	Link LK1 Pin 8, N=3, normally open
4	GND, U&LC-N for VP601 and VP611 Keyboards
5	Link LK1 pin 7, MRD-N, normally open
6	No connection
7	Link LK1 pin 6, EF2-N, normally open
8	EF3-N, KD-N for VP601 and VP611 Keyboards
9	Buffered audio output
10	No connection
11	V_{DD}
12	Link LK3 pin 5, input port strobe
13	Input port bit 7
14	Input port bit 0
15	Input port bit 6
16	Input port bit 1
17	Input port bit 5
18	Input port bit 2
19	Input port bit 4
20	Input port bit 3

Table VII - Signals at Terminal J3

Pin	Signal
1	Link LK2 pin 1, external oscillator in, normally open
2	Link LK2 pin 2, red gun control,normally closed
3	Link LK2 pin 3, blue gun control,normally closed
4	Link LK2 pin 4, green gun control, normally closed
5	EHS-N, external horizontal sync
6	EVS-N, external vertical sync
7	No connection
8	No connection
9	BURST-P output
10	Luminance, TTL drive output
11	VSYNC-N, TTL drive output
12	HSYNC-P, TTL drive output
13	GND
14	Unbuffered audio output

CDP18S661V3

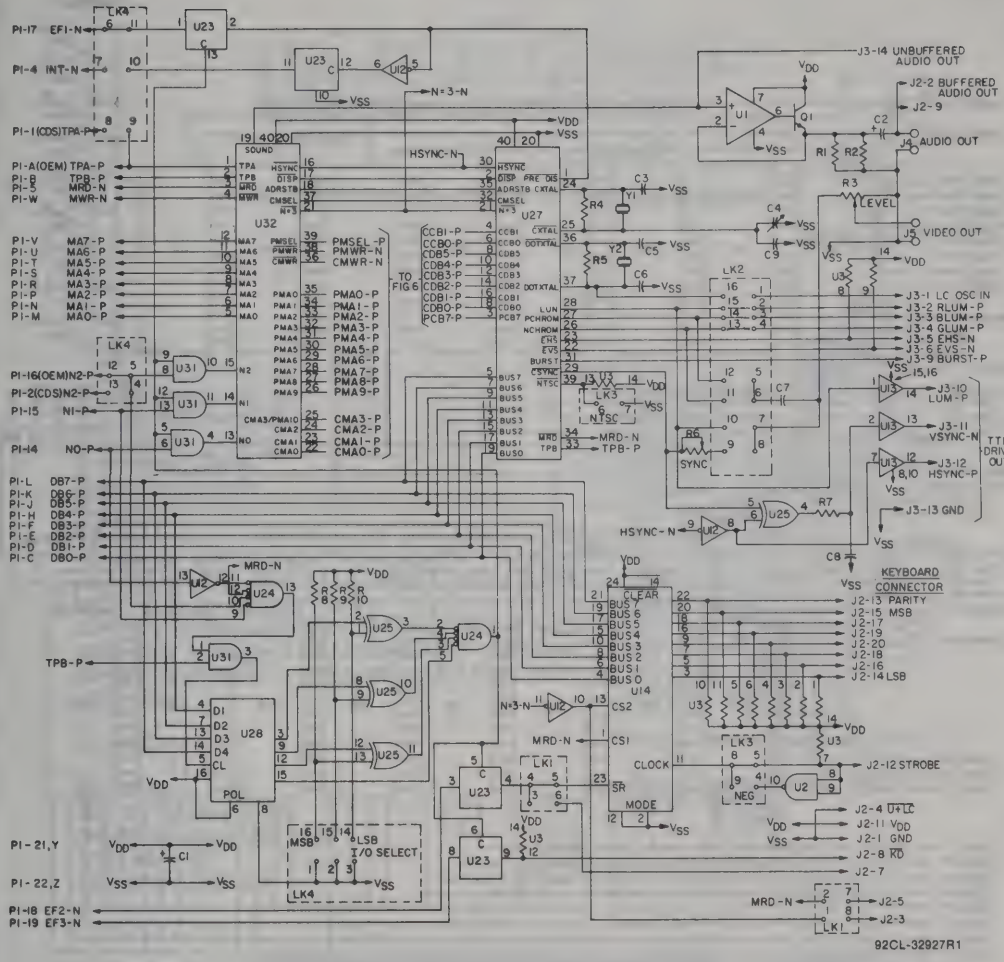


Fig. 5 - Logic diagram of Microboard Video-Audio-Keyboard Interface CDP18S661 - generator and control portions.

CDP18S661V3

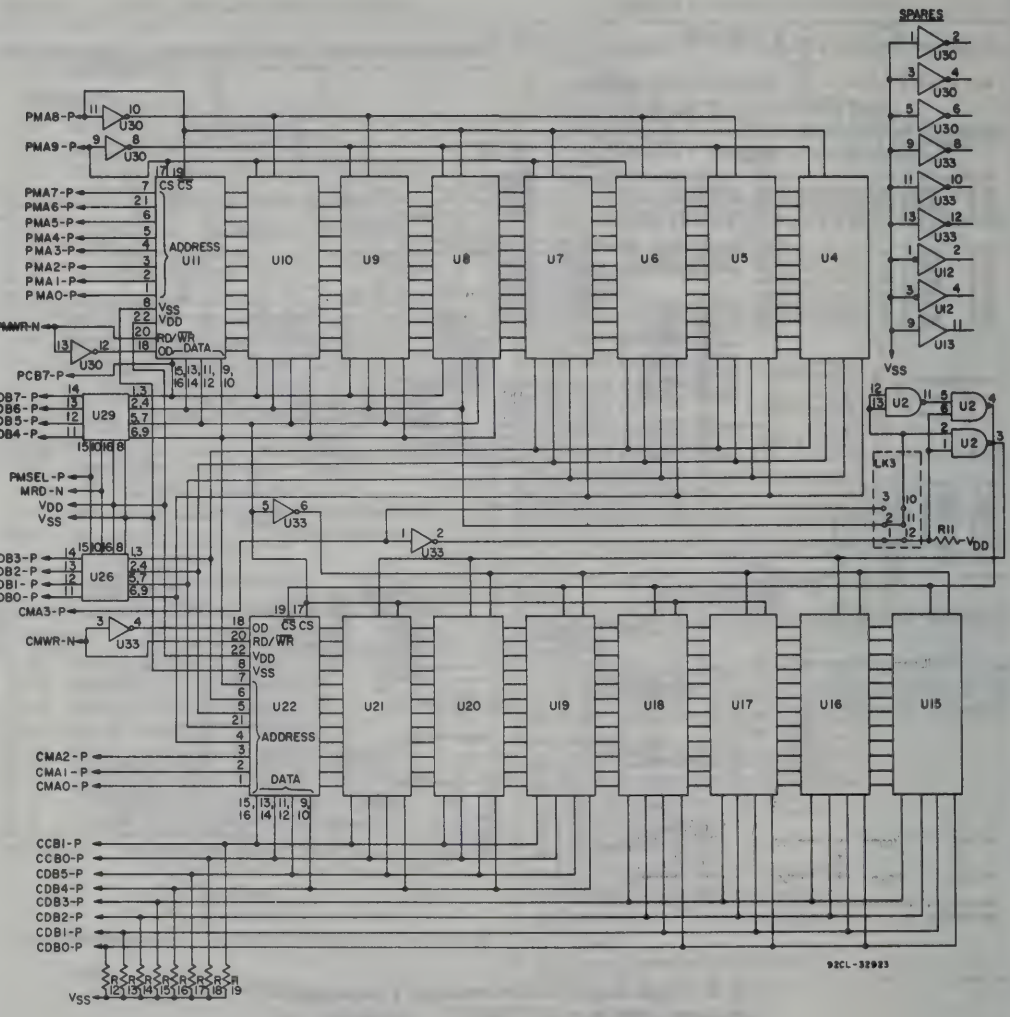


Fig. 6 - Logic diagram of Microboard Video-Audio-Keyboard Interface CDP18S661 - memory portions.

CDP18S661V3

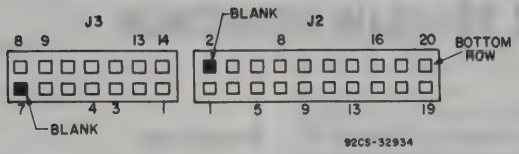


Fig. 7 - Pin location diagram for terminals J2 and J3.

Parts List

C1, C2=22 μF, 25 V
C3, C5, C6, C9=22 pF
C4=variable, 5-25 pF
C7=120 pF, 500 V
C8=0.001 μF, 100 V

J2=right-angle connector, 20 pin, (mates with connector comprised of housing-AMP 86148-1, contact-AMP 86016-1, keying plug-AMP 87077-1, or equivalent)
J3=right angle connector, 14 pin, (mates with connector comprised of housing-AMP 1-86148-4, contact-AMP 86016-1, keying plug-AMP 87077-1, or equivalent)

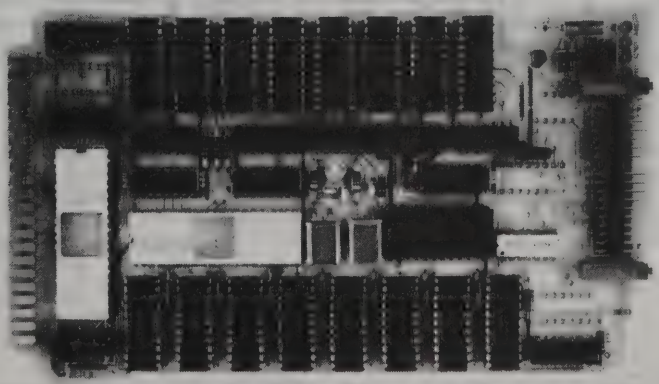
Q1=2N2222

R1, R2=91 Ω, ¼ W
R3, R6=variable 10 kΩ
R4, R5=22 megohms, ¼ W
R7=1 kΩ, ¼ W
R8 - R19=22 kΩ, ¼ W

U1=CA3160BE
U2=CD4011BE
U3=resistor module 22 kΩ
U4 - U11, U15 - U22=MWS5101EL3
U12, U30, U33=CD4069BE
U13, U26, U29=CDP1856CE
U14=CDP1852CE
U23=CD4016BE
U24=CD4002UBE
U25=CD4070BE
U27=CDP1876CE
U28=CD4042BE
U31=CD4081BE
U32=CDP1869CE

Y1=crystal, 8.867237 MHz (PAL)

Y2=crystal, 5.626 MHz (PAL)



CDP18S662

RCA COSMAC Microboard PIO Opto 22 Module Interface

The RCA COSMAC Microboard PIO Opto 22* Module Interface CDP18S662 provides 24 bidirectional parallel I/O lines. In addition to its general-purpose I/O capabilities, the CDP18S662 is specially suited to interface with industry-standard optically isolated solid-state plug-in modules mounted on module racks. Any combination of up to 24 AC or DC input or output, optically isolated, plug-in modules can be interfaced without modifying the Microboard.

The CDP18S662 features a novel built-in interrupt structure that can be programmed to generate an interrupt in response to a change in one or more of the 24 signal lines.

No Microboard modification or programming is required to select the direction of each signal line. The user simply reads or writes independently from each bit.

All optional connections are made with push-on shorting links. No cutting or soldering is required.

The CDP18S662 has minimal power supply and cooling requirements because of its CMOS design. Because the CDP18S662 utilizes the RCA Microboard Universal Backplane, it is readily interchangeable with other RCA Microboards.

Features

- 24 bidirectional signal lines
- Versatile interrupt structure
  - Detects changes in input signals
  - Unique circuit design eliminates selecting the direction of each line
- Interrupts maskable on bit basis
- Compatible with RCA COSMAC Industrial Series Systems and Development Systems
- Wide-operating temperature range –40°C to +85°C
- Low-power static CMOS logic
- Ribbon-cable input/output connector
- High-noise immunity
- Operable from single 5-volt power supply
- Small board size - 4.5 x 7.5 inches
- Assignable I/O addresses
- Simple system interface
- Expandable by use of RCA COSMAC Microboard Universal Backplane

*Opto 22 is a tradename of Opto 22, Huntington Beach, Calif.

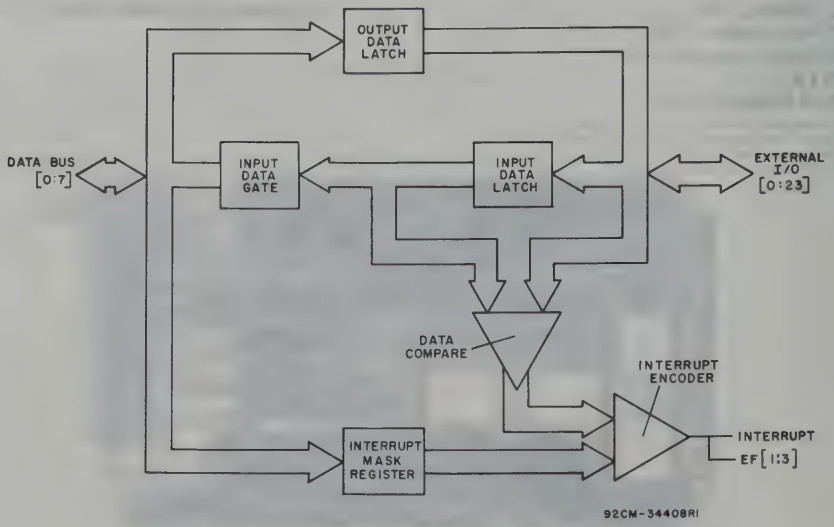


Fig. 1 - Block Diagram of RCA COSMAC Microboard CDP18S662.

Specifications

Operating Temperature Range
–40°C to +85°C
Input Switching Threshold Voltage
Input high: 3.5 volts max.
Input low: 1.5 volts min.
Output Drive Current
Output low (sink, logic 1)
at output volts=0.4 volt: 14 milliamperes
Output high (open-drain leakage, logic 0):
20 microamperes
Power requirements
+5 volts at 10 milliamperes (typ.)
Dimensions
4.5 inches × 7.5 inches (114.3 mm × 190.5 mm)
Board Pitch 0.5 inch (12.7 mm) minimum
Connectors
System interface: Edge fingers, 44 pins on 0.156-inch centers
External interface: Edge fingers, 50 pins on 0.100-inch centers
Option Links: AMP Inc. P/N 531220-3

Solid-State Module Vendors
Opto 22
Huntington Beach, California 92649
International Rectifier (Crydom Div.)
1521 East Grand Ave.
El Segundo, California 90245
GORDOS Arkansas Inc.
1000 North Second St.
Rogers, Arkansas 72756
Guardian California
4050 West Spencer St.
Torrance, California 90503

Microboard Bus Interface Signals (Connector P1)

The following Microboard bus signals are required by the COSMAC Microboard PIO Opto 22 Module Interface, CDP18S662. For additional information on these signals, refer to the published data on the CDP1802A (File No. 1305) and to the **User Manual for**

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P *	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P *	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P *	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P *	In/Out	Data Bus	4	INT-N *	In	Interrupt Request
E	DB2-P *	In/Out	Data Bus	5	MRD-N *	Out	Memory Read
F	DB3-P *	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P *	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P *	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P *	In/Out	Data Bus	9	CLEAR-N *	In	Clear-Mode Request
L	DB7-P *	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	–5V/–15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P *	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P *	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P *	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N *	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N *	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N *	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V *	In	+5 V dc	21	+5 V *	In	+5 V dc
Z	GND *	In	Digital Ground	22	GND *	In	Digital Ground

92CS-34443

*Signals used on RCA COSMAC Microboard CDP18S662.

CDP18S662

the CDP1802 COSMAC Microprocessor, MPM-201. The signals are summarized in Table I which lists the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the CDP18S662.

DB7 through DB0—Eight-bit bidirectional data bus lines. These lines transfer data from the 24 signal lines to and from the CPU in three groups of 8 bits each.

N0, N1, N2—These lines indicate that an I/O instruction is being executed. They are derived from the three low-order bits of the CDP1802 N-register and are true only during an I/O instruction execution. The CDP18S662 decodes these lines to determine which device or channel data is input from or output to. See Table II.

Table II—I/O Instructions

Instruction Code				I/O	P2
Input	Output	Interrupt Mask	Flag	Signal Lines	Connector Pins*
6A	62	65	EF1	0-7	47-33
6B	63	66	EF2	8-15	31-17
6C	64	67	EF3	16-23	15-1

*All even numbered pins connected to logic ground.

$\overline{\text{MRD}}$—This signal defines the direction of the I/O data transfer. A low level indicates a transfer from the memory to I/O; a high level, a transfer from I/O to memory.

TPA & TPB—Timing pulses generated by the CPU which occur once in each machine cycle. TPA & TPB are coded with the N-lines to provide seven input/output enable lines. Additionally, the leading edge of TPB is used to latch data into the output registers.

$\overline{\text{EF1}}$, $\overline{\text{EF2}}$, $\overline{\text{EF3}}$—The CDP18S662 uses these three inputs to indicate which of the three groups of 8 signal lines has requested an interrupt. These lines are active only when the CDP18S662 assigned group is selected. See Table II.

$\overline{\text{INT}}$—If interrupts are enabled, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be disabled or enabled under software control. If Interrupt Enable (IE) is set, the recognition of INT results in the completion of execution of the current instruction, followed by an interrupt service cycle during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The interrupt service cycle lasts one machine cycle (eight clock pulses), after which processing resumes with R1 as the program counter. After processing the interrupt, interrupts must be enabled by executing a return instruction.

$\overline{\text{CLEAR}}$—A low level on this signal indicates a system reset. The output registers and the interrupt mask registers are reset. The effect of this signal is to set the open collector output line drivers to the high-impedance state and to disable all interrupts.

Operation of the CDP18S662 Parallel Interface

Two Level I/O Addressing Conventions. During an I/O instruction execution, the CPU outputs the three low-order bits of its N register on the N2, N1, and N0 lines. The $\overline{\text{MRD}}$ signal indicates the direction of the data flow. Thus, the instructions 61 through 67 provide seven output and 69 through 6F provide seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices.

The OUT 1 (hex 61) output instruction is used to transmit a group select byte to the I/O. This byte is latched and decoded by all Microboards in the system.

This group number is divided into two parts. The four least significant bits are linearly encoded (0,1,2,4) and the upper four bits are binary encoded (0-15). Thus, the number of addresses provided is 15 (binary-encoded) plus 4 (linear encoded), times the 6 commands left after reserving the 61 and 69 instructions. The total number of useful I/O addresses is 114. The CDP18S662 does not use the lower four bits of the group number, and because the various functions on the Microboard require all six available commands, there can only be 15 of these Microboards in a system. The use of additional boards would require additional external selection logic.

The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S662 does not provide this feature.

Data Transfers. The CDP18S662 includes a row of four header pins and matching shorting clips that can be used to assign the board to any of 15 possible I/O groups. See Table III. To enable the Microboard, a 61 instruction outputting the hex selection address from Table III is executed. Once the CDP18S662 Microboard I/O group has been selected, subsequent I/O instructions will transfer data or set/reset interrupt masks.

Table III—I/O Select Connections

I/O Select Code	Jumper Connections (LK1)
10	4-5
20	3-6
30	3-6, 4-5
40	2-7
50	2-7, 4-5
60	2-7, 3-6
70	2-7, 3-6, 4-5
80	1-8
90	1-8, 4-5
A0	1-8, 3-6
B0	1-8, 3-6, 4-5
C0	1-8, 2-7
D0	1-8, 2-7, 4-5
E0	1-8, 2-7, 3-6
F0	1-8, 2-7, 3-6, 4-5

Any of the 24 signal lines can be input to the data bus, and into memory, by instructions 6A, 6B, or 6C. Similarly, data can be output to any of the 24 open collector outputs by executing instructions 62, 63, or 64. See Table II for the byte/bit position assignments of data bits to the 24 output/input signal lines. Writing a zero to any bit position disables the output driver (high-impedance state) and enables the use of that signal line for input.

Interrupts. The CDP18S662 can be programmed to generate an interrupt when any selected input changes state after being read by the system. By executing instructions 65, 66, and 67, mask bits can be set true or false. Writing a one in the corresponding bit position will enable the interrupt for that signal line. Once enabled, if that signal line changes state, an interrupt will be generated. The interrupt will remain on until the data bit that generates the interrupt to the system is read, or a new mask is loaded that disables that signal line's interrupt. Link LK2 can be removed to disable interrupts entirely. Interrupts generated as a result of mask output by instructions 65, 66, or 67 will turn on flags EF1, EF2, and EF3, respectively. See Table II.

Power to External Logic

Link LK3 connects the 5-volt power supply from the backplane connector P1 to pin 49 on connector P2. This connection may be used to power external circuitry including the optical modules. The current requirements of the external equipment must not be in excess of a value that can be adequately handled by the power supply.

Installation in COSMAC Development Systems

The CDP18S662 may be installed into any of the available I/O slots (14-18 or 21-23) in the COSMAC Development System (CDS II) CDP18S005 or in the COSMAC DOS Development System (CDS III) CDP18S007 to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may be easily allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

When a CDP18S662 is installed in a COSMAC Development System II or III, the signals indicated in Table IV must be connected on the backplane to the I/O slot on the CDS selected for the CDP18S662.

The CDP18S662 is fully compatible with the COSMAC Development System IV.

Table IV—CDS Backplane Connections (CDP18S005 and CDP18S007 Only)

Signal	Jumper to Pin
N0-P	P1-14
N1-P	P1-15
N2-P	P1-16
RESET-OP	P1-9

CDP18S662

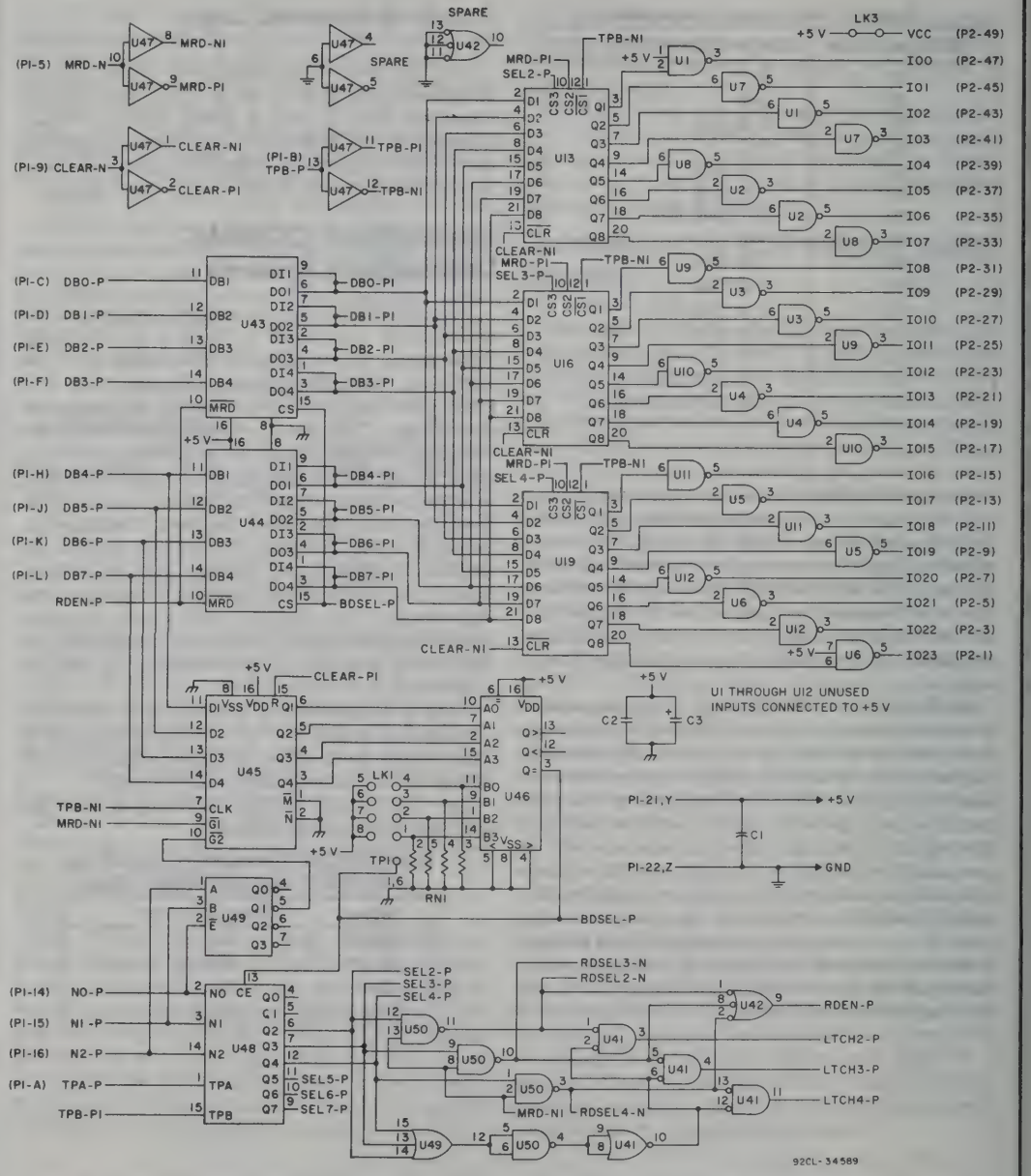


Fig. 2 - Logic Diagram of RCA COSMAC Microboard CDP18S662—Output and I/O Selection Portion.

CDP18S662

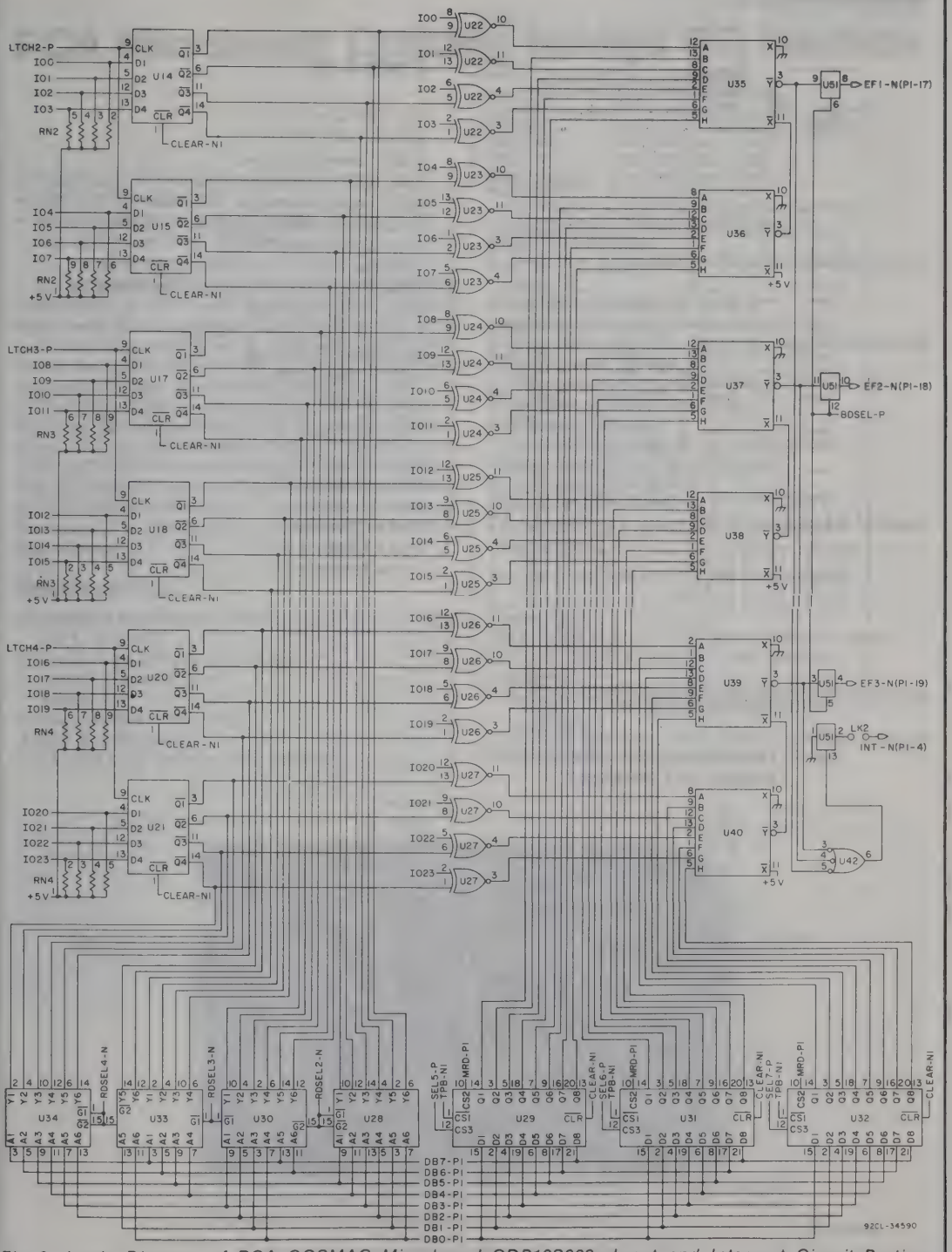


Fig. 3 -Logic Diagram of RCA COSMAC Microboard CDP18S662—Input and Interrupt Circuit Portion.

CDP18S662

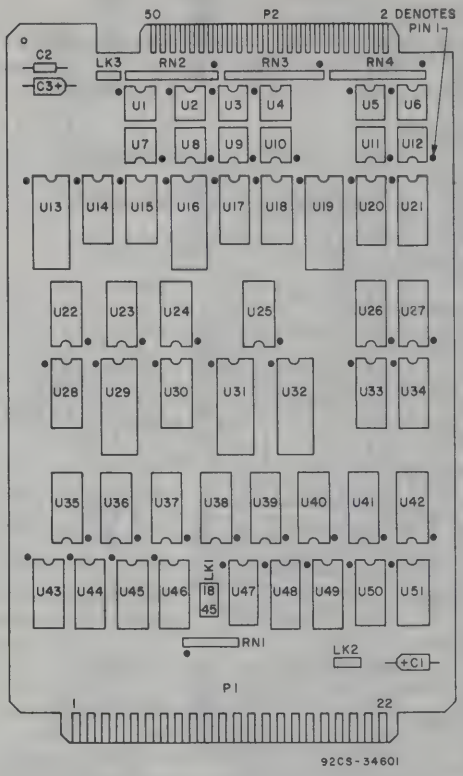


Fig. 4 - Layout Diagram of RCA COSMAC Microboard CDP18S662.

Parts List

C1, C3 = 22 μF, 15 V
C2 = 0.1 μF, 50 V
LK1 = connector, 8-pin
LK2, LK3 = connector, 2-pin
RN1 = resistor network, 22 kilohms
RN2-RN4 = resistor network, 10 kilohms
U1-U12 = CD40107BE
U13,U16,U19,U29,U31,U32 = CDP1875CE
U14,U15,U17,U18,U20,U21 = F40175BPC
U22,U27 = CD4077BE
U28,U30,U33,U34 = CD4503BE
U35-U40 = CD4086BE
U41 = CD4001UBE
U42 = CD4023UBE
U43,U44 = CDP1857CE
U45 = CD4076BE
U46 = CD4585BE
U47 = CD4041UBE
U48 = CDP1853CE
U49 = CD4556BE
U50 = CD4011UBE
U51 = CD4066BE

CDP18S663

RCA Microboard Optically Isolated DC Interface

- **8 Input and 8 Output Parallel I/O Lines**
- **1500-Volt Isolation**
- **Accepts Two Input Voltage Ranges — 4 to 16 Volts or 24 to 50 Volts**

The RCA Optically Isolated DC Interface Microboard CDP18S663 provides eight general-purpose input and eight ouput parallel I/O lines, isolated from each other and from the system by up to 1500 volts. This feature makes the CDP18S663 suitable for industrial signaling applications where ground loops must be avoided.

The CDP18S663 features a novel built-in interrupt structure that can be programmed to generate an interrupt in response to a change in one or more signal lines.

The CDP18S663 has minimal power supply and cooling requirements because of its CMOS design. Because the CDP18S663 utilizes the RCA Microboard Universal Backplane, it is readily interchangeable with other RCA Microboards.

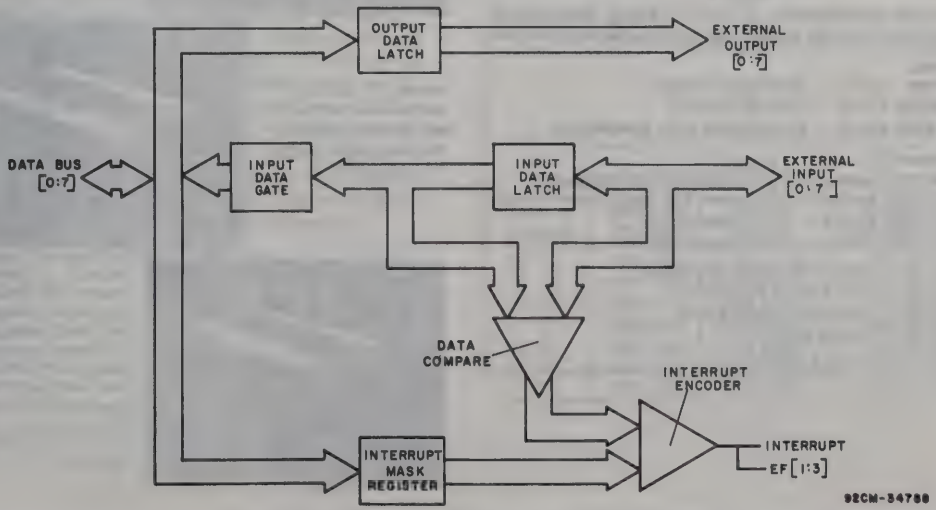
Features

- **8 Input and 8 Output signal lines**
- **1500-Volt isolation**
- **Versatile interrupt structure — Detects changes in input signals**
- **Interrupts maskable on bit basis**
- **Options selected by push-on jumpers**
- **Compatible with RCA Industrial Series Systems and Development Systems**
- **Wide-operating-temperature range -40°C to +85°C**
- **Low-power CMOS static logic**
- **High-noise immunity**
- **Operable from single 5-volt power supply**
- **Small board size - 4.5 x 7.5 inches**
- **Assignable I/O address**
- **Simple system interface**
- **Expandable by use of RCA Microboard Universal Backplane**

Specifications

Operating Temperature Range:
-40°C to +85°C
Input Voltage Range (Logic High):
Jumper On: 4-16 volts
Jumper Off: 24-50 volts
Output Current: 10mA max.
Power Requirements:
+5 volts at 50 milliamperes (typical)

Dimensions:
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board Pitch 0.5 inch (12.7 mm) minimum
Connectors:
System interface: Edge fingers, 44 pins on 0.156-inch centers
External interface: 32-pin header, 0.025-inch square pins on 0.150-inch centers



Block Diagram of RCA Microboard CDP18S663.

RCA Microboard Industrial Chassis Series

RCA's Microboard Industrial chassis series includes 21 chassis easily convertible, through a broad line of versatile accessories, to hundreds of different customer-selectable configurations for mounting on a rack, backwall, or desk, or in custom equipment.

They range from a simple backplane with connectors for four boards to a fully enclosed chassis with room for a plug-in power supply and 24 boards. Other sizes hold 8, 12, 16, 20, or 24 boards. Each unit can be customized with accessories to give you exactly what you want in a chassis.

Rugged — designed to stand up to tough industrial environments
Flexible — for system prototyping design and redesign
Attractive — desk-top configuration enhances any office
Versatile — mountable on 19″ EIA rack, on backwall, or on surface
Accessible — provides front or side access to controls
Efficient — sizes available to accommodate up to 24 cards
Easy to Use — Microboard Universal Backplane
Compact — small CMOS Microboards, no bulky fans

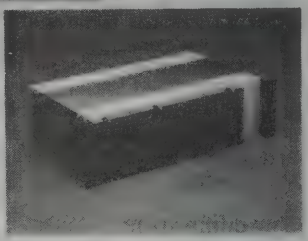
Table I — Product Designations of RCA COSMAC Microboard Industrial Chassis Series and Associated Accessories.

Chassis
MSI 800 series — Standard chassis
MSI 8800 series — Deluxe chassis
MSI 8000 series — Backplanes with connectors
Accessories
MSIA 0100 series — Solid top and bottom covers
MSIA 0200 series — Perforated top and bottom covers
MSIA 0300 series — Solid rear panels
MSIA 0400 series — Front panel guards
MSIA 06 — Mounting angle brackets
MSIA 07 — End bezels (handles)
MSIA 08 — Four-card front panel
MSIA 10 — Cable conduit
MSIA 11 — Card extractor

Flexibility with Style — Deluxe Chassis MSI 8825
Includes all accessories shown

Photo A — Deluxe chassis MSI 8825 with angle brackets positioned for flush mounting in a 19-inch rack.

Photo B — Deluxe chassis MSI 8825 with front panel guard and angle brackets positioned for recessed mounting in 19-inch rack.



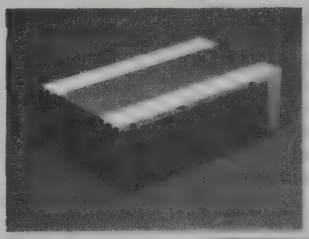


Photo C — Deluxe chassis MSI 8825 with front panel guard and angle brackets positioned for backwall mounting.

Photo D — Deluxe chassis MSI 8825 with end bezels (handles) and front panel guard for desk top use.

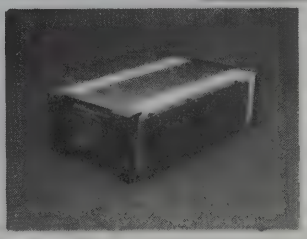


Photo E — Deluxe chassis MSI 8825 with end bezels (handles) and front panel guard. End panel removed to show CDP18S640 display and control Microboard module (available separately) in end position for access to controls.

Industrial Chassis Series

The RCA COSMAC Microboard Industrial Chassis Series provides the designer with extremely flexible means of mounting, connecting, and enclosing the broad line of standard RCA Microboards as well as the newly developed RCA MSI-series Industrial Microboard products. The three series of industrial chassis available provide the user with both a wide range of option levels and a wide choice in the number of Microboard slots. One chassis series comprises a bare 44-pin Microboard backplane (MSI 8000); the second comprises a functional but unadorned chassis (MSI 800); the third comprises a complete chassis system that is fully enclosed, looks at home on a desk top, but is also rack or backwall mountable (MSI 8800). The Deluxe MSI 8800 series is the optimum starting point for packaging design.

Accessories are available to build the MSI 800 series at any option level up to that of the MSI 8800 series. See Tables I and II for model designations of the various chassis and accessories.

The basic unit of all series is 2.4 inches wide and accepts four Microboards (4.5 x 7.5 inches) on 0.6 inch pitch. Each series is available in 1 to 7 unit widths, with space for up to 24 Microboards. The 7-unit-wide model has a 25th connector dedicated to a plug-in power supply. The supply can mount in any other chassis, but occupies four slots.

The Standard MSI 825 (with optional MSIA 06 angle brackets) or the Deluxe MSI 8825 (angle brackets included) can be mounted in a 19-inch EIA rack, taking only 5-1/4-inch panel height. Flush or recessed mounting is possible. The brackets may also be used for backwall mounting of any of the MSI 800 or 8800 series chassis. See photos A, B, C, and K.*

The Deluxe MSI 8800 series is supplied with end bezels/carrying handles for portable or desk top use. The cover plate(s) under the end bezels may be omitted for access to the end card. This access allows the use of boards such as the CDP18S640 Control and Display Module or CDP18S480 PROM Programmer Module while the rest of the system is kept enclosed. See photos E and N. The end bezels are available as accessories for the Standard MSI 800 series.

*Photos G through P are on the back cover.

Features*

- **Rugged steel/aluminum frame — protective coating**
- **Microboard Universal Backplane**
- **Gold plated card edge connectors**
- **0.062 inch FR4 epoxy backplane**
- **4, 8, 12, 16, 20, 24, or 25 card slots**
- **Full-length card guides**
- **Extractor rails**
- **Access slots for ribbon cable**
- **Ample room within chassis for internal cabling**
- **Fully enclosed (MSI 8800)**
- **Rack or backwall mounting: only 5-1/4-inches high x 10.08 inches deep**
- **Flush or recessed rack mounting**
- **Protective see-through cover for wiring (MSI 8800)**
- **Desk-top use with carrying handles/end bezels (MSI 8800)**
- **Optional accessibility of end card (MSI 8800)**
- **Optional plug-in power supply (MSIM 40 or MSIM 40E)**
- **Optional power I/O interface module MSIM 20**
- **Connector for external supply**
- **Many accessories available: customize the chassis as needed**
- **Optional rack-mount wire trough front-panel wiring**

*Apply to MSI 800 or 8800 Series.

Table II —
Designation Numbers for the Various Chassis

No. of Slots:	Standard Chassis	Deluxe Chassis	Backplanes With Connectors
4	MSI 804	MSI 8804	MSI 8004
8	MSI 808	MSI 8808	MSI 8008
12	MSI 812	MSI 8812	MSI 8012
16	MSI 816	MSI 8816	MSI 8016
20	MSI 820	MSI 8820	MSI 8020
24	MSI 824	MSI 8824	MSI 8024
25	MSI 825	MSI 8825	MSI 8025

Industrial Chassis Series

MSI 800 Series: Standard Chassis

The MSI 800 series standard chassis have card guides and chassis added to the MSI 8000 series backplanes. See photo L and M. Front and rear aluminum extrusions have an alodine finish and are mounted to painted steel side pieces to give considerable structural strength. Spacer strips slide into the extrusions to locate full-length snap-in card guides. The connector tabs of the MSI 8000 backplane series slide into the rear extrusions, and nut plates slide into the front extrusions. Both are held captive by the side pieces. The nut plates provide for the mounting of MSI series industrial Microboards or matching MSIA 08 blank front panels. See Fig. 1 for dimensions.

A power supply connector is supplied loose with each chassis. For information see page 7. The chassis is electrically isolated from the Microboard backplane but may readily be grounded by connecting pin 22 or Z to a convenient chassis screw.

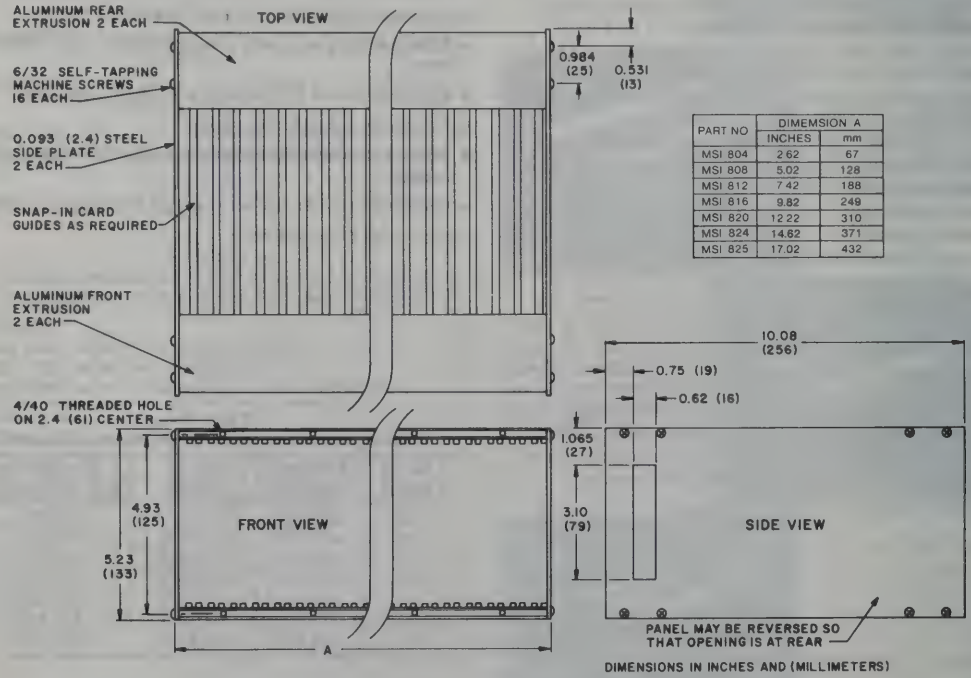
The side pieces have an entry slot for cable access to the front of the Microboards, but are reversible front to rear. If it is desired to mount and access the power-supply connector from the outside of the chassis, the left side piece should be reversed so that the entry slot is towards the rear.

Stick-on rubber feet are provided for desk-top use and are supplied loose.

A number strip along the inside of the bottom front extrusion identifies slot positions.

If the Microboards to be inserted in the chassis contain mounted standoffs, see the discussion under accessories for standoff removal. The standoffs will not clear the full-length card guides.

The MSI 800 series chassis will take any of the options listed in Table IV to bring it up partially or fully to the MSI 8800 deluxe chassis. Figs. 2 and 3 show mounting of optional accessories. Photo F shows a MSI 812 with available accessories. Refer to Fig. 4 for dimensions with optional end bezels or angle brackets. The MSI 825, which has slots for 24 Microboards, dedicates four additional right-most slots to power supply use.



PART NO	DIMEMSION A	
	INCHES	mm
MSI 804	2.62	67
MSI 808	5.02	128
MSI 812	7.42	188
MSI 816	9.82	249
MSI 820	12.22	310
MSI 824	14.62	371
MSI 825	17.02	432

Fig. 1 — Standard chassis MSI 800 series dimensions.

Industrial Chassis Series

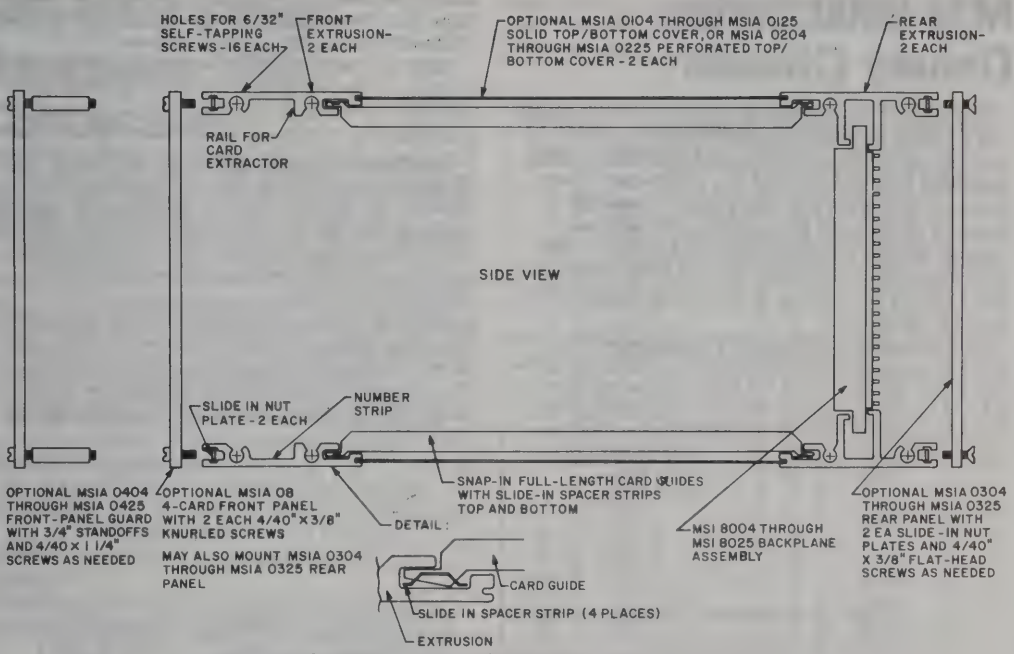

HOLES FOR 6/32" SELF-TAPPING SCREWS-16 EACH
FRONT EXTRUSION-2 EACH
OPTIONAL MSIA 0104 THROUGH MSIA 0125 SOLID TOP/BOTTOM COVER, OR MSIA 0204 THROUGH MSIA 0225 PERFORATED TOP/BOTTOM COVER-2 EACH
REAR EXTRUSION-2 EACH
RAIL FOR CARD EXTRACTOR
SIDE VIEW
SLIDE IN NUT PLATE-2 EACH
NUMBER STRIP
OPTIONAL MSIA 0404 THROUGH MSIA 0425 FRONT-PANEL GUARD WITH 3/4" STANDOFFS AND 4/40 x 1 1/4" SCREWS AS NEEDED
OPTIONAL MSIA 08 4-CARD FRONT PANEL WITH 2 EACH 4/40"x3/8" KNURLED SCREWS
MAY ALSO MOUNT MSIA 0304 THROUGH MSIA 0325 REAR PANEL
SNAP-IN FULL-LENGTH CARD GUIDES WITH SLIDE-IN SPACER STRIPS TOP AND BOTTOM
DETAIL:
CARD GUIDE
SLIDE IN SPACER STRIP (4 PLACES)
EXTRUSION
MSI 8004 THROUGH MSI 8025 BACKPLANE ASSEMBLY
OPTIONAL MSIA 0304 THROUGH MSIA 0325 REAR PANEL WITH 2 EA SLIDE-IN NUT PLATES AND 4/40" X 3/8" FLAT-HEAD SCREWS AS NEEDED

Fig. 2 — Standard chassis MSI 800 series assembly cutaway.

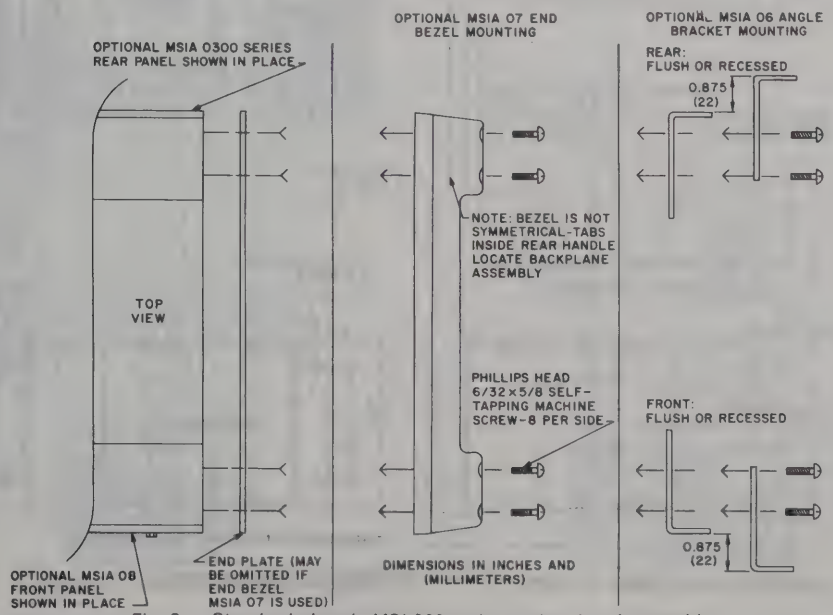

OPTIONAL MSIA 0300 SERIES REAR PANEL SHOWN IN PLACE
TOP VIEW
OPTIONAL MSIA 08 FRONT PANEL SHOWN IN PLACE
END PLATE (MAY BE OMITTED IF END BEZEL MSIA 07 IS USED)
OPTIONAL MSIA 07 END BEZEL MOUNTING
NOTE: BEZEL IS NOT SYMMETRICAL-TABS INSIDE REAR HANDLE LOCATE BACKPLANE ASSEMBLY
PHILLIPS HEAD 6/32x5/8 SELF-TAPPING MACHINE SCREW-8 PER SIDE
DIMENSIONS IN INCHES AND (MILLIMETERS)
OPTIONAL MSIA 06 ANGLE BRACKET MOUNTING
REAR: FLUSH OR RECESSED
0.875 (22)
FRONT: FLUSH OR RECESSED
0.875 (22)

Fig. 3 — Standard chassis MSI 800 series optional end assembly.

Industrial Chassis Series

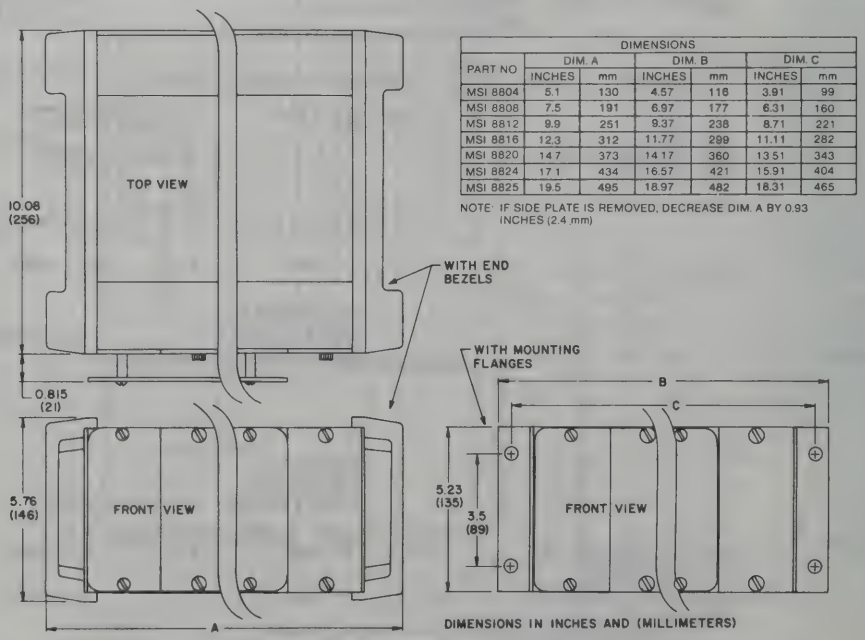
MSI 8800 Series Deluxe Chassis

The MSI 8800 series deluxe chassis have full covers and a variety of mounting options added to the standard MSI 800 series. **The MSI 8800 series comes assembled with slide-in solid top and bottom covers, screw-fastened front and rear panels, a standoff mounted see-through front panel guard, and two carrying handle/end bezels.** Photo D shows an MSI 8825 setup for desk-top use. See Fig. 4 for dimensions, and Table IV for a listing of accessories supplied with the MSI 8800 series.

Two mounting angle brackets are included (loose) to allow flush or recessed mounting from the front or the rear of the chassis. The MSI 8825 may be mounted in a 5-1/4-inch opening of a 19-inch rack and may have either the chassis front or the protective wiring cover flush with the rack front. As in the MSI 800 series, **rubber feet and a power-supply connector are supplied** loose. See the discussion under accessories for removal of standoffs from Microboard modules.

Both the end bezels and steel side plates may be left in place, or one or the other may be omitted. With only the end bezels in place, the chassis becomes a good basis for a desk-top development system. The left-most position might mount a CDP18S480 PROM Programmer or CDP18S640 Control and Display Module. See photos E and N. Access to the right-most socket solder side would be useful for board development. Note that for the MSI 8825, the right-most socket is only for power supply use and will not operate Microboards.

The front panel guard supplied is one unit width (2.4-inch) smaller than the chassis width. This space is to provide access to the supply power switch (if used). The MSI-8804 is not supplied with a front panel guard. Guards of any unit width may be bought as options.



PART NO	DIMENSIONS					
	DIM. A		DIM. B		DIM. C	
	INCHES	mm	INCHES	mm	INCHES	mm
MSI 8804	5.1	130	4.57	116	3.91	99
MSI 8808	7.5	191	6.97	177	6.31	160
MSI 8812	9.9	251	9.37	238	8.71	221
MSI 8816	12.3	312	11.77	299	11.11	282
MSI 8820	14.7	373	14.17	360	13.51	343
MSI 8824	17.1	434	16.57	421	15.91	404
MSI 8825	19.5	495	18.97	482	18.31	465

NOTE: IF SIDE PLATE IS REMOVED, DECREASE DIM. A BY 0.93 INCHES (2.4 mm)

Fig. 4 — Deluxe chassis MSI 8800 series dimensions.

MSI 8000 Series: Backplane With Connectors

Each of the MSI 8000 series chassis consists of a backplane (See photo G) with 44-pin, 0.156-inch pitch card edge connectors on 0.6-inch centers. See Fig. 5 for dimensions. All pins having the same designations are bussed together. Pins 22 and Z (Microboard ground) and 21 and Y (+5 volt) are heavily bussed. See Table III for Microboard backplane pin assignments.

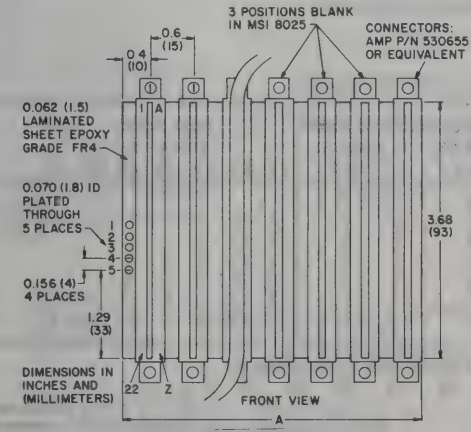
A five-hole pattern on 0.156-inch centers is provided at the extreme left side of the backplane for mounting a power-supply connector. Backplane pins 11 (-15 volts), 12 (spare), and 20 (+15 volts), as well as +5 volts and ground, are wired to this location. See Fig. 6 for connector details. **The power supply connector is supplied loose.**

The MSI 8025, 25-card backplane, occupies the same space as a 28-card version would. Connectors 25, 26, and 27 are omitted, however, and the 28th connector is wired only for plug-in power supply connections.

Connector positions are numbered left to right as seen from the connector side, and connector pins are numbered top to bottom: 1-22 on the left, A-Z on the right. Microboards are to be mounted with components facing left.

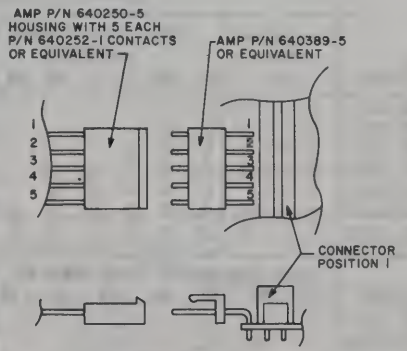
Table III — Microboard Backplane Pin Assignments

Pin	Signal	Pin	Signal
1	DMAI-N	A	TPA-P
2	DMAO-N	B	TPB-P
3	RNU-P	C	DB0-P
4	INT-N	D	DB1-P
5	MRD-N	E	DB2-P
6	Q-P	F	DB3-P
7	SC0-P	H	DB4-P
8	SC1-P	J	DB5-P
9	CLEAR-N	K	DB6-P
10	WAIT-N	L	DB7-P
11	-15 V	M	A0-P
12	SPARE	N	A1-P
13	CLOCK OUT	P	A2-P
14	N0-P	R	A3-P
15	N1-P	S	A4-P
16	N2-P	T	A5-P
17	EF1-N	U	A6-P
18	EF2-N	V	A7-P
19	EF3-N	W	MWR-N
20	+15 V	X	EF4-N
21	+5 V	Y	+5 V
22	GND	Z	GND



PART NO.	DIMENSION A	
	INCHES	mm
MSI 8004	2.4	61
MSI 8008	4.8	122
MSI 8012	7.2	183
MSI 8016	9.6	244
MSI 8020	12.0	305
MSI 8024	14.4	366
MSI 8025	16.8	427

Fig. 5 — Backplane MSI 8000 series dimensions.



SUPPLY CONNECTOR PIN NO.	BACKPLANE CONNECTOR PIN NO	USE
1	11	-15V
2	12	SPARE
3	20	+15V
4	Y, 21	+5V
5	Z, 22	GROUND

Fig. 6 — Power supply connector.

Industrial Chassis Series

MSIA Accessory Series

Table IV lists the accessory part numbers versus the chassis that they fit. Parts that are standard on the Deluxe MSI 8800 series are marked "S"; those that are available optionally to fit are marked "O". Any part marked "S" or "O" will also fit the corresponding Standard MSI 800 series chassis. Table V gives condensed description of each accessory. **Accessories are normally supplied in quantities of 10.**

MSIA 0100 series **solid top or bottom covers** or MSIA 0200 series **perforated top or bottom** covers slide into slots in the front and rear extrusion (See Fig. 2). To mount the cover one end bezel and/or slide plate must be removed. Only one end plate should be removed at one time and the chassis should not be stressed when the end plate is off.

Note that MSI 0400 series **front panel guards** are normally supplied one size smaller than the corresponding chassis (except MSI 8804), but may be used at any size up to the width of the chassis.

The MSIA 0300 series of **rear panels** can be mounted on the front to replace one or more MSIA08 front panels. An access slot for front entry of cables is thus provided. When a MSIA 0300 series panel is mounted in the rear of a MSI 800 series chassis, a side panel must be removed to insert top and bottom slide-in nut plates supplied with the panel.

The MSIA 10 **cable conduit** is a 19-inch rack mount wiring guide that occupies 1-3/4 inches of rack space. It has a snap-off aluminum cover and is recessed so that the cover is flush with the rack front. See photo K. It may be used with a MSI 8825 or MSI 825 chassis with angle brackets to guide wiring to the front surface of the chassis. The chassis should be mounted in the recessed position.

Depending on the date of manufacture, Microboards may be equipped with **standoffs.** These standoffs are unnecessary for Microboards installed in the Industrial Chassis Series and should be removed because they may not clear the full-length card guides. If the spacer is a drive pin inside a nylon sleeve, heat the head of the pin for several seconds with a hot soldering iron, and remove the sleeve with pliers. The pin is then free to drop out. Do not use cutters on the pins: they are hardened and will damage cutters or fly apart suddenly.

The MSIA 11 **card extractor** consists of an ejector cam and a snap-on retaining ring. This card extractor is to be inserted through the hole at the top corner of a Microboard and the retaining ring snapped over its pin. The ring is marked "up" for the side away from the board. The ejector cam may be mounted on the bottom corner of the Microboard if the top is not clear, but extra care may be needed to remove and insert the Microboard. The card extractor mounts in a 0.1-inch hole that is 0.15 inch from both the end and the side of the Microboard.

Figs. 7 through 14 give the dimensions for the optional accessories.

Table IV — Accessory Table — MSI 8800 Series.

Chassis	Front Panel MSIA* 08	Front Panel Guard MSIA 04* 04	08	12	16	20	24	25	Angle Brackets MSIA 06, N=2	End Bezel MSIA 07, N=2	Rear Panel MSIA 03* 04	08	12	16	20	24	25
MSI 8804	S, N = 1	O							S	S	S						
MSI 8808	S, N = 2	S	O						S	S	O	S					
MSI 8812	S, N = 3	O	S	O					S	S	O	O	S				
MSI 8816	S, N = 4	O	O	S	O				S	S	O	O	O	S			
MSI 8820	S, N = 5	O	O	O	S	O			S	S	O	O	O	O	S		
MSI 8824	S, N = 6	O	O	O	O	S	O		S	S	O	O	O	O	O	S	
MSI 8825	S, N = 7	O	O	O	O	O	S	O	S	S	O	O	O	O	O	O	S

Chassis	Solid Top/Bottom Cover MSIA 01* 04	08	12	16	20	24	25	Perforated Top/Bottom Cover MSIA 02* 04	08	12	16	20	24	25
MSI 8804	S							O						
MSI 8808		S							O					
MSI 8812			S							O				
MSI 8816				S							O			
MSI 8820					S							O		
MSI 8824						S							O	
MSI 8825							S							O

Notes:
N = ( ): Number of these accessories supplied, otherwise N = 1
S = Standard
O = Optional — any rear panel MSIA 0300 series marked S or O will fit on front of chassis.

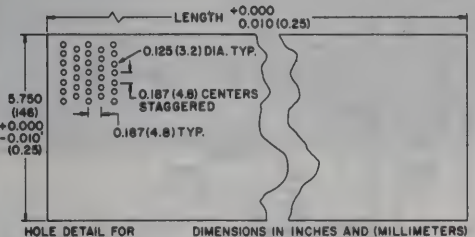
*The last two digits of these designations are one of 04, 08, 12, 16, 20, 24, or 25 depending on size.

Industrial Chassis Series

Table V — Condensed Description of Accessories for RCA COSMAC Microboard Industrial Chassis Series. See Photos F and K for accessory photographs.

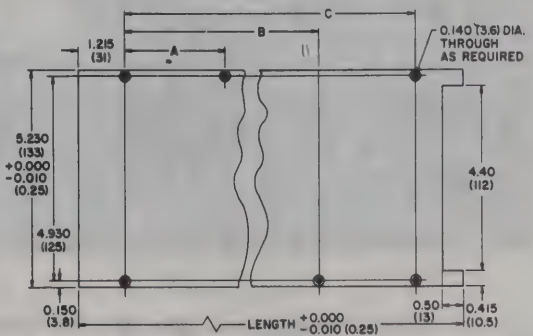
Part Designation	Name	Material	Finish	Fig. No.
MSIA 0100*	Solid Cover (Top or Bottom)	Aluminum	Yellow-Bronze Alodine (inside) Black Paint (outside)	7
MSIA 0200*	Perforated Cover	Aluminum	Yellow-Bronze Alodine (inside) Black Paint (outside)	7
MSIA 0300*	Rear Panel	Aluminum	Yellow-Bronze Alodine	8
MSIA 0400*	Front Panel Guard	Plastic	Gray Transparent	9
MSIA 06	Angle Bracket	Steel	Black Paint	10
MSIA 07	End/Bezel/ Handle	Plastic (non-conductive)	Black Paint	11
MSIA 08	Front Panel (4 card)	Aluminum	Yellow-Bronze Alodine	12
MSIA 10	Cable Conduit: Cover Duct End Brackets	Aluminum Plastic Steel	Yellow-Bronze Alodine Dark Gray Black Paint	13
MSIA 11	Card Extractor	Nylon	White	14

*The last two digits of these designations are one of 04, 08, 12, 16, 20, 24, or 25 depending on size.


LENGTH +0.000 0.010 (0.25)
0.125 (3.2) DIA. TYP.
0.187 (4.8) CENTERS STAGGERED
0.187 (4.8) TYP.
5.750 (146) +0.000 -0.010 (0.25)
HOLE DETAIL FOR MSIA 0200 SERIES PERFORATED COVERS ONLY
DIMENSIONS IN INCHES AND (MILLIMETERS)
MATERIAL: 0.062 (1.6) ALUMINUM
FINISH: INSIDE: ALODINE TREATMENT
OUTSIDE: BLACK TEXTURED PAINT

LENGTH		PART NUMBER	
INCHES	mm	SOLID	PERFORATED
2.430	62	MSIA 0104	MSIA 0204
4.830	123	MSIA 0108	MSIA 0208
7.230	184	MSIA 0112	MSIA 0212
9.630	245	MSIA 0116	MSIA 0216
12.030	306	MSIA 0120	MSIA 0220
14.430	367	MSIA 0124	MSIA 0224
16.830	427	MSIA 0125	MSIA 0225

Fig. 7 — MSIA 0100, MSIA 0200 series solid or perforated top and bottom covers.

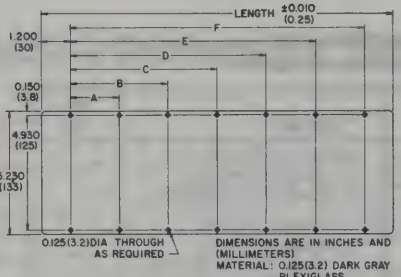


LENGTH	A DIM.	B DIM.	C DIM.	HOLES REQUIRED	PART NO.
2.430 (62)				2	MSIA 0304
4.830 (123)			2.400 (61)	4	MSIA 0308
7.230 (184)			4.800 (122)	4	MSIA 0312
9.630 (245)			7.200 (183)	4	MSIA 0316
12.030 (306)	4.800 (122)	4.800 (122)	9.600 (244)	6	MSIA 0320
14.430 (367)	4.800 (122)	7.200 (183)	12.000 (305)	6	MSIA 0324
16.830 (427)	7.200 (183)	7.200 (183)	14.400 (366)	6	MSIA 0325

DIMENSIONS IN INCHES AND (MILLIMETERS)
MATERIAL: 0.125 (3.2) ALUMINUM
FINISH: ALODINE TREATMENT

Fig. 8 — MSIA 0300 series rear panels.

Industrial Chassis Series



A	B	C	D	E	F	LENGTH	PART NO.
—	—	—	—	—	—	2.400	MSIA 0404
2.400	—	—	—	—	—	4.800	MSIA 0408
2.400	4.800	—	—	—	—	7.200	MSIA 0412
2.400	4.800	7.200	—	—	—	9.600	MSIA 0416
2.400	4.800	7.200	9.600	—	—	12.000	MSIA 0420
2.400	4.800	7.200	9.600	12.000	—	14.400	MSIA 0424
2.400	4.800	7.200	9.600	12.000	14.400	16.800	MSIA 0425

CONVERSION OF INCHES TO MILLIMETERS:
2.400 (61); 4.800 (122); 7.200 (183); 9.600 (244);
12.000 (305); 14.400 (366); 16.800 (427)

Fig. 9 — MSIA 0400 series front panel guards.

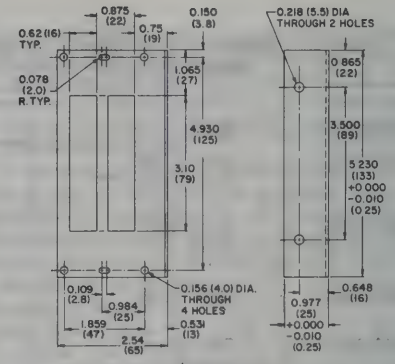


Fig. 10 — MSIA 06 mounting angle brackets.

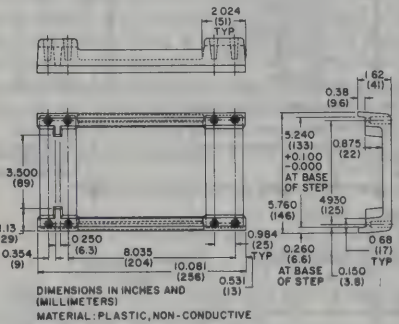


Fig. 11 — MSIA 07 end bezels.

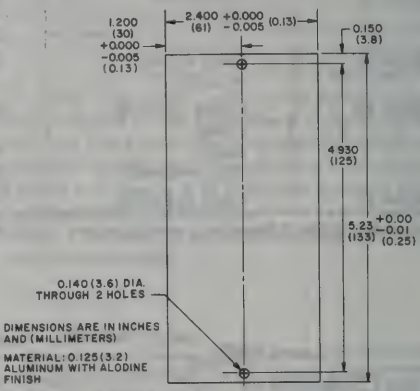

1.200 (30) +0.000 -0.005 (0.13)
2.400 +0.000 (61) -0.005 (0.13)
0.150 (3.8)
4.930 (125)
5.23 +0.00 (133) -0.01 (0.25)
0.140 (3.6) DIA. THROUGH 2 HOLES
DIMENSIONS ARE IN INCHES AND (MILLIMETERS)
MATERIAL: 0.125 (3.2) ALUMINUM WITH ALODINE FINISH

Fig. 12 — MSIA 08 4-card front panel.

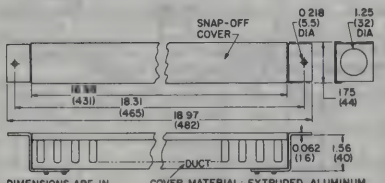


Fig. 13 — MSIA 10 cable conduit.

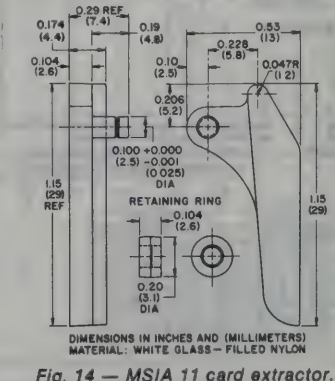


Fig. 14 — MSIA 11 card extractor.

Industrial Chassis Series

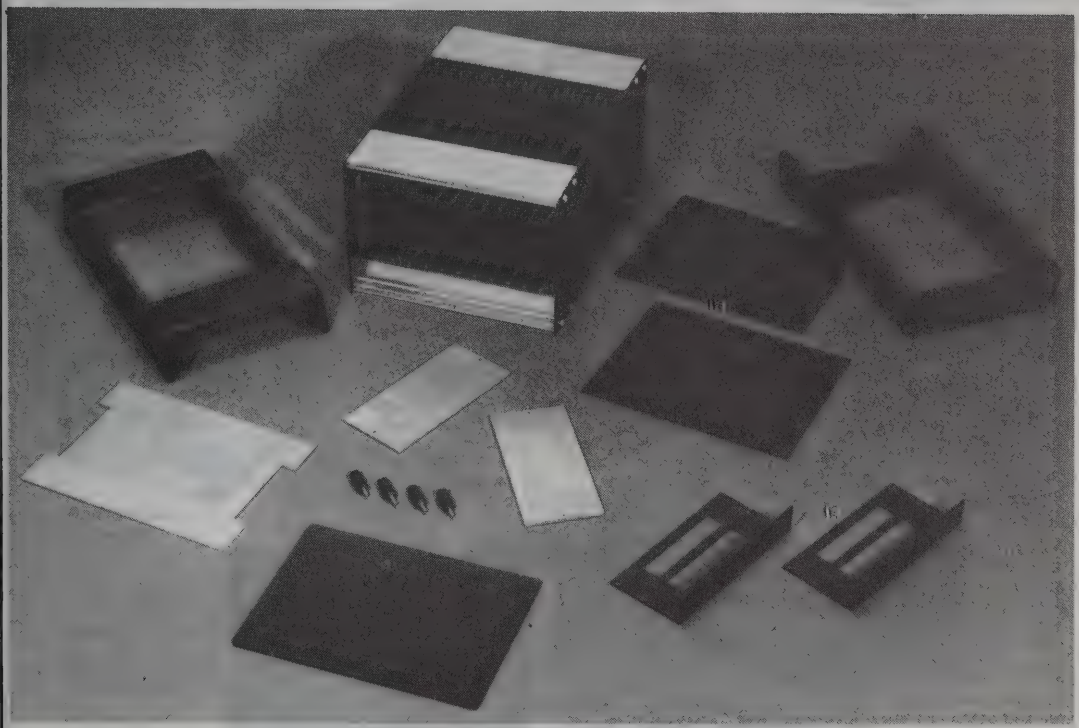


Photo F — Standard 12-card chassis MSI 812 with available accessories identified with call outs.

Optional Plug-In Modules

The **RCA Microboard I/O Module Card MSIM 20** mounts in a 4-slot segment of the Industrial Chassis Series and has a mating 4-slot cover with barrier strips for making power connections. The card mounts up to 8 industry standard optically isolated power modules in any mix of AC or DC, input or output signals. LED's mounted on the front panel provide a visual indication of channel activity.

The **RCA Industrial Microboard Power Supplies MSIM 40 and MSIM 40E** are self-contained front-access switching supplies that plug into any RCA Industrial Series Chassis. They occupy 4 card slots and are complete with power cord, circuit breaker, switch, and power-on light. Operate with either 110 or 220 volts AC and provide logic (5 volts) and analog (+/-15 volts) voltages. They feature a power-down circuit for detecting impending power supply loss.

Industrial Chassis Series

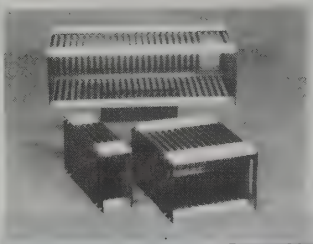


Photo G — Three representative standard chassis. Shown are MSI 825, MSI 812, and MSI 804.

Photo L — Interior of standard 4-card chassis MSI 804. Left side panel is removed to display interior card guides and backplane.

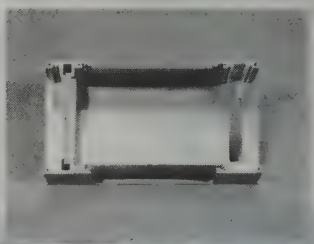
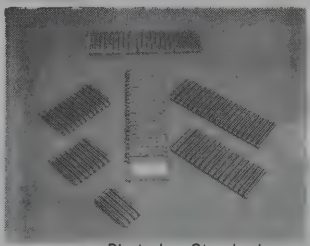


Photo H — MSI 8000 series of backplanes and connectors. Shown are MSI 8004, MSI 8008, MSI 8012, MSI 8016, MSI 8020, MSI 8024, and MSI 8025.



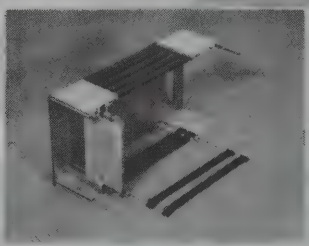


Photo M — Standard 4-card chassis MSI 804 disassembled to show relationship of parts.

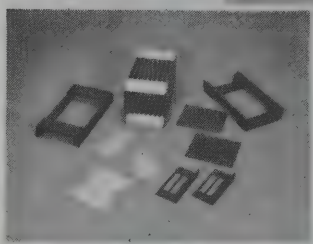


Photo I — Standard 12-card chassis MSI 812 with optional mounting angle brackets in place for flush mounting. Other optional accessories shown are the solid and perforated top and bottom covers, a solid rear panel, a front panel guard with 4 standoffs, and two end bezels (handles).

Photo N — Standard 16-card chassis MSI 816 in typical desk-top configuration. Optional end bezels are added and left side panel is removed to provide access to PROM Programmer module in end position.

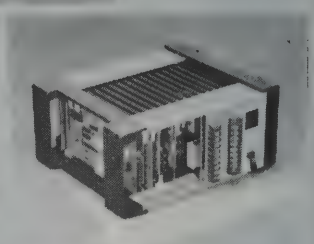


Photo J — Standard 12-card chassis MSI 812 with slotted side panels removed and optional end bezels mounted in place. Optional front panel guard with standoffs, solid and perforated top and bottom covers, and mounting angle brackets are shown unmounted.

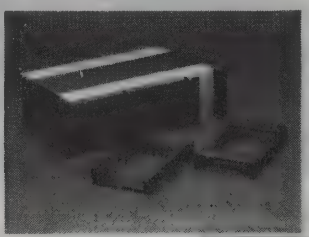


Photo O — Deluxe 25-card chassis MSI 8825 showing all supplied components.

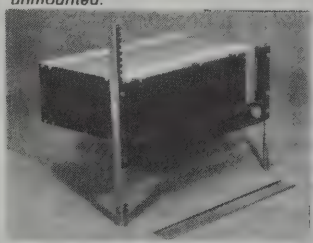
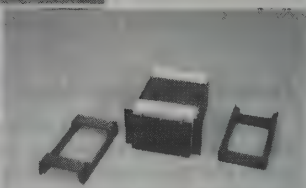
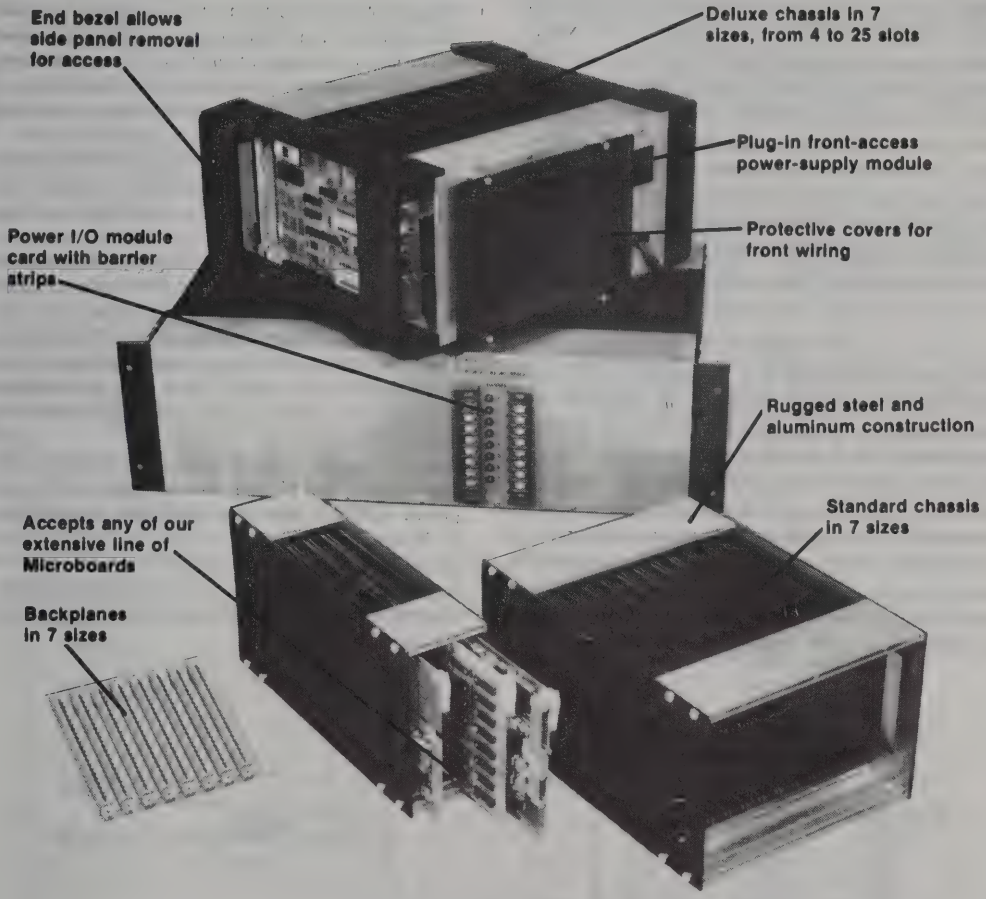


Photo K — Deluxe 25-card chassis MSI 8825 and cable conduit MSIA 10 with cover removed mounted on simulated 19-inch rack.

Photo P — Deluxe 16-card chassis MSI 8816 showing all supplied components.



Industrial Chassis Series


End bezel allows side panel removal for access
Deluxe chassis in 7 sizes, from 4 to 25 slots
Plug-in front-access power-supply module
Protective covers for front wiring
Power I/O module card with barrier strips
Rugged steel and aluminum construction
Standard chassis in 7 sizes
Accepts any of our extensive line of Microboards
Backplanes in 7 sizes

MSIM 20
Power I/O Interface

The MSIM 20 Power I/O Interface provides a rugged, compact, and extremely flexible way to interface power input or output signals to a Microboard computer system. The MSIM 20 accepts eight industry-standard optically isolated interface modules in any mix of input or output and provides barrier strips with captive clamps for wiring connections. The MSIM 20 occupies only 2.4 inches of front panel space (4 board slots) on an RCA Industrial Chassis and is firmly secured to the chassis. It has eight status LED's visible from the front and eight clip-mounted fuses inside.

The direction, input or output, of each channel is determined only by the module that is plugged in; no changes of any kind are required on the MSIM 20. The status of all channels can be read at any time. A versatile interrupt circuit is provided that senses a change of state of any or all channels. The interrupt mask is set under software control. I/O addresses and flag assignments are set by push-on links; no cutting or soldering is required.

All CMOS circuitry is employed, resulting in high noise immunity, a wide (-40 to +85° C) operating range, and low power consumption. The MSIM 20 is compatible with the broad line of RCA Microboards.

Features

- **Flexible:** Accepts eight channels of industry standard I/O modules in any combination of input or output, AC or DC; no changes of any kind are required. Interfaces with any of the broad line of RCA Microboards.
- **Powerful:** Controls eight channels of up to 3A, 240 V AC each.
- **Rugged:** 1/8" thick aluminum front panel mounts barrier strips with captive screw clamp connections: takes wire sizes up to #12. Operates over a wide temperature range, -40 to +85° C.
- **Compact:** Takes only 2.4" of front panel space 5.25" high, mounted in a MSI 800 or 8800 series chassis.
- **Convenient:** Wiring trough (MSIA 10) and protective see-through front panel guards (MSIA 400 series) are available (See RCA Microboard Industrial Chassis Series, publication MB-8). Fuses (clip mounted) and I/O modules (socketed) may be changed without unwiring the front panel.
- **Easy to Program:** I/O address set by a few links. Standard Microboard I/O conventions apply and are supported in several high-level languages such as Pascal, PLM, and BASIC.
- **Versatile Interrupts:** Any channel may be unmasked (under program control) to give an interrupt when it changes state. Interrupts are automatically reset when the board is read.

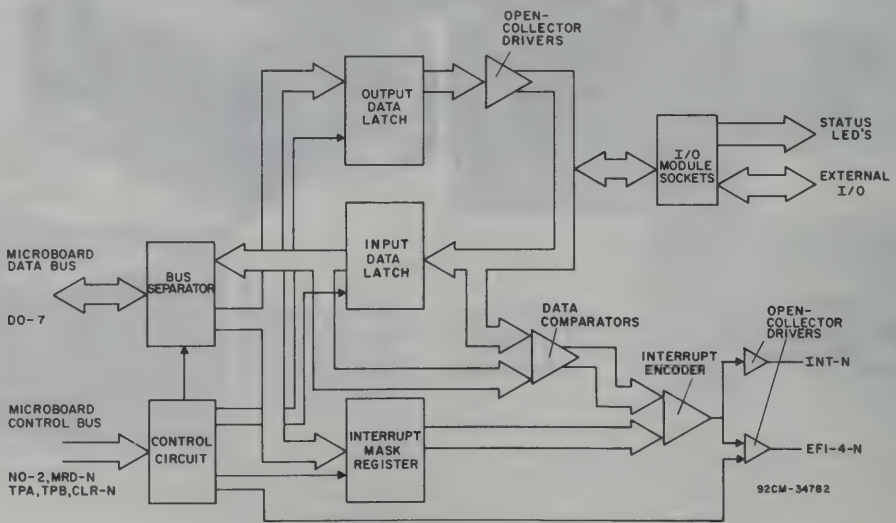


Fig. 1 - Block diagram of MSIM 20 Power I/O Interface.

Specifications:

Operating Temperature Range:
-40°C to +85°C
Drive Current:
(Current available to drive I/O module.)
Sink (on drive): 14 mA min.
Source (off leakage): 20 μA max.
Drive Voltage:
(Voltage available to drive I/O module.)
3 V min. (nominal 5-V supply; includes drop across status-indicator LED)
Input Impedance:
3.3-kilohm pullup to 5-volt supply
Input Threshold:
"0" input: 1.5 V max.
"1" input: 3.5 V min.
Voltage Requirements:
+ 5 volts ± 10 %
Current Requirements:
See discussion under system power requirements.
Dimensions:
See Fig. 2
Fusing:
(8 fuses provided in spring clips)
4 A; 250 V rating, 5 X 20 mm
Littlefuse No. 212 004,
Bussman No. GMA4, or equivalent
Isolation:
1.5 KV rms AC minimum, input (output) to logic or channel to channel
Wire Capacity:
#12 - #22 AWG
Wiring Connections:
Two barrier blocks with 8 captive clamps each
Weight:
11 ounces (312 grams) with no modules mounted; modules weight approximately 1.25 ounces (35 grams) each.

Introduction

The MSIM 20 Power I/O Interface consists of two sections: (1) a logic/power board that plugs into a Microboard backplane and a (2) front panel assembly that mounts to the front of any Microboard Industrial Chassis (MSI 804 - 825 or MSI 8804 - 8825). The two parts plug together with heavy right-angle connectors.

The **logic/power board** contains the interface between the Microboard backplane and the power I/O modules, as well as interrupt-generating logic. Spring sockets and press in nuts are provided to mount up to eight modules. Fuses (5 x 20 mm) are provided mounted in spring clips.

The **front panel assembly** holds two eight-position barrier strips for external wiring and eight LED'S driven by the modules. It mounts in place of a MSIA 08 four-card

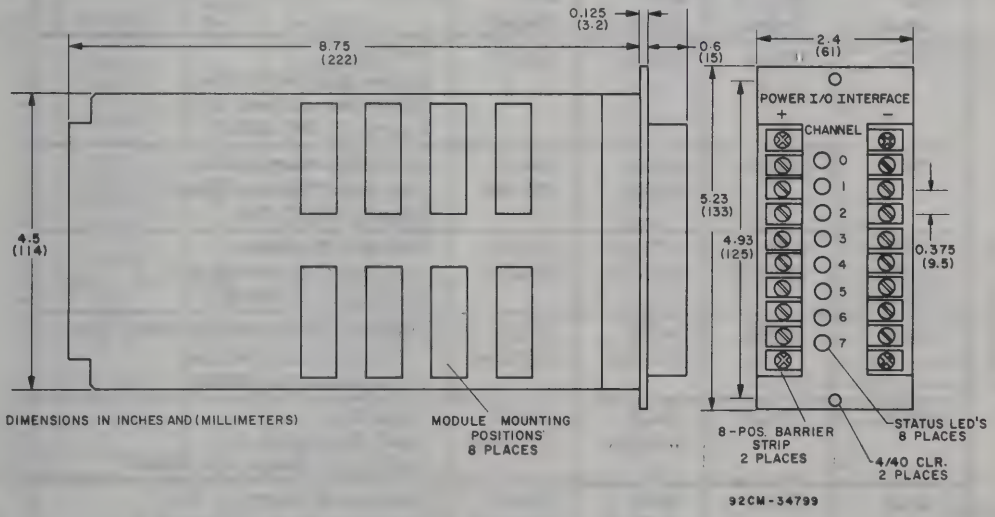


Fig. 2 - Dimensions of MSIM 20 Power I/O Interface.

MSIM 20

front panel to the chassis front extrusions. The barrier strips are marked channels 0 - 7 (corresponding to bit positions 0 - 7), and + and - are indicated for use when DC modules are installed.

RCA does not supply the power modules for use in the MSIM 20. See Table I for a representative list of functionally equivalent modules that should work with the MSIM 20. Fig. 3 gives the dimensions for the module mounting positions.

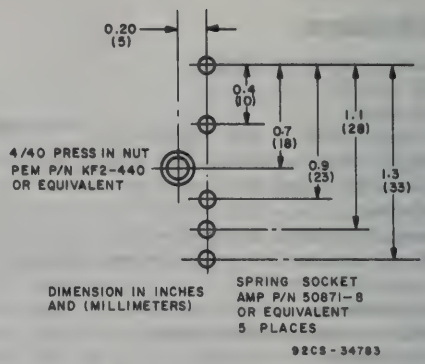


Fig. 3 - Dimensions of MSIM 20 module mounting positions.

Microboard Backplane

The Microboard Backplane consists of a 44-pin bus that is common to all sockets. Table II gives assignments for the backplane interface with the signals that are of interest to the MSIM 20 marked with an asterisk (*). Refer to published data on the CDP1802A microprocessor (File No. 1305) or to the **User Manual For the CDP1802 COSMAC Microprocessor,** MPM-201, for detailed information on CDP1802 bus signals. Following is a brief discussion of the signals that apply to the MSIM 20.

DB0-DB7: The 8 bit bidirectional bus through which input or output data is passed between the Microboard system and the MSIM 20. Bit 0 through bit 7 correspond to channels 0 - 7. They are driven by three-state drivers.

N0-N2: The three I/O address lines from the microprocessor used to indicate that an input or output is in progress and to which address (1 through 7).

Table I - Industry Modules that Mount in the MSIM 20 Power I/O Interface

Module Number				Vendor Name and Address
DC Input	DC Output	AC Input	AC Output	
IDC5	ODC5	IAC5	OAC5	AMF Inc. (Potter & Brumfeld Div.) 200 Richland Creek Drive Princeton, Ind. 47671
IDC5	ODC5	IAC5 IAC5A	OAC5 OAC5A	GORDOS Arkansas Inc. 1000 North Second Street Rogers, Ark. 72756
IDC-01 IDC-11 IDC-21	ODC-01 ODC-11	IAC-01 IAC-11	OAC-01 OAC-11	Guardian California 4050 West Spencer Street Torrance, Cal. 90503
IDC5	ODC5	IAC5 IAC5-A	OAC5 OAC5-A	International Rectifier (Crydom Div.) 1521 East Grand Avenue El Segundo, Cal. 90245
IDC5	ODC5	IAC5 IAC5-A	OAC5 OAC5-A	Opto 22 15461 Springdale St. Huntington Beach, Cal. 92649
IDC5	ODC5	IAC5 IAC5-A	OAC5 OAC5-A	Preferred Electronics, Inc. Main Line Drive, P.O.Box 954 Westfield, Mass. 01086

MSIM 20

MRD: When low, MRD indicates a read from memory. If combined with active "N" lines, an output is in progress. (The CDP1802 transfers data between I/O and memory.) If high, combined with active "N" lines, an input is in progress. MRD originates at the microprocessor.

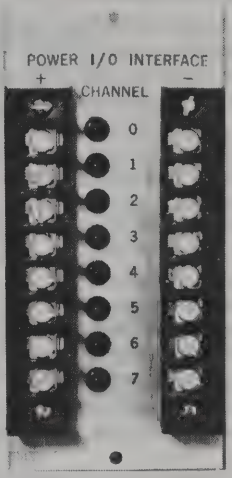
TPA,TPB: An input or output cycle starts at the falling edge of TPA and ends at the falling edge of TPB. It is during this window that "N" lines, MRD, and memory addresses are guaranteed stable. These lines also originate at the microprocessor.

EF1-EF4: These are four flag lines that may be sampled by the microprocessor. They are pulled high by resistors at the microprocessor and are pulled low by "open collector" drivers on I/O boards.

INT: This line, when pulled low, forces the microprocessor to jump to a specific program. It is also an "open collector" line, and it may be disabled internally under software control.

CLEAR: This line is an external input that, when low, resets boards to a known state.

+5V,GND: These lines are the normal system supplies.



Front panel showing barrier strips and LED's.

Table II - Pin Terminals and Signals for the RCA Microboard Universal Backplane

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
1	DMAI-N	In	DMA Input Request	A	TPA-P *	Out	System Timing Pulse 1
2	DMAO-N	In	DMA Output	B	TPB-P *	Out	System Timing Pulse 2
3	RNU-P	—	Run Utility Request	C	DB0-P *	In/Out	Data Bus
4	INT-N *	In	Interrupt Request	D	DB1-P *	In/Out	Data Bus
5	MRD-N *	Out	Memory Read	E	DB2-P *	In/Out	Data Bus
6	Q-P	Out	Programmed Output Latch	F	DB3-P *	In/Out	Data Bus
7	SC0-P	Out	State Code	H	DB4-P *	In/Out	Data Bus
8	SC1-P	Out	State Code	J	DB5-P *	In/Out	Data Bus
9	CLEAR-N *	In	Clear-Mode Request	K	DB6-P *	In/Out	Data Bus
10	WAIT-N	In	Wait-Mode Request	L	DB7-P *	In/Out	Data Bus
11	−15V	—	Auxiliary Power	M	A0-P	Out	Multiplexed Address Bus
12	SPARE	—	Not Assigned	N	A1-P	Out	Multiplexed Address Bus
13	CLOCK OUT	Out	Clock from CPU Osc.	P	A2-P	Out	Multiplexed Address Bus
14	N0-P *	Out	I/O Primary Address	R	A3-P	Out	Multiplexed Address Bus
15	N1-P *	Out	I/O Primary Address	S	A4-P	Out	Multiplexed Address Bus
16	N2-P *	Out	I/O Primary Address	T	A5-P	Out	Multiplexed Address Bus
17	EF1-N *	In	External Flag	U	A6-P	Out	Multiplexed Address Bus
18	EF2-N *	In	External Flag	V	A7-P	Out	Multiplexed Address Bus
19	EF3-N *	In	External Flag	W	MWR-N	Out	Memory Write Pulse
20	+15V	—	Auxiliary Power	X	EF4-N *	In	External Flag
21	+5 V *	In	+5 V dc	Y	+5 V *	In	+5 V dc
22	GND *	In	Digital Ground	Z	GND *	In	Digital Ground

92CS-34444

Note: Signal flow direction is relative to CPU.
Signals marked with an asterisk (*) are used on the MSIM 20.

MSIM 20

Setting I/O Addresses

There are seven possible input or output addresses on a CDP1802A microprocessor. In order to expand to a larger system, a two-level select addressing scheme has been adapted for RCA Microboards. The "OUT 1" (61) instruction has been reserved for outputting an 8-bit I/O address. I/O boards latch and compare that address to that set by links on each board. If they match, they are then free to respond to the remaining I/O instructions (62-67 or 6A-6F). Note that the "INP 1" (69) instruction is reserved so the processor can read back (where implemented) the last 61 instruction.

The eight bits that are output during a 61 instruction are divided into two groups of four. The four lower bits (D0 - D3) are usually used to select system functions such as a terminal or disk and are decoded linearly. The four upper bits (D4 - D7) are used for other I/O (such as this board) and are decoded in a binary manner (16 combinations).

LK1 is used to select the two-level address of the MSIM 20. A stick of push-on connectors is supplied (Amp P/N 531220-3 or equivalent) for setting the address and other links. Note that the end of the connector towards the break-off stick is the end to insert over the pins. See Table III for a list of two-level addresses and the corresponding LK1 connections. The low order bits, bits 0 - 3, are ignored. See Fig. 4 for link locations.

Note that the number of LK1 links installed affects standby current See discussion under system power requirements. Note also that TP1 shown on Fig. 4 is the output of the two-level select circuit. It will be high if the MSIM 20 is selected.

Table III — Two Level I/O Link Assignments for Link LK1

Two Level Address	LK1 Connector Pins			
	1-8	2-7	3-6	4-5
FX	C	C	C	C
EX	C	C	C	O
DX	C	C	O	C
CX	C	C	O	O
BX	C	O	C	C
AX	C	O	C	O
9X	C	O	O	C
8X	C	O	O	O
7X	O	C	C	C
6X	O	C	C	O
5X	O	C	O	C
4X	O	C	O	O
3X	O	O	C	C
2X	O	O	C	O
1X	O	O	O	C
0X	O	O	O	O

Notes: X = Don't Care, C = Closed, O = Open

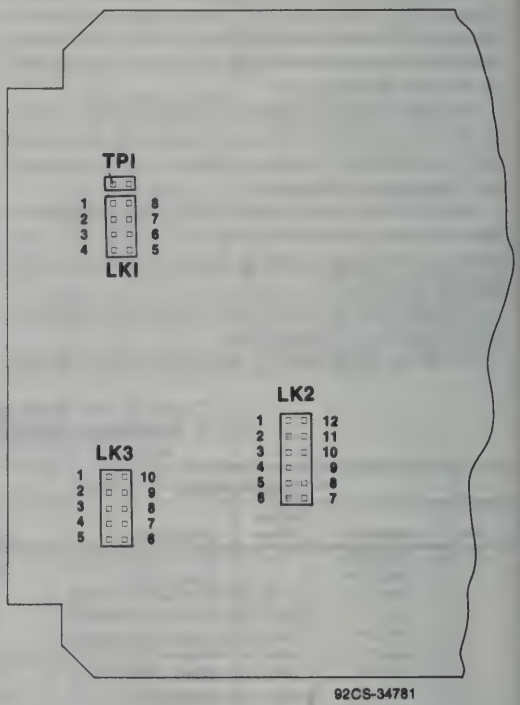


Fig. 4 - Location of links LK1, LK2, LK3, and Test Point TP1.

Once the specific MSIM 20 has been selected, there are six more output (62 - 67) and six more input (6A - 6F) addresses available for use. Link LK2 sets the choice of these addresses.

The MSIM 20 has two output ports: the main output port and the interrupt mask port (discussed later). It has one input port; this port occupies the same address as set for the main output port. If both the main and interrupt ports are to be used, three different pairs of addresses can be set on MSIM 20's occupying the same two-level select group. See Table IV for LK2 connections for this mode.

Table IV - I/O Address Assignments for Link LK2

LK2 Pin Connections	Corresponding I /O Instruction		
	Main Input	Main Output	Interrupt Mask
1 - 12	INP 2 (6A)	OUT 2 (62)	-
2 - 11	-	-	OUT 3 (63)
3 - 10	INP 4 (6C)	OUT 4 (64)	
4 - 9	-	-	OUT 5 (65)
5 - 8	INP 6 (6E)	OUT 6 (66)	
6 - 7	-	-	OUT 7 (67)

Note that the INP 3 (6B), INP 5 (6D), and INP 7 (6F) instructions are not used. If desired, they may be used by other boards occupying the same two-level select group.

If interrupts are not to be used on the MSIM 20, the three Interrupt Mask addresses can be used instead for the Main Input/Output Ports by linking the desired address (3, 5, or 7) and placing a second link across any adjacent higher-numbered LK2 positions (pins 7-8, 8-9, 9-10, etc). Fig. 5 demonstrates LK2 set for a main I /O address of 5. It is important to make sure that no LK3 links are in place because the interrupt circuit will still be active.

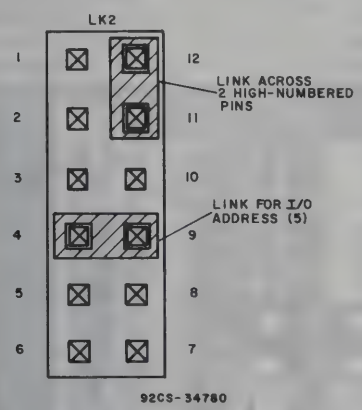


Fig. 5 - Setting of Link LK2 for I/O address of 5.

Setting Flag and Interrupt Links

If the interrupt circuit is to be used, LK3 pins 1 - 10 have to be connected. The interrupt line is an "open collector" line with a pull-up resistor on the CPU board (CDP18S601 - CDP18S610). Interrupts are active low and are given whether the board is two-level selected or not. In conjunction with the interrupt line, one of four flag lines, EF1 - EF4, can also be pulled low by the MSIM 20. These lines, also "open collector," are disabled when the MSIM 20 is not selected. By using a different flag line for each board that is in the same two-level group, the CPU can determine which board gave the interrupt. This subject is discussed further under "Interrupt Control." Table V gives the flag assignments for link LK3.

Table V - Flag Line Connections for Link LK3

LK3 Pin Connections	Flags Enabled
1 - 10	Interrupt
2 - 9	EF1
3 - 8	EF2
4 - 7	EF3
5 - 6	EF4

Mounting and Interfacing I/O Modules

As mentioned earlier, the MSIM 20 accepts any mix of industry-standard isolated I/O modules. In small systems it is likely that input and output modules will be mounted on the same MSIM 20. The modules are simply plugged into the spring socket locations on the board, and screwed down with 4/40 hardware normally supplied with the modules.

CAUTION: Some brands of I/O modules have plastic ears that keep the base from sitting flush with the board. Tightening the mounting screws excessively will deform the board and possibly damage it.

Modules are color coded by function as follows:

White: DC Input
Red: DC Output
Yellow: AC Input
Black: AC Output

The MSIM 20 is preprinted with a white dot at each I/O module location. Red, yellow, and black dots are

MSIM 20

supplied as an aid in marking each socket for the type relay used.

The front panel holds two 8-position barrier blocks marked channels 0 - 7. The left block (marked "+") connects to pin 1 of module positions 0 - 7 on the main board. The right block (marked "-") connects through fuse positions 0 - 7 to pin 2 of module positions 0 - 7. The polarities correspond to those of DC modules and have no meaning for AC modules.

If it is desired to "common up" one side of several modules, jumper strips, part No. J6-N (where N is the number of positions to be shorted together), are available from:

RDI / Reed Devices Inc.
525 Randy Road
Carol Stream, Ill. 60187

The front panel LED'S will be lit if the corresponding input or output channel is on. If an output, a lit LED guarantees that continuity has been established through the internal optical isolator diode of the module, but it does not guarantee that the output circuit is live.

Fuses are clip mounted and are in series with pin 2 of each module. Four-ampere, 250-volt, 5 X 20 mm fuses are provided. A small screwdriver may be inserted between the end of a fuse and its clip to pop it out.

NEVER WORK ON A BOARD WHILE EXTERNAL CONNECTIONS ARE LIVE.

Mounting the MSIM 20

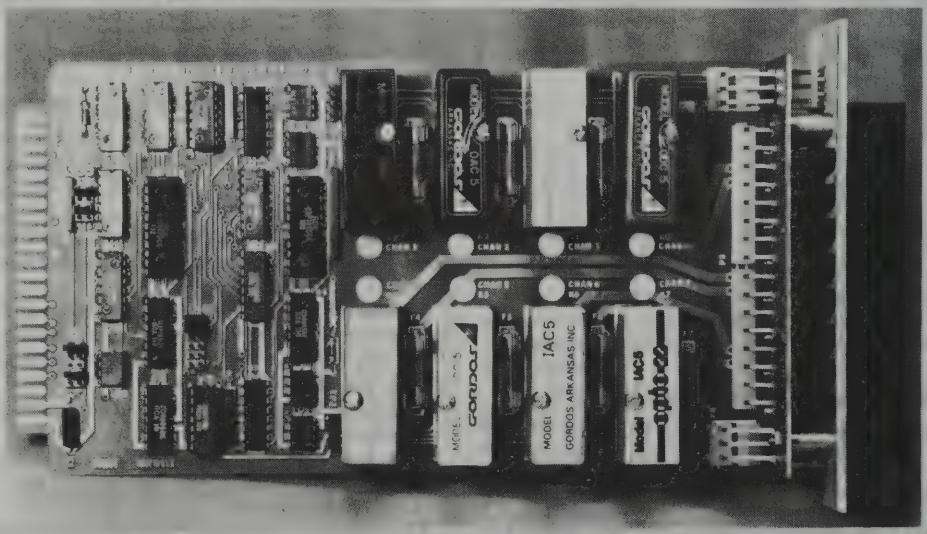
The MSIM 20 is only to be used in a MSI 800 series standard or a MSI 8800 series deluxe Industrial Chassis. It replaces exactly the MSIA 08 blank front panel (standard on the MSI 8800 series chassis), occupying four card slots. The MSIM 20 plugs into the second connector from the right of that space.

CAUTION: Although the rightmost slot will appear free, it should be left free for electrical clearance. The I/O module mounting spring sockets could touch conductive parts (such as crystal cases) of any board inserted there, causing an extreme shock hazard. (With extreme care, a CDP18S604B CPU Microboard can be mounted in this slot, thus allowing a complete eight-channel low-cost control system to fit into a four-card chassis such as the MSI 8804.)

After the front panel of the MSIM 20 is slid into place, it should be secured to the front of the chassis with two 4/40 by 3/8 inch screws. Solid or stranded wires, with or without terminations, can be secured under the captive clamps of the front barrier strips.

CAUTION: It is possible for finely stranded wire to "poke through" small slits in the rear of the barrier strips; care should be taken.

A MSIA 0400 series front panel guard should be used to safeguard the front panel wiring. For 19-inch rack mount applications, a MSIA 10 cable conduit guides and



Representative mix of I/O modules mounted on MSIM 20 Power I/O Interface.

protects wiring to the chassis. See publication **RCA Microboard Industrial Chassis Series,** MB-8, for details.

It is possible, if necessary for fuse or module replacement, to gain access to the board once the front wiring is in place. The wiring to the front panel must not be live and the Microboard system power must be off. The two 4/40 screws securing the front panel should be removed, and the board pulled slightly out of the chassis. With the board grasped securely, the front panel can be pulled off and swung down out of the way. Care must be taken when reconnecting the two parts of the board that the right-angle connectors are inserted properly into their holes; forcing an improperly mated connector will cause damage.

System Power Requirements

The MSIM 20 only requires + 5 volts from the Microboard Universal Backplane. The current required will vary according to how many and what types of active I/O modules are in place. Each "on" output module draws 10 to 12 mA from the logic supply; each "on" input module needs 4 to 6 mA.

The interface circuitry also requires some current. Each LK1 link inserted draws 0.5 mA. In addition, the circuitry typically draws 1 mA when selected, and 0.3 mA when not. With the system in reset (no active backplane signals), no LK1 links, and no "on" input signals, current consumption should drop below 0.1 mA.

Temperature Considerations

Although the MSIM 20 board is rated for a -40 to +85° C operating temperature range, most I/O modules do not meet this specification. Consult the manufacturer for temperature range and derating curves.

The ambient temperature rise inside a chassis is greatly affected by its configuration. A "worst case" test was done to find the maximum expected temperature rise. Eight AC output modules were placed on a MSIM 20 with each carrying 2.5 A continuously. The MSIM 20 was mounted in a MSI 8816 Industrial Chassis with solid top and bottom covers, and a Microboard was placed in the next slot to the left to block internal air circulation. The chassis was mounted on a flat surface. The temperature rise measured was 40° C. With MSIA 0216 perforated covers installed and the chassis raised to provide clearance underneath, the rise measured was 25° C. Placing the chassis vertically so that the MSIM 20 was horizontal increased this rise to 32° C.

Controlling I/O Modules

Before an input module can be read or an output module turned on or off, the MSIM 20 has to be selected (two-level select circuit). An OUT 1 instruction with the upper 4 bits of data matching the address set by LK1 will accomplish this selection. The other INP or OUT instructions as set by LK2 now apply.

Note that if two-level select is not desired (as, perhaps, for a small system), LK1 may be set for an address of 0. When the system is reset, either from power on or manually, the MSIM 20 is selected automatically. The OUT 1 instruction must still be avoided.

If output modules are in place, a data byte written with the selected output instruction controls all channels simultaneously. Every bit position containing a "1" will be on, and those containing a "0", off. The data is latched, and de-selecting the MSIM 20 will not then affect the channels. Note that a system reset signal will turn all output modules off.

If input modules are in place and the board selected, all channels are read simultaneously with the selected input instruction. Again, a "1" in a bit position indicates an "on" channel, and a "0", "off."

If a mix of input and output modules is placed on a board, they may be controlled or read in the same manner. The only constraint is to not write a "1" in a bit position that contains an input module: it will mask the input and show a "1" when read.

An input instruction may be used whether or not there are input modules present. It will show, on channels that are outputs or that have no modules at all, the last bit written to that channel. This feature can be a useful aid to software operation. Fig. 6 diagrams the module interface circuitry.

Interrupt Control

Interrupts can be generated by any selected input on the board changing state in either direction (On to Off, or Off to On). The interrupt mask must first be set to enable the desired channels. The board must be two-level enabled (as in the previous discussion), and a data byte written to the Interrupt Mask with the output instruction set by LK2. A "1" in any bit position enables the corresponding channel to generate interrupts. (After reset, the mask is all 0's.) LK3, pins 1 - 10, must also be in place.

Whenever a board is read, an internal latch stores the state of all channels. If an interrupt-enabled channel then changes state, an (open collector) interrupt signal is ap-

MSIM 20

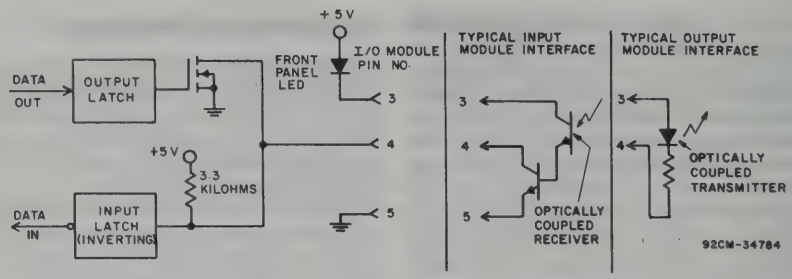


Fig. 6 - Diagrams of the module interface circuitry.

plied to the backplane. (Interrupts are not disabled with two-level select.) The interrupt signal remains until the board is read again (thus loading the latch with the new state), or until the affecting channel resorts back to its former state.

The latch circuit operates early in the read cycle, and the data read by the CPU is actually the output of the latch. This arrangement precludes having different data in the latch (upon which interrupts are based) than that input by the CPU.

The interrupt can also be dropped by changing the interrupt mask, but this change does not actually reset the interrupt request. If the bit is enabled again, the interrupt will still be active.

One of the four flag lines, EF1 - EF4, can also be linked to the interrupt circuit. These lines, however, are only enabled when the MSIM 20 is two-level-selected, and they allow the software to determine which MSIM 20 generated the interrupt. If, for instance, three MSIM 20's were in the same two-level group, they could have three separate flag lines linked up. The software would simply enable that group and check which flag line was active. As an alternate method, the MSIM 20's might be placed in different two-level-select groups, but have the same flag hooked up. The software could then enable one group at a time and check the one flag.

CAUTION: On the CDP18S601, 603, 606, or 608 CPU Microboard, EF3 or EF4 (Link Selected) are not conditioned by two-level-select circuitry. The flag in use on that Microboard should be avoided.

As supplied, the MSIM 20 contains two socketed IC's, U11 and U12. These IC's are CD4077BE Exclusive-NOR gates and generate interrupt request bits when a channel changes state in either direction. U11 controls channels 0 - 3, and U12, channels 4 - 7. The bits are then fed to the masking circuitry.

It is possible to change the MSIM 20 so that interrupts are only generated with "On to Off" or "Off to On" transitions. If CD4081BE AND Gates are inserted, only "On to Off" changes will give interrupts; CD4001BE NOR gates accomplish the opposite.

CAUTION: For the above-modified circuitry to work, the selected channels must be "armed". Arming is accomplished by reading the MSIM 20 at the time when the selected channel is in the "relaxed" state; that is, the state from which a change generates an interrupt.

Parts List

C1=22 μF, 15 V
C2,C3=0.1 μF, 50 V

CR1 - CR8=LED, Dialight 559-0101-001, or equivalent

F0 - F7=fuse, 4 A, 250 V, Bussman No. GMA4, Littlefuse No. 212 004, or equivalent

LK1=connector, 8 pin, double row
LK2=connector, 12 pin, double row
LK3=connector, 10 pin, double row

RN1=resistor network, 10 kilohms, 6 pins
RN2,RN3=resistor network, 3.3 kilohms, 6 pins
RN4=resistor network, 22 kilohms, 10 pins

T1,T2=RDI 6WWV-08, or equivalent

TP1=connector, 2 pin, single row
TP2,TP3=connector, 4 pin, single row

U1,U2,U5,U6,U20=CD40107BE
U3,U14=CDP1875CE
U4=CD4013BE
U7,U10=CD40175BE
U8,U9=CDP1856CE
U11,U12=CD4077BE
U13,U16=CD4086BE
U15=CDP1853CE
U17=CD4011UBE
U18=CD4585BE
U19=CD40194BE

MSIM 20

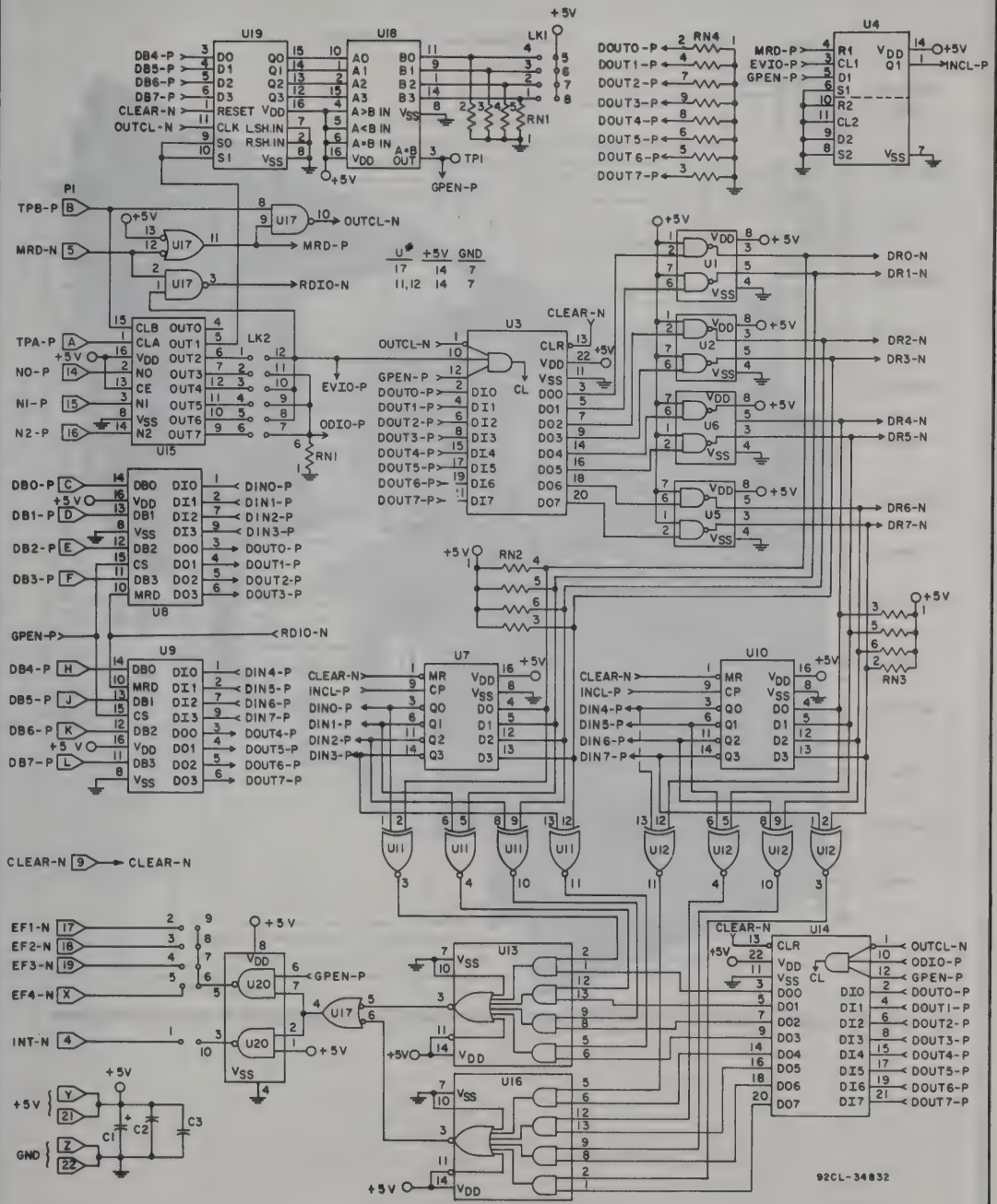


Fig. 7 - Logic diagram of MSIM 20 Power I/O Interface - control section.

MSIM 20

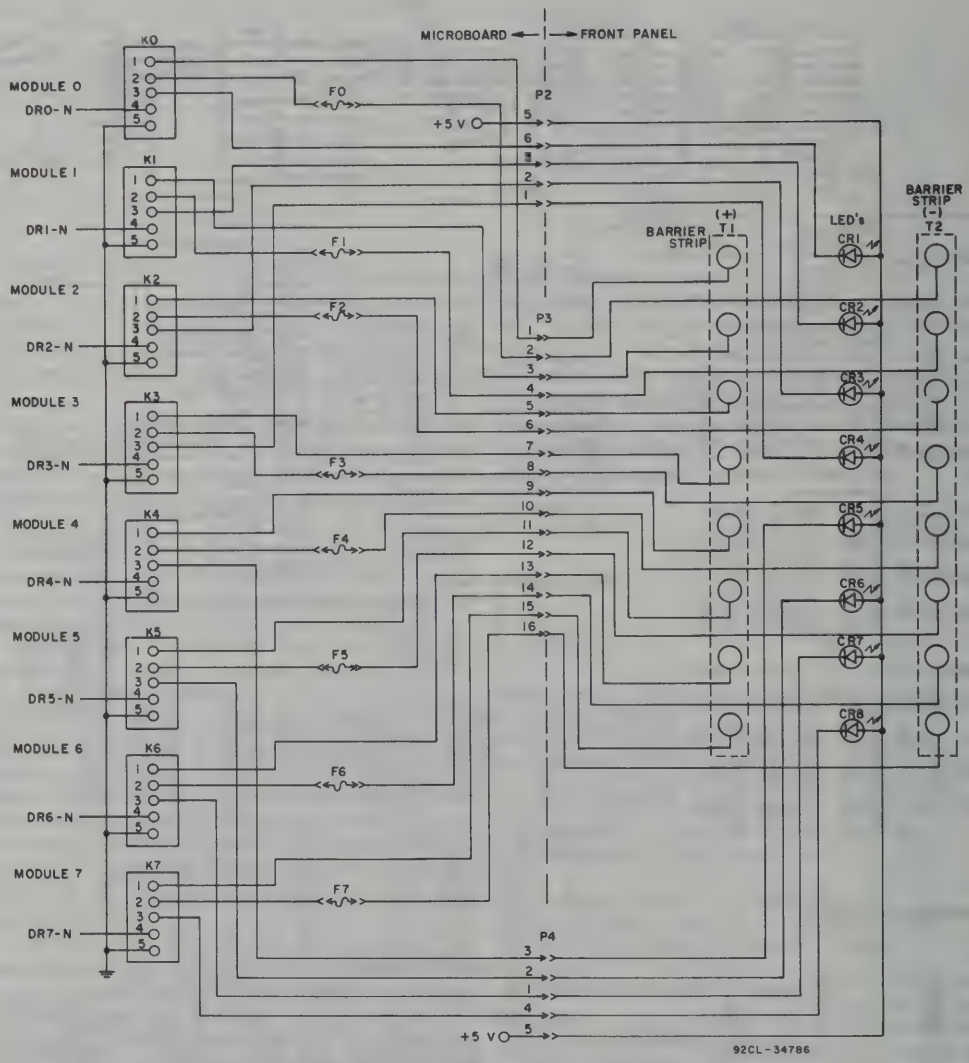
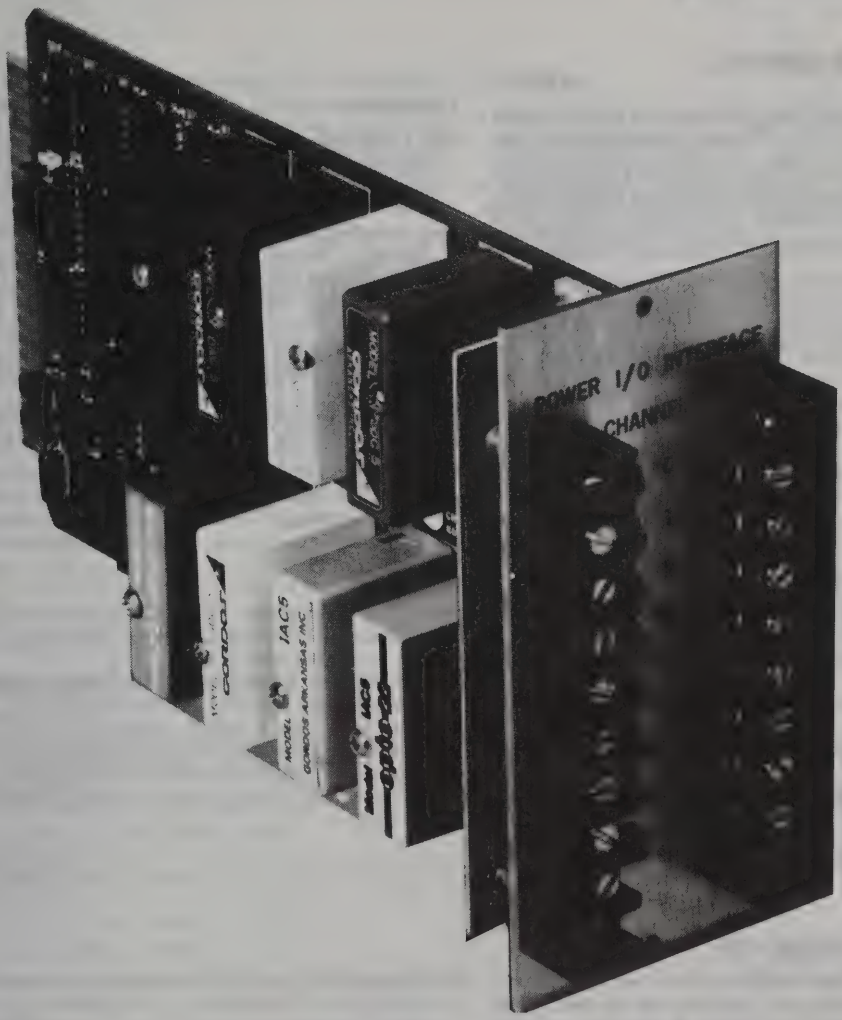


Fig. 8 - Logic diagram of MSIM 20 Power I/O Interface - front panel and module connections.

MSIM 20



Advance Data

MSIM 40, MSIM 40E, MSIM 41, MSIM 41E
Power Supplies for RCA Industrial Microboard Chassis Series

MSIM 40, MSIM 40E

The RCA Industrial Microboard Power Supplies MSIM 40 and MSIM 40E are self-contained switching supplies that plug into any RCA Industrial Series Chassis. They occupy four card slots (2.4 inches of rack space) and are complete with power cord, circuit-breaker switch, and LED pilot light. A front panel RESET/RUN switch and run indicator LED allows system control and monitoring.

The supplies may be strapped to accept either 110-volt or 220-volt AC input, and provide logic (5 volts), and analog (±15 volts) voltages to the RCA Microboard Universal Backplane. Full output is available over a 0-50°C range, with linear derating over the full Microboard operating temperature range (–40 to +85°C).

Impending power loss is detected by the supply, and a logic signal may be used to interrupt the system. This feature provides a way of preserving the machine state or important parameters in battery-backed RAM during a power outage.

Features

Self Contained: Complete with power switch, circuit breaker, line cord, and LED pilot light. RESET/RUN switch and run indicator LED provided for system control.

Easy Installation: Plugs into any four-slot segment on Industrial Microboard Chassis; all connections are made through backplane.

Flexible: Accepts either 110-volt or 220-volt AC input with simple strap change. Provides all logic and analog supply needed for Microboard cards.

Efficient: Uses state-of-the-art switching power supply circuit.

Power Down Detector: Impending supply loss is detected and an interrupt or flags presented to the system backplane.

Specifications

AC Input: Strappable to either 90-132 volts AC or 180-264 volts AC. Frequency range = 47-440 Hz. MSIM 40 prestrapped for 115 volts, MSIM 40 E for 230 volts.

DC Output: On standard Microboard 44-pin connector: +5 V @ 3 A, +15 V @ 1.6A, -15 V @ 0.8A.

Regulation: ±3% over all line load and temperature variations.

Temperature Range: Full output: 0-50°C. Derate linearly to 20% at -40°C and +85°C

Efficiency: > 65% at nominal line and maximum load.

Over-Voltage Protection: 5-volt output only.

Short-Circuit Protection: All outputs protected for indefinite short circuit over 0-50°C range. Momentary short may be applied outside of this range.

Electro-Magnetic Interference (EMI): When mounted in chassis, supply will meet the limits specified in FCC Rule 15 for Class A and B Computing Devices.

Power Fail Circuit: A signal will be available at least 10 ms before loss of regulation due to loss of line voltage. This signal may be strappable to any flag or the Interrupt line.

MSIM 41, MSIM 41E

The MSIM 41 and MSIM 41E are lower power linear supplies for systems not requiring all the features or power capability of the MSIM 40 supplies described above. They mount in a similar manner, with front panel functions consisting of a power switch, fuse holder, line cord, and +5 V status LED. They may be strapped to accept either 115 or 230 volt AC inputs.

Specifications

AC Input: Strappable to either 103-127 volts AC, or 207-253 volts AC. Frequency range=47-440 Hz. MSIM 41 prestrapped for 115 volts, MSIM 41E for 230 volts.

DC Output: On standard Microboard 44-pin connector: +5 V @ 2 A, +15 V @ 0.4 A, –15 V @ 0.4 A. ±15 V outputs adjustable to ±12 V, –15 V output further strappable to –5 V.

Regulation: ±3% over all line, load, and temperature variations.

Tempurature Range: Full output: 0-50°C. Derate linearly to 40% @ 70°C.

Over-Voltage Protection: 5-volt output only.

Short-Circuit Protection: Current limiting and foldback on all outputs.

Advance Data

MSIM 50

RCA Micro Floppy-Disk Drive Module

The RCA MSIM 50 Micro Floppy-Disk Drive Module contains two 3.5-inch disk drives and mounts in a MSI 800 or 8800 Series Industrial Chassis. The module only occupies 8 slots (4.8 inches) of panel space, and is styled to match other Industrial Chassis Modules. A CDP18S651 Microboard Floppy Disk Controller (available separately) completes the interface.

The MSIM 50 Module is powered from the chassis backplane. An MSIM 40 or 40E plug-in power supply (available separately) provides the needed voltages.

Each 3.5-inch disk holds up to 315 Kbytes* of data (formatted, double-density) on 70 tracks. Track-to-track seek time is 15 milliseconds, and the data transfer rate is 500 kilobits per second. The CDP18S651 Controller uses DMA cycles for fast data transfer between the disk and host system. The DMA capability is available from the CPU of any RCA Microboard Computer.

The Module is supported by RCA's MICRODOS disk operating system and related support monitor programs (available separately). The monitor programs are in ROM and enable the user to setup his own data storage system.

Features

- **Compact: Takes only 4.8 inches of panel space; an entire microcomputer system can fit in a medium-size Industrial Chassis. Disks are only 3.5 inches square.**
- **High Capacity: 2 floppy disks store 315 Kbytes* each.**
- **Fast Transfer: Data transfers directly to users memory at 500 kilobits per second.**
- **Convenient: Supported by MICRODOS and related monitor programs. Interfaces through CDP18S651 Floppy Disk Controller. Power is supplied through backplane. No external connections needed.**
- **Low Power: Only 7 watts standby, 15 watts operating (2 drives operating)**

Specifications

Capacity:
315 Kbytes* per drive formatted, double density (70 tracks, 9 sectors/track, 512 bytes/sector)

Transfer Rate:
Double density = 500 kilobits/second
Single density = 250 kilobits/second

Access Time:
Track to Track = 15 ms
Settling Time = 15 ms
Head Load Time = 60 ms
Average Latency = 50 ms

Power Requirements:
+15 V or +12 V, ±5%, 0.8 A typ., 2 A max. start up; +5 V ± 5%, 1.2 A typ., 1.6 A max.

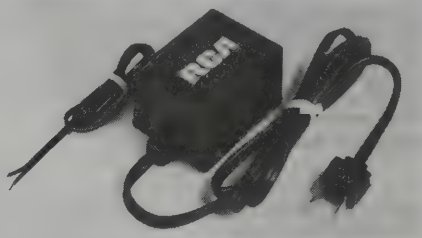
Dimensions:
Occupies 8 slots (4.8 inches) in MSI 800 or 8800 Series Industral Chassis. 9th slot needed for CDP18S651 Floppy Disk Controller.

*Kbyte = 1024 bytes

CDP18S023
CDP18S023V3
Power Converter

The Power Converters CDP18S023 and CDP18S023V3 are lightweight, inexpensive, convenient power supplies especially suitable for use with RCA COSMAC Microboard System modules. The CDP18S023 plugs into any standard 110-volt 50/60-Hz wall outlet and has a regulated output of +5 volts dc ±5% at 600 milliamperes. Its overall dimensions are 2.7 x 2.1 x 1.6 inches (69 x 53 x 41 mm); its weight is 12.5 ounces (354 grams).

The CDP18S023V3 operates with input voltages from 210 to 250 volts, 50 Hz; and provides a regulated output of +5 volts dc ±5% at 600 milliamperes. It is supplied with a standard European-type two-pin molded plug. The CDP18S023V3 over-all dimensions are 5.12 x 2.5 x 2.0 inches (130 x 63.5 x 50.8 mm); its weight is 17 ounces (482 grams).



CDP18S023

CDP18S023V3

CDP18S659

RCA COSMAC Microboard Breadboard

The RCA COSMAC Microboard CDP18S659, a blank module that mates with the Microboard Universal Backplane, provides a high-quality, high-density method for the hand fabrication of prototype or low-production modules for the expansion of a Microboard system. Its hole patterns, printed pads, and voltage runs are designed to maximize the number of integrated circuit locations available and to accommodate all sizes of dual in-line packages as well as discrete components.

An area at the end of the board opposite the backplane connector is arranged to accept a variety of connector types including flat-cable right-angle headers, open-wire right-angle headers, and right-angle delta connectors. When this area is not used for connectors, it may be used for a number of DIP devices. The backplane connector area is labeled with signal names to facilitate breadboarding and testing.

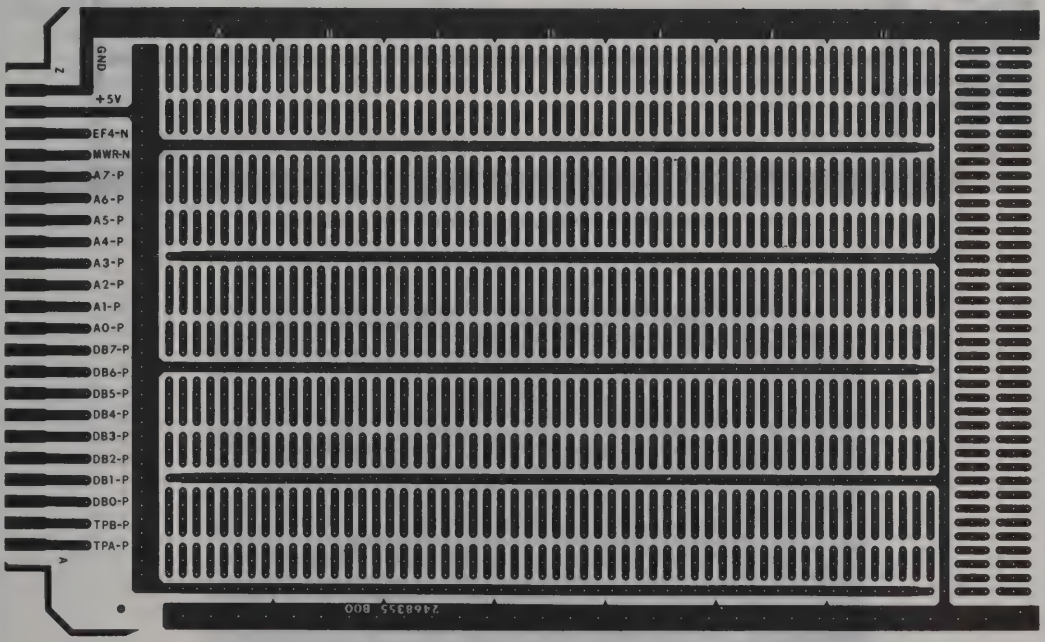
Features

- Up to 40 IC locations
- Accommodates any size DIP
- Mates with Microboard Universal Backplane
- Signal names labeled on connector
- Distributed +5 V and ground connections on both sides of board
- Accepts a variety of connectors for off-board interfacing

Specifications

Size: 4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)

Backplane Connector: edge fingers, 44 pins (dual 22) on 0.156-inch centers



CDP18S659 Microboard Breadboard — solder side

CDP18S659

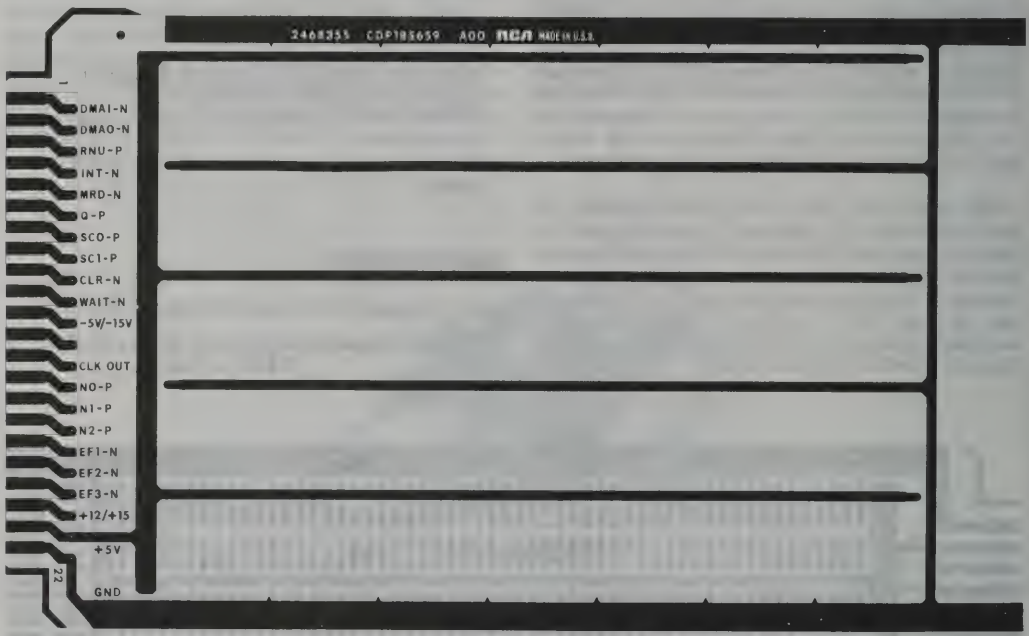
Hole Pattern: 0.100 inch centers

Hole Size: 0.035, +0.003, -0.001 inch

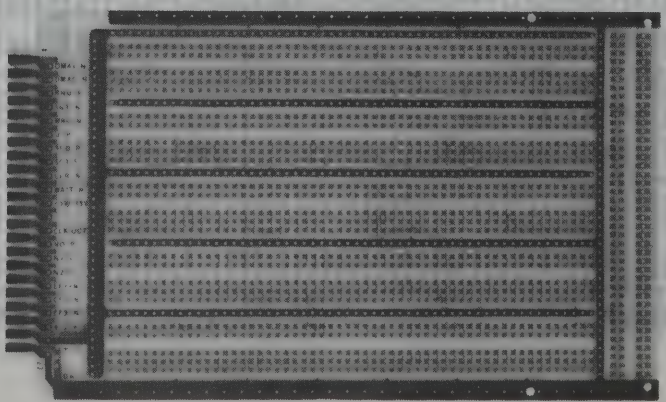
Printed-Circuit Pattern: three- and four-hole solder pads on solder side; ground and +5 V runs on both sides

IC Capacity: up to 40 DIP's of 14 or 16 pins; any mix of DIP sizes

Front Connector: up to 40 dual (80 pin) positions for right-angle headers; 0.100 inch spacing.



CDP18S659 Microboard Breadboard — component side



CDP18S670

RCA COSMAC Microboard 22-Card Chassis With Integral Power Supply*

The RCA CDP18S670 COSMAC Microboard 22-Card Chassis with Integral Power Supply provides compact convenient means for assembling and operating systems comprised of RCA Microboards. The Chassis includes 22 slots with integral card guides mounted on an RCA COSMAC Universal Printed-Circuit Backplane and a triple-output power supply housed in a metal frame and enclosed in a protective metal enclosure. The enclosure is provided with rubber feet as well as holes for vertical mounting. Access holes are provided in the metal frame for the connection of flat cables to either the backplane or to the opposite end of the Microboard modules having additional outboard connectors. The subchassis can be easily removed from the protective metal enclosure for installation in any industry-standard 19-inch computer rack.

The fused power supply provided with the CDP18S670 is a dual-primary, triple-output supply "Power-One Type HTAA-16W." (Manufactured by Power-One Incorporated, Camarillo, Calif., 93010).

The outputs of this supply are --

+5 volts dc at 2A, 5% regulation
-5 volts or -12 volts dc at 0.4A, 5% regulation
+12 volts dc at 0.4A, 5% regulation

The ac input to the supply can be either 105-125 or 210-250 volts, 47-440 Hz. An input-voltage selector is provided to configure the chassis power supply for either 120-volt or 220-volt operation. A representative schematic for the power supply is shown in Fig. 10.

Output voltages for the Microboard Universal Backplane are +5 V dc, +12 V dc, and -5 V dc. The +5 and the -5 volt outputs can be adjusted ±20% by the user. The +12 volt output can be adjusted to any value between +10 and +15 volts. In addition, the -5 volt supply can be changed to provide any voltage between -10 and -15 volts. See section on Power Supply Adjustments.

Features

- **Preprinted Microboard Universal Backplane for 22 cards**
- **19-inch, rack-mountable subchassis 5-1/4 inches high**
- **Subchassis accessible by removal of only 4 screws**
- **Blue metal protective case with control panel**
- **0.6-inch Microboard spacing**
- **Integral card guides**
- **Built-in, triple-voltage fused power supply**
- **Supply provides +5 volts at 2A, +12 volts at 400 mA, -5 volts at 400 mA**
- **Power input adjustable to 120 volts or 220 volts, 50/60 Hz**
- **Power on switch and indicator**
- **Temperature range: 0 to +70° C**

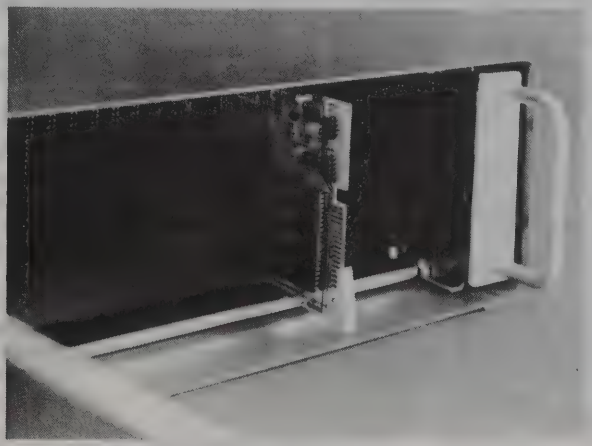


Fig. 1 - Chassis with representative Microboard inserted.

* Refer to the Industrial Chassis Series for a complete series of industrial-grade housings for RCA Microboards.

CDP18S670

Specifications

Backplane:
- 0.062-inch printed-circuit board
- 22 locations for 44-pin connectors
- Universal Microboard Backplane wiring
- Pre-wired power bus (+5 V, +12 V, -5 V) and ground

Card Socket Connectors:
- 44-pin (dual 22) on 0.156-inch centers,
- ELCO Part No. 00-6022-044-451-001, or equivalent
- Integral plastic card guides
- 0.6-inch separation

Power Supply Requirements:
- Input voltage:
  - 105-125 volts AC, 47-440 Hz, 40 watts max
  - 210-250 volts AC, 47-440 Hz, 40 watts max
  - Fuse: 0.5A, SLO-BLO
- Output voltage:
  - +5 volts dc at 2.0A, 5% regulation
  - -5 or -12 volts dc at 0.4A, 5% regulation
  - +12 V dc at 0.4A, 5% regulation
  - Derate from 100% at 0-50°C to 40% at 70°C

Cabling Supplied:
- AC power cord: 7 feet, 6 inches

Dimensions (with Case)
- Width: 19-3/8 inches (492 mm)
- Depth: 12-3/4 inches (324 mm)
- Height: 5-3/4 inches (146 mm)
- Weight: 24 lbs approx. (10.8 kg)

Input-Voltage Selector

The CDP18S670 includes an input-voltage selector located on its back panel. (See Fig. 2). Before applying power to the CDP18S670 be sure that the label on the voltage-selector PC board indicates the correct ac voltage value (110 volts or 220 volts). Then, connect the ac power cord to the ac connection on the input-voltage selector.

To change the input voltage proceed as follows:

1. unplug power cord
2. slide cover over power jack
3. remove the ac fuse by pulling the fuse lever
4. gently remove the PC board from the voltage-selector module with a pair of needle-nose pliers
5. orient the PC board so that the correct voltage label (120 volts or 220 volts) is visible
6. re-insert the PC board in such a manner that the PC board when viewed through the window will show the correct value of input voltage
7. re-insert the fuse
8. plug-in power cord

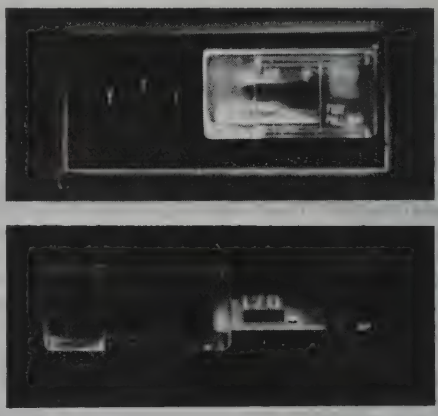


Fig. 2 - Window View of Input-Voltage Selector showing Voltage Label, Fuse, and Fuse Assembly.

Power Supply Adjustments

The Power-One Type HTAA-16W Triple-Output Power Supply shown in Figs. 3, 4, and 10 is shipped with three factory-set output voltage levels: +5 volts dc, +12 volts dc, and -5 volts dc. Potentiometers, shown in Fig. 3, are provided to adjust the range of each supply voltage. Potentiometer (R9) is used to adjust the +5 volt supply; potentiometer (R17), the +12 volt supply; potentiometer (R19), the -12 volt or -5 volt supplies. Holes are located on the left side panel of the chassis to facilitate adjustment of the three potentiometers. To adjust any one of the potentiometers, simply locate the hole in the chassis that is in-line with the required potentiometer, insert an insulated screw driver in the hole, and adjust the potentiometer. In addition, the -5 volt dc supply can be changed to -12 volts dc by placing a jumper between hole locations E1 and E2 on the power supply PC board and adjusting potentiometer (R19) for the desired voltage. To gain access to the jumper remove four screws holding the power supply to the panel, then move the power supply away from the panel far enough to permit insertion of the jumper.

CDP18S670

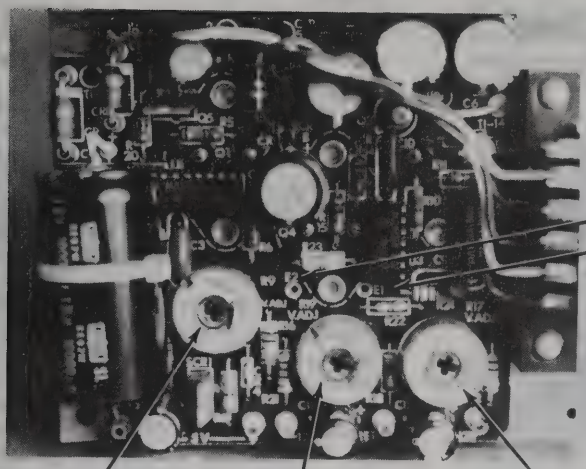


Fig. 3 - RCA COSMAC Microboard CDP18S670 "Power-One Type HTAA-16W" Power Supply - Component View.

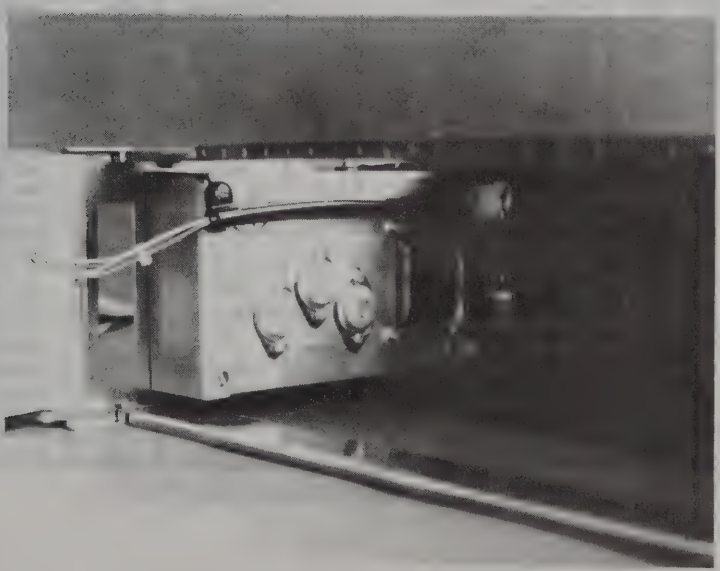


Fig. 4 - RCA COSMAC Microboard CDP18S670 Power Supply - Top View.

CDP18S670

Rack Mounting

The CDP18S670 chassis shown in Fig. 5, can be mounted in any industry-standard 19-inch computer rack by simply removing the 4 mounting screws near the front handles of the metal protective cover and gently withdrawing the chassis.

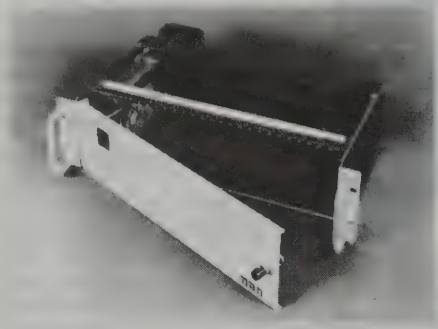


Fig. 5 - RCA COSMAC Microboard CDP18S670 Subchassis (without enclosure) for installation in 19-inch standard rack.

Microboard Universal Bus and Backplane

The Microboard Universal Bus is a compact 44-pin (dual 22) bus that contains lines for logic power, analog power, data address, and control.

All logic levels swing the full supply voltage, typical of CMOS logic, and thereby provide high noise immunity. The design of the Universal Bus and the associated backplane arrangement allow any RCA CMOS Microboard to plug into any slot. Simple and compact, this interface supports Microboard interchangeability and facilitates the rapid incorporation and evaluation of design changes.

The signals on the universal backplane and their pin assignments are listed in Table 1. For a description of the Microboard Bus Interface Signals, refer to RCA Microboard Computer Product Descriptions, MB-601, MB-602, MB-603, and MB-604. Most of these signals are derived from the CDP1802A Microprocessor. For additional information, refer to the **User Manual for the CDP1802 Microprocessor, MPM-201 and to the CDP1802A CMOS Microprocessor data sheet, File No. 1305.**

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

92CS-34444

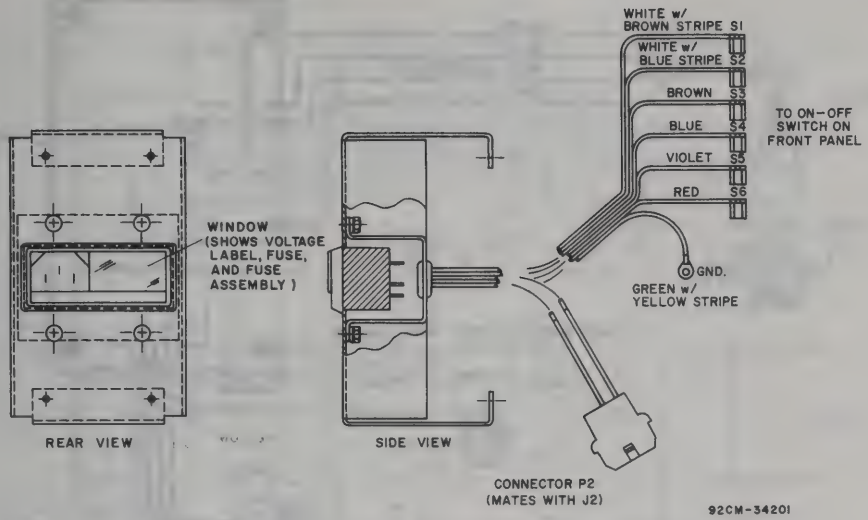


Fig. 6 - RCA COSMAC Microboard CDP18S670 Input-Voltage Selector.

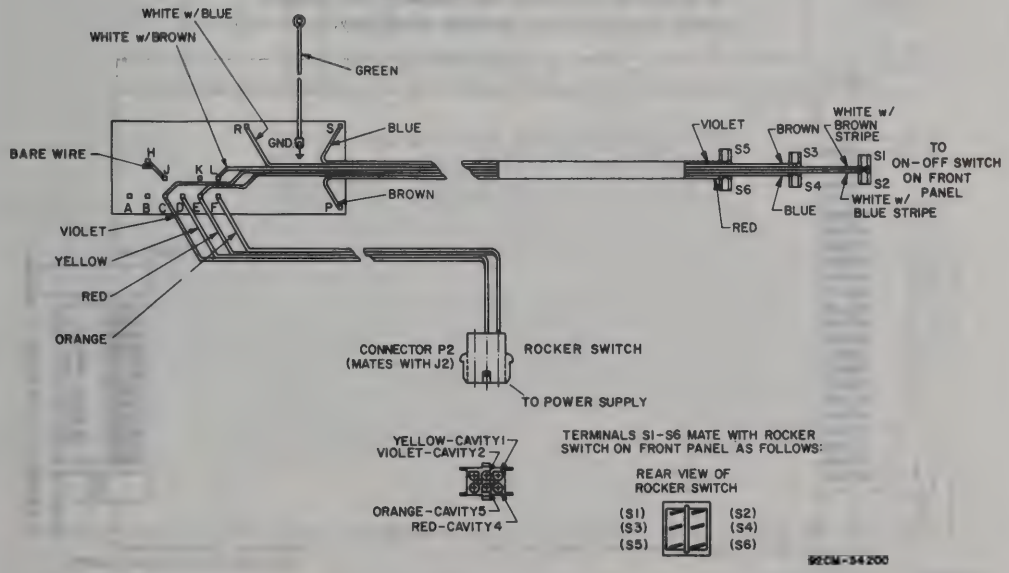


Fig. 7 - RCA COSMAC Microboard CDP18S670 Input-Voltage Selector Assembly.

CDP18S670

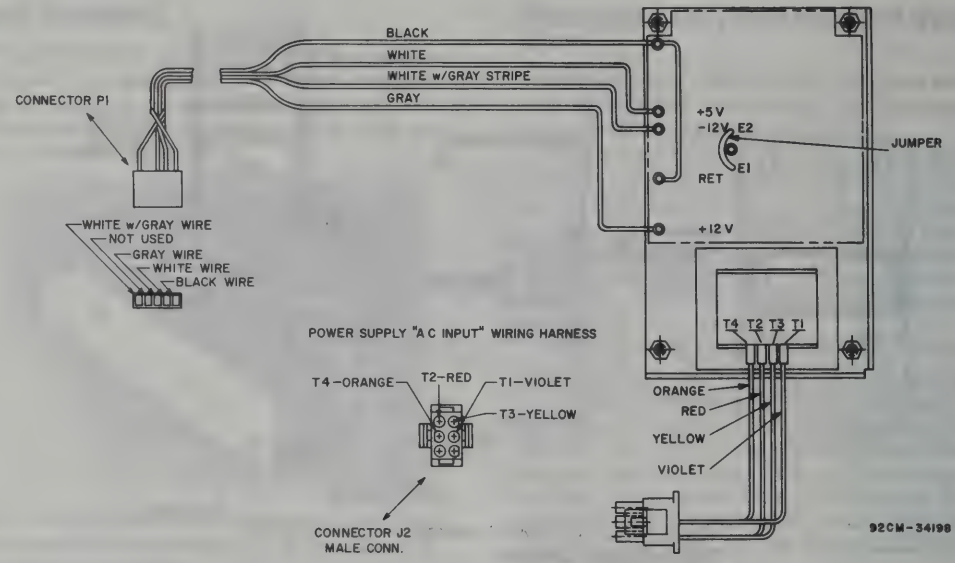


Fig. 8 - RCA COSMAC Microboard CDP18S670 Power Supply Wiring Harness Assembly.

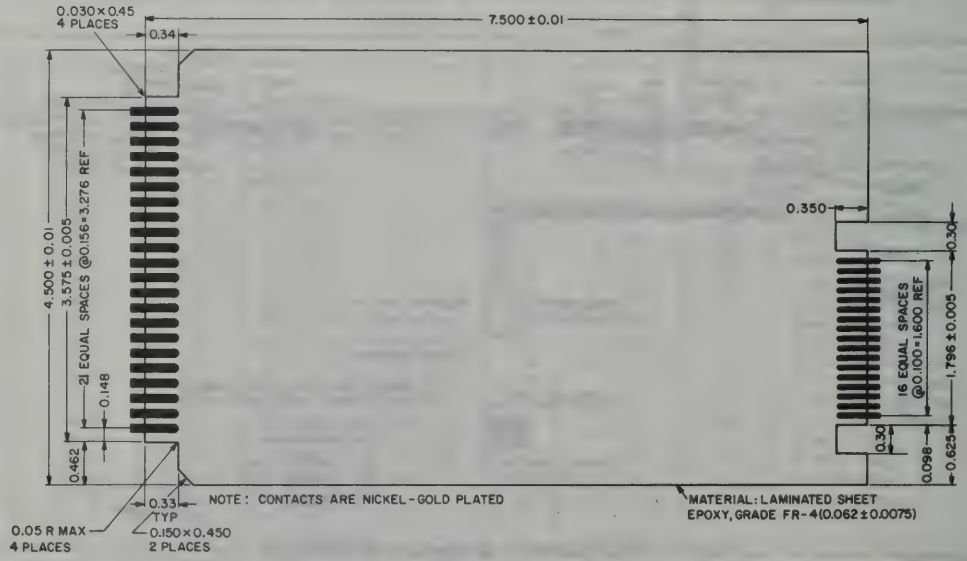


Fig. 9 - Typical Printed-Circuit Card for Representative Microboard.

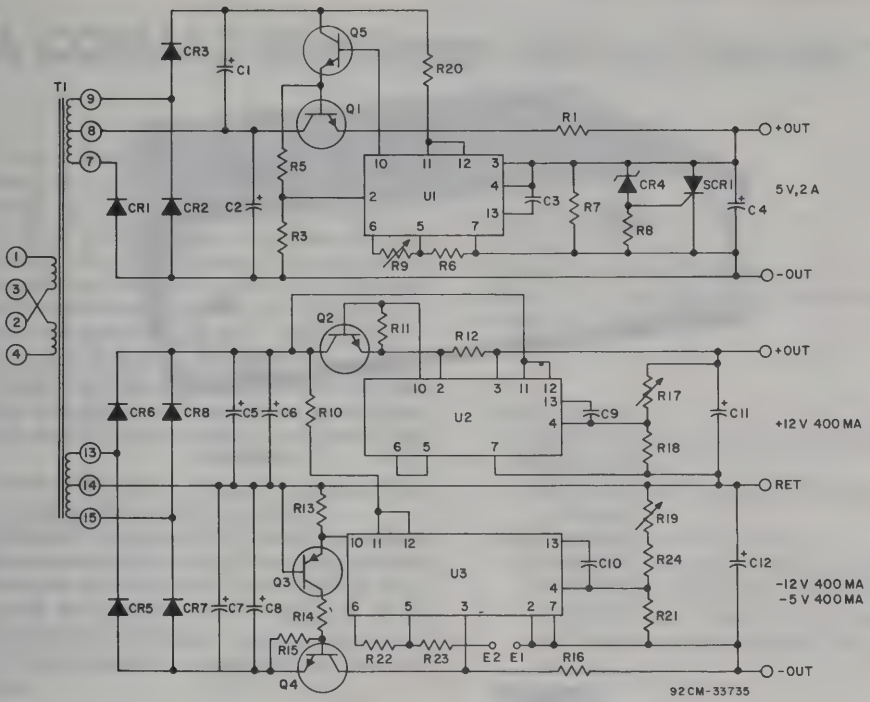
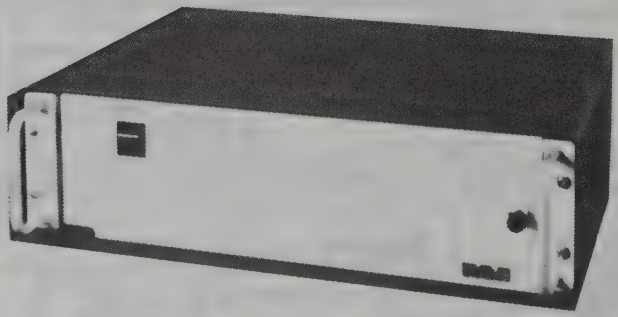
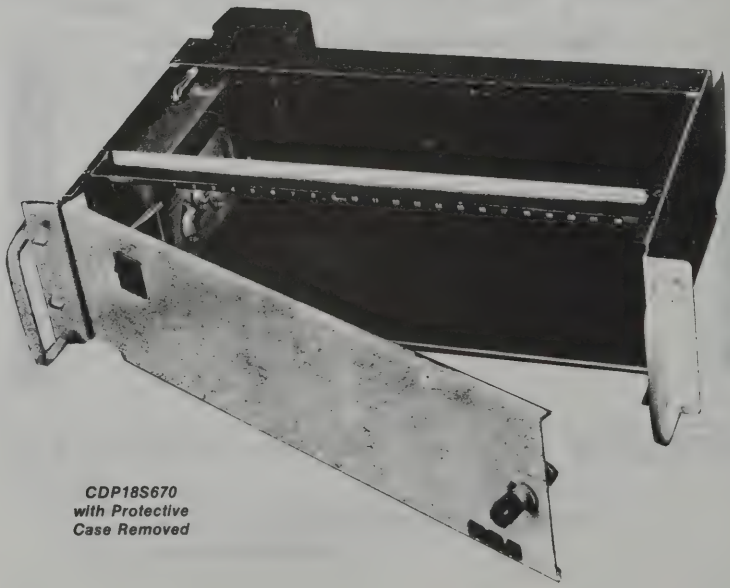


Fig. 10 - Representative Schematic Diagram for Triple-Output Power Supply "Power-One Type HTAA-16W, or Equivalent".

CDP18S670



CDP18S670



CDP18S670 with Protective Case Removed

CDP18S675
CDP18S676 (with Case)

RCA COSMAC Microboard 5-Card Chassis *

The RCA COSMAC Microboard 5-Card Chassis CDP18S675 and CDP18S676 provide compact, low-cost means for assembling systems comprised of members of the RCA Microboard milliwatt computer system family. The chassis consists of five sockets with integral card guides mounted on the RCA COSMAC universal printed-circuit backplane. The backplane pin-connection configuration is shown in Table I. For expansion beyond five cards, multiple chassis can be stacked by the soldering of an edge socket connection to the pads provided on the backplane. The added chassis mates with the edge socket through the gold-plated edge fingers.

The CDP18S675 may be mounted by means of the threaded brass inserts in each card socket.

The CDP18S676 includes a CDP18S675 chassis plus a metal base and a protective cover. The base is provided with rubber feet as well as holes for vertical mounting. Access holes are provided for the connection of flat cables to either the backplane or to the opposite end of the Microboard modules having additional outboard connectors.

Specifications

Backplane
- 0.062-inch printed-circuit board
- Five locations for 44-pin connectors
- Universal wiring (like pins connected)
- Power bus (+5 volts) on pins 21 and X
- Ground bus on pins 22 and Z

Card Socket Connectors
- 44 pin (22 dual) on 0.156-inch centers
- Integral plastic card guides

Features

- Universal backplane
- Five card slots
- Expansion and nesting interface
- Protective base and metal cover (CDP18S676 only)
- Integral card guides

Edge Connector
- Gold-plated fingers on 0.100-inch centers
- 50 pins (dual 25)
- Mates with industry-standard flat cable connectors

Edge Connector Socket Provision
- Provision is made for lap-solder mounting of an edge-connector socket (AMP PN 530268-3 or 530282-2) that will mate with the edge fingers described above for stacking two or more chassis.

Dimensions

CDP18S675 (See photo)
- Length (L) = 4-7/8 inches (124 mm)
- Depth (D) = 3.0 inches (76 mm)
- Height (H) = 2.343 inches (60 mm)

CDP18S676
- Length = 9-7/16 inches (240 mm)
- Width = 5-1/4 inches (133 mm)
- Height = 3-1/2 inches (89 mm)

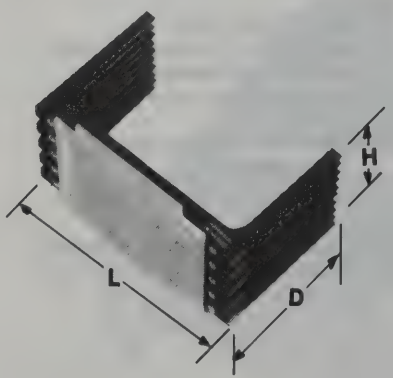
Weight
- CDP18S675: 5-1/2 ounces (155 grams)
- CDP18S676: 3 pounds 11 ounces (1.67 kilograms)

* Refer to the Industrial Chassis Series for a complete series of industrial-grade housings for RCA Microboards.

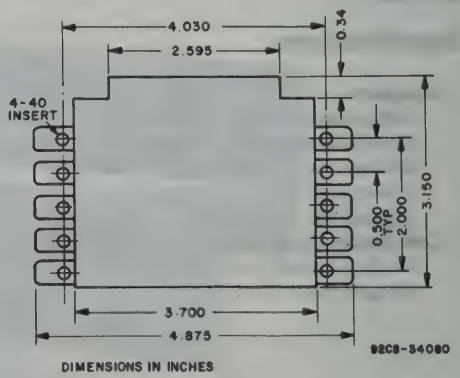
CDP18S675, CDP18S676

Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane

P1 Pin	J1-J5 Pin	Signal	P1 Pin	J1-J5 Pin	Signal
1	A	TPA-P	2	1	DMAI-N
3	B	TPB-P	4	2	DMAO-N
5	C	DB0-P	6	3	RNU-P
7	D	DB1-P	8	4	INT-N
9	E	DB2-P	10	5	MRD-N
11	F	DB3-P	12	6	Q-P
13	H	DB4-P	14	7	SC0-P
15	J	DB5-P	16	8	SC1-P
17	K	DB6-P	18	9	CLEAR-N
19	L	DB7-P	20	10	WAIT-N
23	M	A0-P	21,22	11	−5 V/−15 V
25	N	A1-P	26	12	SPARE
27	P	A2-P	28	13	CLOCK OUT
29	R	A3-P	30	14	N0-P
31	S	A4-P	32	15	N1-P
33	T	A5-P	34	16	N2-P
35	U	A6-P	36	17	EF1-N
37	V	A7-P	38	18	EF2-N
39	W	MWR-N	40	19	EF3-N
41	X	EF4-N	42	20	+12 V/+15 V
43,45	Y	+5 V	44,46	21	+5 V
47,49	Z	GND	48,50	22	GND

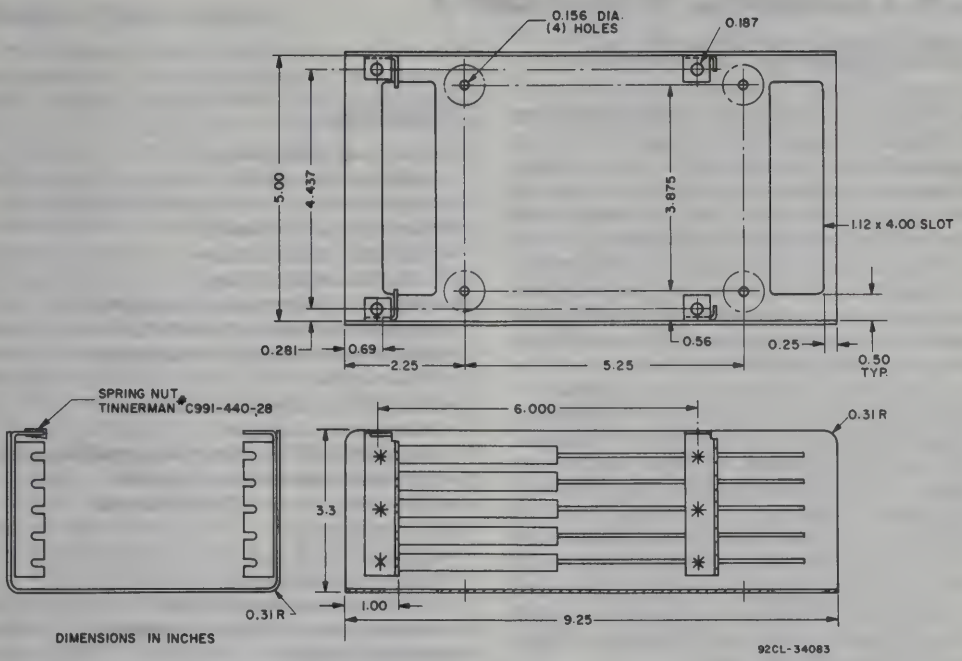


CDP18S675 5-Card Chassis



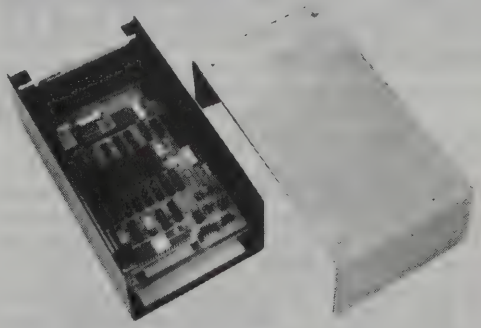
CDP18S675 5-Card Chassis — Dimensional Outline

CDP18S675, CDP18S676



CDP18S676 5-Card Chassis Base — Dimensional Outline

CDP18S676
5-Card Chassis with Base and Cover (Microboard Module - not included - shown in position)



CDP18S691, CDP18S691V3
RCA COSMAC Microboard Prototyping System*

The RCA COSMAC Microboard Prototyping System CDP18S691 is a fully assembled package that includes hardware, software, and technical literature needed to enable the user to design a microcomputer system. It provides a quick, inexpensive way to investigate and evaluate the Microboard family of components, to train personnel in microprocessor usage, and to develop computer systems for custom applications. It has 4 kilobytes of read/write memory and provides for the addition of 4/8 kilobytes of mask programmed ROM or EPROM, depending on the application requirements.

The CDP18S691 Prototyping System includes a CDP18S601 Microboard Computer to provide the complete computer function, the CDP18S640 Microboard Control and Display Module to provide the switches and displays for prototyping operation, the CDP18S675 5-Card Chassis containing the preprinted Universal Backplane for all five card positions, the CDP18S023V1 Power Converter, the CDP18S659 Microboard Breadboard for expansion flexibility, the UT60 ROM-based utility program, a CDP18S502 Extender Card, technical literature, a protective metal case of functional design, and cables for terminals and I/O.

The CDP18S691V3 is identical with the CDP18S691 except that it is supplied with the CDP18S023V3 power converter which operates on 210-250 volts, 50 Hz. It is designed for overseas use.

Features

- Low-power static CMOS
- High noise immunity
- Simple to use
- Easy to expand or modify
- Selectable serial interface—
  RS232C or 20 mA loop
- COSMAC Microprocessor architecture
- Temperature range—0 °C to 70 °C
- 65,536-byte addressable memory range
- Power on reset
- All I/O lines on edge connectors
- Microterminal interface
- Uses COSMAC Microboard Universal Backplane
- CDP18S601 Microboard Computer
- CDP18S640 Control/Display Module
- Five-card chassis
- Protective metal case
- Four control switches
- Six hexadecimal display digits
- 600-mA power converter—regulated
- Six LED displays
- ROM-based monitor software (UT60)
- 2-MHz crystal clock
- Sockets for 4/8-kilobyte ROM/PROM
- 4-kilobyte read/write memory

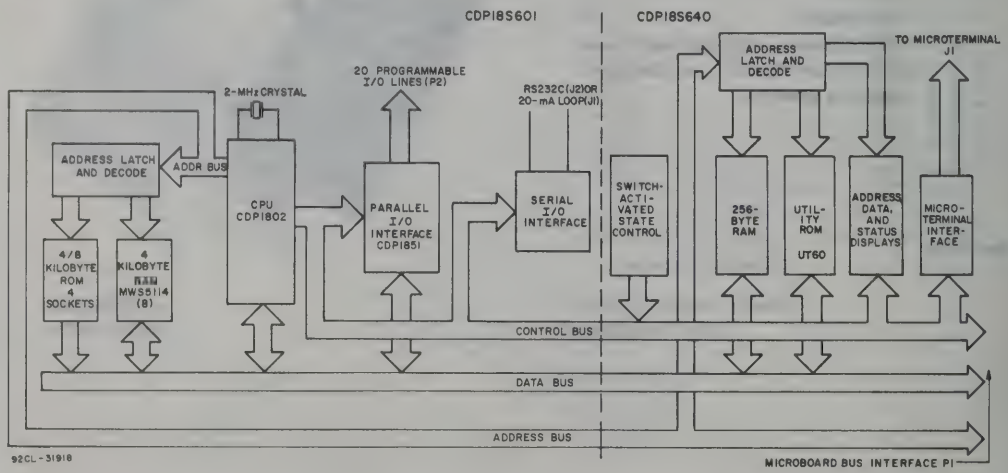


Fig. 1 - Block diagram of RCA COSMAC Microboard Prototyping System CDP18S691.

*For low-cost, highly versatile microcomputers, refer to CDP18S693, CDP18S694, and CDP18S695 Microboard Computer Development Systems.

Module Descriptions

The modules included in the Prototyping System are described below. The block diagram in Fig. 1 shows the major functions of the CDP18S601 and the CDP18S640 and how they are interconnected. Additional details on each of these two Microboard modules may be found in their product descriptions (MB-601 and MB-640).

The **CDP18S601 Microboard Computer** contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power on reset, and an expansion interface. Four on-board sockets are provided for read-only memory, enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or PROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The **central processor** for the CDP18S601 is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter, thereby giving the system multiple program states. Each register may also be used for data storage or as memory pointers for subroutines, I/O stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

By means of eight MWS5114 RAM's, the CDP18S601 provides the Prototyping System with 4 kilobytes of CMOS **read-write memory**. Four sockets are provided for four or eight kilobytes of non-volatile **read-only memory**. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in any of the 16 four-kilobyte blocks comprising the 64-kilobyte system memory space.

By means of the CMOS programmable I/O Interface CDP1851, the CDP18S601 provides the Prototyping System with 20 programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique handshaking signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard Universal Backplane. Right-angle header connections are provided for the serial communications interfaces.

The **CDP18S640 Control and Display Module** provides the Prototyping System with its operating controls, consisting of four switches, and its display system, consisting of six hexadecimal digits and six status indicators. In addition, the CDP18S640 provides two sockets which may be used for either 2 kilobytes of mask-programmable ROM (CDP1834) or 2 kilobytes of EPROM (2758). The first of these sockets contains UT60, a utility program. The second is available for expansion. A one-page (256-byte) RAM for use by either the utility program or the user program and an interface for Microterminal CDP18S021 are included.

The four control switches, labeled RESET, RUN P, RUN U, and STEP/CONT, enable the operator of the CDP18S691 Prototyping System to clear the system and hold it in the reset state, to initialize and start the user program at address 0000_{16}, to initialize and start the utility program at address 8000_{16}, or to operate the system in either the single-step mode or in the continuous mode. The STEP/CONT switch may also be used as a manual pause during program operation. The single-step mode permits execution of a single machine cycle for each pressing of the RUN U or RUN P switch.

The six-digit hexadecimal display utilizes four of the digits for current memory address and two for current data bus content. The six LED indicators provide machine status information. By means of these facilities, the operator can observe on the six-digit hexadecimal display the address and data sequences of both the fetch and the execute cycles.

The ROM-based Utility Program UT60 operates through any standard data terminal (EIA RS232C or 20-milliampere loop) to allow the user to monitor and alter the contents of memory and to start execution at any address.

The **CDP18S675 5-Card chassis** provided with the CDP18S691 Prototyping System can accommodate three Microboard modules in addition to the CDP18S601 and CDP18S640 supplied with the System. Because the chassis utilizes the RCA COSMAC Microboard Universal Backplane (See Table I for the Backplane Connector Pin List), the Prototyping System can be readily expanded with any of the Microboard Milliwatt Computer System Modules or with a user-designed module, as needed. Access holes for the cable connections are provided in the chassis base. In addition, rubber feet are provided, as well as holes for vertical mounting.

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The **CDP18S023V1 Power Converter** is a convenient, compact power supply that plugs into any standard 110-volt, 60-Hz wall outlet. It has a regulated output of +5 volts dc ±5% at 600 milliamperes, thus providing enough reserve power to operate additional Microboard Memory or other 5-volt expansion modules. The CDP18S023V1 can operate the 20 milliampere loop interface and 5-volt ROM's such as the CDP1834, the 2758, or the 2716.

The CDP18S023V3 Power Converter (supplied with the CDP18S691V3) has the same regulated output as the CDP18S023V1 (+5 volts dc ±5% at 600 milliamperes), but it is operated from an input of 210-250 volts, 50 Hz. It is provided with a standard European-type two-pin molded plug.

Provision is made on the CDP18S691 for the addition of two auxiliary voltages. Backplane pins 11 and 20 are for a negative and a positive voltage, respectively. For example, +12 volts and −5 volts on these terminals allow the use of 2708 EPROM's as well as the RS232C interface. The provision of +15 volts and −15 volts would allow the use of analog circuits as well as the RS232C interface.

The **CDP18S659 Microboard Breadboard**, supplied with the Prototyping System, is a blank module designed to mate with the Microboard Universal Backplane Connector. It provides the user with a convenient means for expansion flexibility and custom design.

The **CDP18S502 Extender Card**, supplied with the Prototyping System, provides an extension of the backplane so that the Microboard Module is accessible to the user for design modifications or trouble shooting.

Utility Program UT60

The ROM-based Utility Program UT60 is designed to examine memory, alter memory, and begin program execution at a specified location. These functions are accomplished through a series of commands initiated by a (?), (!), or ($). The functions described include memory insert (!M), memory display (?M), memory move ($M), memory fill ($F), memory substitute (!S), and run program ($P). The move and fill functions can also be called by user programs.

The UT60 includes read and type routines which provide communication with the user terminal. A "software UART" is provided which uses the Q and EF4 lines for output and input, respectively. The timing constant and duplex mode are determined when the utilities are entered from reset. Once the system has been RESET, the user can either press RUN P to begin program execution at location 0000_{16}, or press RUN U to begin execution of UT60 at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and a (LF) half-duplex operation and, at the same time, calculate the time constant to match the baud rate of the data terminal. Acceptable baud rates are 110, 300, or 1200.

The UT60 also includes user-callable routines which help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are lost, however, by the process. The CPU register contents can be examined by displaying memory beginning at $8C00_{16}$ for 20_{16} bytes.

When UT60 is ready to accept commands, it types out an asterisk (*) as a user prompt. The UT60 commands may then be entered. Where addresses are specified, leading zeroes are assumed, and if more than four digits are entered, only the last four are retained. In all cases, a command is terminated by a carriage return (CR). If a syntactical error is detected during the entry of a command, UT60 will respond with a (?) and reprompt the user with an asterisk (*).

The UT60 commands include:

?M	Memory Display
!M	Memory Insert
$M	Memory Move
$F	Memory Fill
!S	Memory Substitute
$P	Program Run

Specifications

System Contents

- CDP18S601 Microboard Computer
- CDP18S640 Microboard Control and Display Module
- CDP18S675 Microboard 5-Card Chassis
- CDP18S023V1 or CDP18S023V3 Power Converter
- CDP18S659 Microboard Breadboard
- CDP18S515 Cable for TTY terminal (20 mA loop)
- CDP18S516 Cable for RS232C terminal
- CDP18S517 Flat Cable and Connector for parallel I/O, 34 pin

CDP18S691, CDP18S691V3

Two-part metal case
ROM-based utility software (UT60)
CDP18S502 Extender Card
Technical literature (MPM-291, MPM-201, MB-601, MB-640)

RAM
4 kilobytes on CDP18S601
256 bytes on CDP18S640

ROM
4 sockets for up to 8 kilobytes on CDP18S601
1 kilobyte preprogrammed with UT60 on CDP18S640

Parallel I/O
20 lines, programmable
4 external flag inputs
1 Q line output

Serial I/O
RS232C or 20 mA loop, software driven, automatic baud rate selection of 110, 300, or 1200.

Interface Option
CDP18S021 Microterminal, hand held, low cost.

Control Switches
RESET—Clears system and holds it in reset state
RUN P—Initializes system and starts program execution at 0000_{16}
RUN U—Initializes system and starts program execution at 8000_{16}.
STEP/CONT—In step position, allows execution of a single machine cycle upon depression of RUN P. May be used as manual pause during program execution.

Displays
4 hex digits for address
2 hex digits for data
6 discrete LED's for status:
S 0 , S 1 = State code
Q = Programmable latched output
WT, CLR = Machine mode indicators
RUN = Machine running, not at idle, not reset

Expansion Options

A number of Microboard modules are available to expand the RAM/ROM and I/O capabilities of the Prototyping System. A listing of these modules follows.

CDP18S620	4-Kilobyte RAM
CDP18S621	16-Kilobyte RAM
CDP18S621V1	16-Kilobyte RAM
CDP18S622	8-Kilobyte Battery-Backup RAM
CDP18S623	8-Kilobyte RAM
CDP18S624	4-Kilobyte Battery-Backup RAM
CDP18S625	8/16/32-Kilobyte ROM/PROM
CDP18S641	UART Interface
CDP18S642	D/A Converter
CDP18S643	A/D Converter
CDP18S660	Combination Memory and I/O
CDP18S661	Video-Audio-Keyboard Interface

Each of the memory modules above has decoders with DIP switches that allow the memory to be user-assigned within the 64-kilobyte address range. All of the Microboard modules fit the COSMAC Universal Backplane. The Prototyping System 5-Card Chassis will accommodate any additional three Microboard modules.

Optional Accessories and Software

COSMAC Micromonitor CDP18S030
COSMAC Microterminal CDP18S021
PROM Programmer CDP18S480
Binary Fixed-Point Arithmetic Subroutines CDP18S826
Binary Floating-Point Arithmetic Subroutines CDP18S827

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Pin Terminals and Signals
for the RCA COSMAC Universal Backplane Connector
(P1)

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-P	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5V	In	+5 volts dc	21	+5V	In	+5 volts dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

Microboard Computer 20-mA Serial Interface (J1)				*Microboard Computer EIA RS232C Serial Interface (J2)*			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC	1	GND	6	HIGH LEVEL
2	NC	7	DATA OUT SOURCE	2	DATA IN	7	HIGH LEVEL
3	DATA OUT RETURN	8	DATA IN SOURCE	3	DATA OUT	8	HIGH LEVEL
4	DATA IN RETURN	9	NC	4	NC	9	NC
5	NC	10	NC	5	VACANT (KEY)	10	GND

CDP18S691, CDP18S691V3

CDP18S692, CDP18S692V3

RCA COSMAC Microboard Prototyping System*

The RCA COSMAC Microboard Prototyping System CDP18S692* is a fully assembled package that includes hardware, software, and technical literature needed to enable the user to design a microcomputer system. It provides a quick, inexpensive way to investigate and evaluate the Microboard family of components, to train personnel in microprocessor usage, and to develop computer systems for custom applications. It has 2 kilobytes of read/write memory and provides for the addition of 2/4 kilobytes of mask-programmed ROM or EPROM, depending on the application requirements.

The CDP18S692 Prototyping System includes a CDP18S602 Microboard Computer to provide the complete computer function, the CDP18S640V1 Microboard Control and Display Module to provide the switches and displays for prototyping operation, the CDP18S675 5-Card Chassis containing the preprinted Universal Backplane for all five card positions, the CDP18S023V1 Power Converter, the CDP18S659 Microboard Breadboard for expansion flexibility, the UT61 ROM-based utility program, the CDP18S502 Extender Card, technical literature, a protective metal case of functional design, and cables for terminals and I/O.

*Note: The CDP18S692V3 is identical with the CDP18S692 except that it is supplied with the CDP18S023V3 power converter which operates on 210-250 volts, 50 Hz. It is designed for overseas use.

Features

- Low-power static CMOS
- High noise immunity
- Simple to use
- Easy to expand or modify
- Selectable serial interface—RS232C or 20-mA loop
- COSMAC Microprocessor architecture
- Temperature range—0°C to 70°C
- 65,536-byte addressable memory range
- Power on reset
- All I/O lines on edge connectors
- Microterminal interface
- Uses COSMAC Microboard Universal Backplane
- CDP18S602 Microboard Computer
- CDP18S640V1 Control/Display Module
- Five-card chassis
- Protective metal case
- Four control switches
- Six hexadecimal display digits
- 600-mA power converter—regulated
- Six LED displays
- ROM-based monitor software (UT61)
- 2.45-MHz crystal clock
- Sockets for 2/4-kilobyte ROM/PROM
- 2-kilobyte read/write memory

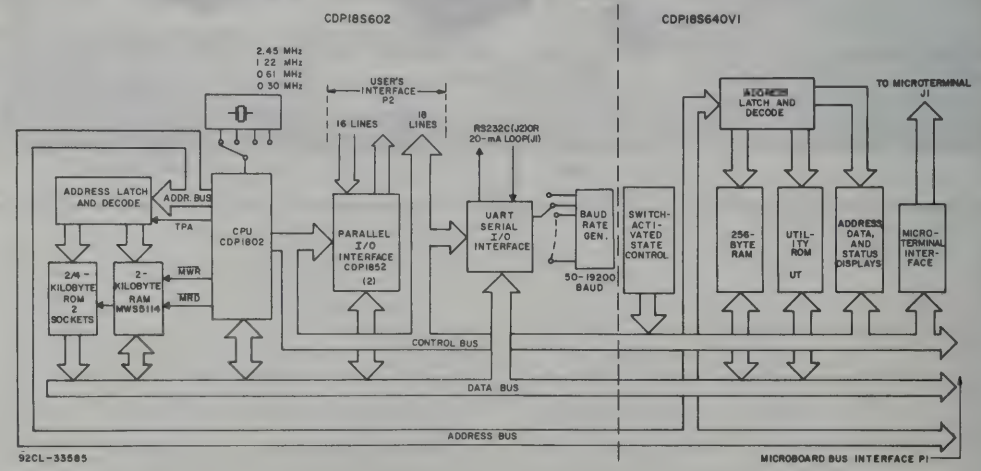


Fig. 1 - Block diagram of RCA COSMAC Microboard Prototyping System CDP18S692

*For low-cost, highly versatile microcomputers, refer to CDP18S693, CDP18S694, and CDP18S695 Microboard Computer Development Systems.

Module Descriptions

The modules included in the Prototyping System are described below. The block diagram in Fig. 1 shows the major functions of the CDP18S602 and the CDP18S640V1 and how they are interconnected. Additional details on each of these two Microboard modules may be found in their product descriptions (MB-602 and MB-640V1).

The **CDP18S602 Microboard Computer** contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power on reset, and an expansion interface. Two on-board sockets are provided for read-only memory, enabling the user to select 2 or 4 kilobytes of mask-programmable ROM or PROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The **Central Processor** for the CDP18S602 is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter, thereby giving the system multiple program states. Each register may also be used for data storage or as memory pointers for subroutines, I/O stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, whose logic levels may be tested with conditional branch instructions.

By means of four MWS5114 RAM's, the CDP18S602 provides the Prototyping System with 2 kilobytes of CMOS **read-write memory**. Two sockets are provided for two or four kilobytes of non-volatile **read-only memory**. RCA CDP1834 mask-programmed CMOS ROM, or 2758 or 2716-type EPROM's may be used in these sockets.

Two kilobytes of contiguous RAM can be placed on any even 2-kilobyte boundary. For the CDP1834 ROM and the 2758 EPROM, 2 kilobytes of contiguous memory can also be placed on any even 2-kilobyte boundary. For the 2716 EPROM, 4 kilobytes of memory can be placed on any even 4-kilobyte boundary. The parallel I/O interface consists of two CDP1852's providing one input and one output port with handshaking lines for each port.

A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by an on-board UART. The baud rate is selectable to 19200 baud. Edge connectors are provided for the parallel I/O lines and the Microboard Universal Backplane. Right-angle header connections are provided for the serial communications interfaces.

The **CDP18S640V1 Control and Display Module** provides the Prototyping System with its operating controls, consisting of four switches, and its display system, consisting of six hexadecimal digits and six status indicators. In addition, the CDP18S640V1 provides two sockets which may be used for either 2 kilobytes of mask-programmable ROM (CDP1834) or 2 kilobytes of EPROM (2758). The first of these sockets contains UT61, a utility program located at address 8000-83FF. The second is available for expansion at address 8400-87FF. A one-page (256-byte) RAM for use by either the utility program or the user program and an interface for Microterminal CDP18S021 are included.

The four control switches, labeled RESET, RUN P, RUN U, and STEP/CONT, enable the operator of the CDP18S692 Prototyping System to clear the system and hold it in the reset state, to initialize and start the user program at address 0000_{16}, to initialize and start the utility program at address 8000_{16}, or to operate the system in either the single-step mode or in the continuous mode. The STEP/CONT switch may also be used as a manual pause during program operation. The single-step mode permits execution of a single machine cycle for each pressing of the RUN U or RUN P switch.

The six-digit hexadecimal display utilizes four of the digits for current memory address and two for current data bus content. The six LED indicators provide machine status information. By means of these facilities, the operator can observe on the six-digit hexadecimal display the address and data sequences of both the fetch and the execute cycles.

The ROM-based Utility Program UT61 operates through any standard data terminal (EIA RS232C or 20-milliampere loop) to allow the user to monitor and alter the contents of memory and to start execution at any address.

The **CDP18S675 5-Card chassis** provided with the CDP18S692 Prototyping System can accommodate three Microboard modules in addition to the CDP18S602 and CDP18S640V1 supplied with the System. Because the chassis utilizes the RCA COSMAC Microboard Universal Backplane (see Table I for the Backplane Connector Pin List), the Prototyping System can be readily expanded with any of the Microboard Milliwatt Computer System Modules or with a user-designed module, as needed. Access holes for the cable connections

CDP18S692, CDP18S692V3

are provided in the chassis base. In addition, rubber feet are provided, as well as holes for vertical mounting.

The **CDP18S023 Power Converter** is a convenient, compact power supply that plugs into any standard 110-volt 60-Hz wall outlet. It has a regulated output of +5 volts dc ±5% at 600 milliamperes, thus providing enough reserve power to operate additional Microboard Memory or other 5-volt expansion modules. The CDP18S023 can operate the 20-milliampere loop interface and 5-volt ROM's such as the CDP1834, the 2758, or the 2716. Provision is made for the addition of two auxiliary voltages. Backplane pins 11 and 20 are for a negative and a positive voltage, respectively. For example, +12 volts and −5 volts on these terminals allow the use of 2708 EPROM's in the CDP18S640V1 as well as the RS232C interface. The provision of +15 volts and −15 volts would allow the use of analog circuits as well as the RS232C interface.

The **CDP18S659 Microboard Breadboard,** supplied with the Prototyping System, is a blank module designed to mate with the Microboard Universal Backplane Connector. It provides the user with a convenient means for expansion flexibility and custom design.

The **CDP18S502 Extender Card,** supplied with the Prototyping System, provides an extension of the backplane so that the Microboard Module is accessible to the user for design modifications or trouble shooting.

Utility Program UT61

The Utility Program UT61 is designed to examine memory, alter memory, and begin program execution at a specified location. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions described include memory insert !M, memory display ?M, memory move $M, memory fill $F, memory substitute !S, and run program $P. The move and fill functions can also be called by user programs.

The UT61 includes read and type routines which provide communication with the user terminal by means of the UART on the CDP18S602 Microboard Computer. Once the system has been RESET, the user can either press RUN P to begin program execution at location 0000_{16}, or press RUN U to begin execution of UT61 at location 8000_{16}. The Prototyping System is delivered with the RAM linked to address 4000_{16} and the ROM linked to address 0000_{16}. The RUN P switch function will work only if ROM's have been inserted or if the RAM is relinked to address 0000_{16}. Loading and starting programs at addresses other than 0000_{16} require the use of the !M and $P commands in UT61. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and a (LF) half-duplex operation. Be sure that the selectable baud rate is the same for both the data terminal and the CDP18S602 Microboard Computer.

The UT61 also includes user-callable routines which help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are lost, however, by the process. The CPU register contents can be examined by displaying memory (see ?M command below) beginning at $8C00_{16}$ for 20_{16} bytes. Register 0 is stored beginning at $8C00_{16}$, first the high byte and then the low byte, placing RF.1 at 8C1E and RF.0 at 8C1F. Questioning of the registers should be the first command after the UT61 is started. Otherwise, in using the stack for other commands, UT61 may over-write the data.

When UT61 is ready to accept commands, it types out an asterisk (*) as a user prompt. The commands described below may then be entered. Where addresses are specified, leading zeroes are assumed, and if more than four digits are entered, only the last four are retained. In all cases, a command is terminated by a carriage return (CR). If a syntactical error is detected during the entry of a command, UT61 will respond with a (?) and reprompt the user with an asterisk (*).

The UT61 commands include:

?M	Memory Display
!M	Memory Insert
$M	Memory Move
$F	Memory Fill
!S	Memory Substitute
$P	Program Run

CDP18S692, CDP18S692V3

Specifications

System Contents

CDP18S602 Microboard Computer
CDP18S640V1 Microboard Control and Display Module
CDP18S675 Microboard 5-Card Chassis
CDP18S023V1 or CDP18S023V3 Power Converter
CDP18S659 Microboard Breadboard
CDP18S515 Cable for TTY terminal (20-mA loop)
CDP18S516 Cable for RS232C terminal
CDP18S517 Flat Cable and Connector for parallel I/O, 34 pin
Two-part metal case
ROM-based utility software (UT61)
CDP18S502 Extender Card
Technical literature (MPM-292, MPM-201, MB-602, MB-640V1)

Note: The CDP18S023V3 Power Converter is used for the CDP18S692V3, the overseas version of the Prototyping System.

Clock

One of four crystal-controlled clock frequencies can be selected: 2.4576, 1.2288, 0.6144, or 0.3072 MHz. A preprinted link on LK3 selects 2.4576 MHz as the CPU clock frequency.

Memory Capacity

On-board RAM: 2 kilobytes
On-board ROM and EPROM: 2 sockets for up to 4 kilobytes
Off-board Expansion: Any user-specified combination of RAM, ROM, and EPROM up to a total of 65, 536 bytes on-board and off-board

Memory Address Map

On-board RAM: 2 kilobytes contiguous on any 2-kilobyte boundary. Links are preprinted for RAM at address 4000_{16}.
On-board ROM and EPROM: For CDP1834 and 2758, 2 kilobytes contiguous on any 2-kilobyte boundary.
For 2716, 4 kilobytes contiguous on any 4-kilobyte boundary. Links are preprinted for ROM and EPROM types CDP1834 and 2758 and for address start at 0000_{16}.

I/O Capacity

Parallel: 8 input lines and 8 output lines.
Serial: UART-controlled input and output lines. Choice of 20-mA loop or EIA RS232C interface. User-programmed data format. 15 selectable baud rates, 50 to 19200 baud. CTS and RTS control lines.

Operating Temperature Range

0°C to 70°C

Dimensions

Length=9-7/16 inches (240 mm)
Width=5-1/4 inches (133 mm)
Height=3-1/2 inches (89 mm)

Weight

3 pounds 11 ounces (1.67 kilograms)

Connectors

System interface: edge fingers, 44 pins (dual 22) on 0.156-inch centers
Microterminal interface: connector, 20 pins

Power Requirements

For the CDP18S602
With CMOS ROM's and RS232C: +5 V at 8 mA, typical operating
With CMOS ROM's and 20-mA loop: +5 V at 30 mA, typical operating
Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical
For the CDP18S640V1
5 V at 350 mA, typical operating

Interface Options

CDP18S021 Microterminal, hand-held, low cost

Control Switches

RESET—Clears system and holds it in reset state
RUN P—Initializes system and starts program execution at 0000_{16}
RUN U—Initializes system and starts program execution at 8000_{16}
STEP/CONT—In step position, allows execution of a single machine cycle upon depression of RUN P. May be used as manual pause during program execution.

Displays

4 hex digits for address
2 hex digits for data
6 discrete LED's for status:
S0, S1 = State code
Q = Programmable latched output
WT, CLR = Machine mode indicators
RUN = Machine running, not at idle, not reset

CDP18S692, CDP18S692V3

Expansion Options

A number of Microboard modules are available to expand the RAM/ROM and I/O capabilities of the Prototyping System. A listing of these modules follows.

CDP18S620	4-Kilobyte RAM
CDP18S621	16-Kilobyte RAM
CDP18S622	8-Kilobyte Battery-Backup RAM
CDP18S623	8-Kilobyte RAM
CDP18S624	4-Kilobyte Battery-Backup RAM
CDP18S625	8/16/32-Kilobyte ROM/PROM
CDP18S626	32/64-Kilobyte EPROM/ROM/RAM
CDP18S627	4-Kilobyte EPROM
CDP18S629	32-Kilobyte RAM
CDP18S641	UART Interface
CDP18S646	Parallel I/O Board
CDP18S642	D/A Converter
CDP18S643	A/D Converter
CDP18S644	A/D and D/A Converter
CDP18S647	D/A Converter
CDP18S648	A/D Converter
CDP18S654	A/D and D/A Converter
CDP18S657	D/A Converter
CDP18S658	A/D Converter
CDP18S660	Combination Memory and I/O
CDP18S661	Video-Audio-Keyboard Interface

Each of the memory modules above has decoders with DIP switches that allow the memory to be user-assigned within the 64-kilobyte address range. All of the Microboard modules fit the COSMAC Universal Backplane. The Prototyping System 5-Card Chassis will accommodate any additional three Microboard modules.

Optional Accessories and Software

COSMAC Micromonitor CDP18S030
PROM Programmer CDP18S480
Binary Fixed-Point Arithmetic Subroutines CDP18S826
Binary Floating-Point Arithmetic Subroutines CDP18S827
Floppy Disk Interface CDP18S651

CDP18S692, CDP18S692V3

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connection (P1)

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-N	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5 V	In	+5 V dc	21	+5 V	In	+5 V dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

Microboard Computer 20-mA Serial Interface (J1)				Microboard Computer EIA RS232C Serial Interface (J2)			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC	1	GND	6	HIGH LEVEL
2	NC	7	DATA OUT SOURCE	2	DATA IN	7	HIGH LEVEL
3	DATA OUT RETURN	8	DATA IN SOURCE	3	DATA OUT	8	HIGH LEVEL
4	DATA IN RETURN	9	NC	4	NC	9	NC
5	NC	10	NC	5	VACANT (KEY)	10	GND

CDP18S692, CDP18S692V3

Development Systems

Microboard Computer Development Systems 456
1800 Development Systems 469

CDP18S693 and CDP18S694
RCA COSMAC
Microboard Computer Development Systems (MCDS)

RCA's Low-Cost Microboard Computer Development System (MCDS) CDP18S693 Combines:

- ☐ CMOS Microprocessor Architecture CDP1802A
- ☐ CMOS Microboard Computer Module CDP18S601
- ☐ CMOS Microboard Memory and Tape I/O Module CDP18S652
- ☐ ROM-Based Basic 3 Interpreter with Full Floating-Point Arithmetic
- ☐ ROM-Based Monitor Program UT62
- ☐ Cassette I/O Unit for Mass Memory Storage
- ☐ RS232C or 20-mA Terminal Interface with Baud Rates to 1200
- ☐ Five-Card Chassis and Case
- ☐ Five-Volt Power Supply

Add a data terminal and you have a CMOS Microcomputer Development System at a surprising, unbelievably low cost.

With the CDP18S693 Microboard Computer Development System YOU can:

- ☐ Develop CDP1802 and/or Microboard software
- ☐ Program with floating-point Basic 3
- ☐ Use the system as a dedicated controller
- ☐ Expand system with any of the extensive Microboard family
- ☐ Expand system to use ROM-based Assembler/Editor
- ☐ Expand memory to full 65 kilobytes
- ☐ Extend I/O capabilities with analog and/or digital I/O Microboards

RCA's Higher-Performance Microboard Computer Development System (MCDS) CDP18S694 Combines:

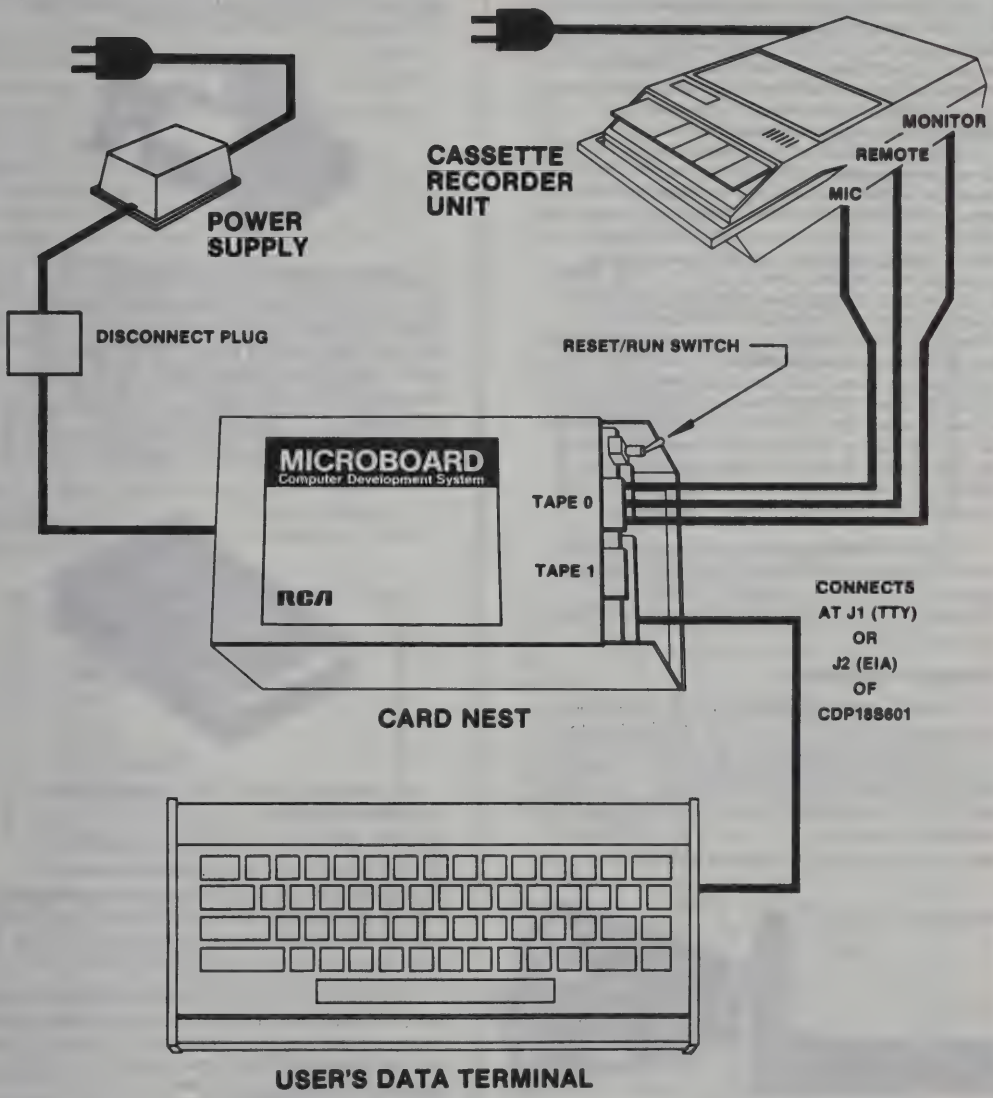
- ☐ CMOS Microprocessor Architecture CDP1802A
- ☐ CMOS Microboard Computer Module CDP18S601
- ☐ CMOS Microboard Memory and Tape I/O Module CDP18S652
- ☐ ROM-Based Assembler/Editor Program
- ☐ ROM-Based Basic 3 Interpreter with Full Floating-Point Arithmetic
- ☐ ROM-Based Monitor Program UT62
- ☐ Two Cassette I/O Units for Mass Memory Storage
- ☐ RS232C or 20-mA Terminal Interface with Baud Rates to 1200
- ☐ Five-Card Chassis and Case
- ☐ Five-Volt Power Supply
- ☐ PROM Programmer Module and Software CDP18S680

Add a data terminal and you have an even higher-performance CMOS Microcomputer Development System at a surprising low cost.

With the CDP18S694 Microboard Computer Development System YOU can:

- ☐ Develop CDP1802 and/or Microboard software
- ☐ Program with floating-point Basic 3 or assembly language
- ☐ Use the ROM-Based Assembler/Editor to develop software
- ☐ Create ASCII files on cassette tape (EDITOR)
- ☐ Convert Level I source code on tape into executable machine language on another tape (ASSEMBLER)
- ☐ Program RCA and other industry-standard UV-erasable PROM's
- ☐ Use the system as a dedicated controller with optional run-time Basic 3 (ROM)
- ☐ Expand the system with any of the extensive Microboard family

CDP18S693 Microboard Computer Development System Configuration



CDP18S693, CDP18S694

The COSMAC Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 are economical and versatile systems for the development of the hardware and software for applications based on the RCA 1800 series of CMOS microprocessor products. With the optional run-time Basic 3 available on ROM, and with the addition if needed of any of the many available expansion Microboards, the MCDS may be used very effectively for control, testing, or other dedicated microcomputer applications.

The CDP18S693 includes a five-card chassis with case, a 5-volt power supply, a CDP18S601 Microboard Computer, a CDP18S652 Microboard Combination Memory and Tape I/O Control Module augmented with a ROM-based monitor program and a ROM-based extended Basic 3 interpreter, an audio cassette tape system for mass memory storage, and the cables needed for connecting a data terminal and for connecting the cassette drive system to the CDP18S652.

The CDP18S694 has all the features of the CDP18S693 plus the following. In an additional three-ROM set on the CDP18S652, a Level I text Editor and Assembler enables the user to create CDP1802 machine language programs in Level I mnemonics. A PROM Programmer Module is also provided along with a control program on cassette tape that enables the user to program a wide variety of EPROM's. A second audio cassette drive unit is included to support the Editor and Assembler operations.

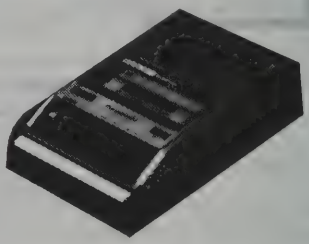
Versions for both domestic and overseas operation are available. Models CDP18S693V1 and CDP18S694V1 operate on 110-120 volts ac, 60 Hz; models CDP18S693V3 and CDP18S694V3 operate on 220-240 volts ac, 50 Hz.

Hardware Features

A **five-card chassis and case** houses the Microboards provided with the MCDS. The CDP18S693 includes the CDP18S601 Microboard Computer and the CDP18S652 Combination Memory and Tape I/O Control Module. The CDP18S694 includes the CDP18S601, CDP18S652, and a PROM programmer module. The chassis and case assembly has openings at the bottom and end to permit easy access to the cabling terminal connections.

The **power supply** for the card nest is wired through a disconnect plug to the universal backplane. Power Converter Type CDP18S023V1 is for 110-volt operation and Type CDP18S023V3 is for 220-volt operation. The dc output is 5 volts at 600 milliamperes.

The **cassette recorder unit** is connected to the CDP18S652 controller board by means of a 3-wire interface cable. The unit uses economical audio-type cassette tape. The controls on the cassette recorder include a tone control, a volume control, and play, record, rewind, fast forward, stop, and eject buttons. The unit also has a tape counter. The recorder drive mechanism is controlled through the "remote" jack by the software to provide system control of the tapes. A 60-minute tape can store over 115,000 ASCII bytes per side.



Two **cables** are provided for connecting the user-supplied **data terminal.** The CDP18S516 cable is for terminals using the EIA RS232C interface and the CDP18S515 is for terminals using a current loop interface. Either cable can be connected to the CDP18S601 Microboard Computer. No handshaking lines are required for operation. When an EIA RS232C data terminal is used, its 5-volt supply is available at the backplane, but the user must provide the additional −5 to −15 and +12 to +15 volts required.

The CDP18S694 includes all the items provided with the CDP18S693 plus a second cassette recorder unit for additional mass memory storage, a ROM-based Editor/Assembler, and a **PROM Programmer module** with cassette-tape software. The Editor/Assembler ERPOM's (3) are on the CDP18S652 Combination Memory and Tape I/O Control Module.

CDP18S693, CDP18S694

Software Features

The Microboard Computer Development Systems have a number of programs to aid the user in both hardware and software development. These programs include a full Basic 3 Interpreter with floating-point arithmetic, a resident ROM-based Monitor program, a ROM-based Editor, a ROM-based Assembler, a cassette-tape-based PROM programmer software program, and a ROM-based Basic 3 run-time version for custom applications (CDP18S842).

The full Basic 3 Interpreter and the Monitor are supplied with both the CDP18S693 and the CDP18S694. The Assembler, Editor, and PROM programmer software are supplied with the CDP18S694 but are also available as options for use with the CDP18S693. The run-time Basic 3 is an option for both systems.

Basic 3 is a 12-kilobyte high-level language that can be easily learned and readily used by the beginning programmer. Features of the Basic 3 Interpreter include full floating-point arithmetic, line editing capabilty, "trace" debugging for program creation, "cold or warm" start capability, tape control, up to 6682 multiple-character variables, 26 string variables or string arrays, and 26 one- or two-dimensional arrays. Because Basic 3 provides the CDP1802 microprocessor I/O constructs, it allows the user to develop his entire program in Basic. However, Basic 3 also allows calls to user machine-language subroutines if desired. A separate manual (MPM-841) describes the Basic 3 language and how to use the interpreter.

```
*B
MCDS BASIC-REL C6.1

C/W?
WREADY
>LIST

10 M=0
20 FOR I=1 TO 5
30 A(I)=RND(9)+1
40 M=M+A(I)
50 NEXT

READY
>
```

The ROM-based **Monitor program UT62** (2 kilobytes) allows the user to (1) inspect and modify memory, (2) to store and retrieve data on tape, (3) start execution of the Basic 3 Interpreter, the Editor, the Assembler, or a user-generated program at any address, and (4) debug programs. The twelve UT62 Monitor commands are Memory Move, Memory Fill, Memory Substitute, Memory Display, Memory Insert, Program Run, Read Tape, Write Tape, Rewind Tape, Run Basic, Run Editor, and Run Assembler. The Monitor program also includes Read and Type routines for communication between the MCDS and the data terminal and for I/O data transfers.

The resident ROM-based **Editor program** is supplied with the CDP18S694 and is an option for the CDP18S693. It allows the user to create ASCII files on cassette tape. These files can be Level I CPD1802 language, Basic 3 instructions with line numbers, or simply text. The Editor output file becomes the input file for the Assembler. The Editor commands include: Move pointer to beginning of buffer, Move pointer to end of buffer, Move pointer by n characters, Move pointer by n lines, Define input tape, Append lines, Insert text, Delete n characters, Delete n lines, Save n lines, Get saved text, Find text, Substitute text, Define output tape, Type n lines, Write n lines to output tape, Write entire buffer to output tape, Print n lines, Return to UT62, and Quit session and restart Editor.

```
*A
MCDS ASSEMBLER VER.0.0
READ?0
WRITE?1
PRESS PLAY ON READ TAPE
TYPE ANY KEY
H,L,U,J?H
00AA QTY
0001 R1
0008 R8
0124 SHORT
2000 LONG
4000 DATA
A000;
```

The resident ROM-based **Assembler program** is also supplied with the CDP18S694 and is an option for the CDP18S693. It allows the user to convert a Level I source file on tape (source code) into an executable machine language program on another tape (object code). The object code can then be loaded into memory by the UT62 Monitor program for execution, or it can be placed in an EPROM by the PROM programmer. The Assembler permits the user to write programs using convenient mnemonic expressions rather than machine language. It is a two-pass assembler with COSMAC Level I syntax. The Assembler also provides error messages to assist in debugging.

The **PROM programmer software** is supplied with the CDP18S694 and is included with the PROM programmer module in the CDP18S680 as an option for the CDP18S693. It enables the rapid programming of the RCA 18U42, the Intel 2704, 2708, 2758, and 2716 UV-erasable PROM's or any other equivalent PROM's. In addition, Intel 1702-type PROM's can be read (but not programmed) so that they can be copied into lower-power CDP18U42 CMOS PROM's or combined into other larger-sized PROM's. Operations can be with either positive or negative data. The operating software object code for the PROM programmer is provided on a tape. Operations available include (1) programming a PROM from a RAM buffer or file, automatically

CDP18S693, CDP18S694

followed by a verification; (2) verifying a PROM against a RAM buffer or file; (3) copying a PROM into a RAM buffer, automatically followed by a verification; (4) filling a RAM buffer with all 1's or 0's used in verifying PROM erasure; and, (5) saving a RAM buffer onto a tape. The software is designed for flexibility so that, in addition to the basic operations provided, more sophisticated procedures can be derived.

Optional Software

The Basic 3 Run-time version CDP18S842 allows the user to execute his program in any CDP1802-based system. This version starts program execution automatically after reset. Thus, the user may develop his program using the Basic 3 development version supplied with the MCDS and then for his final turnkey operation, use the Basic 3 Run-time version. To use Run-time Basic an additional Microboard such as the CDP18S626 32/64-kilobyte ROM/PROM/RAM is required. (Part number CDP18S842)

Accessory and Expansion Options

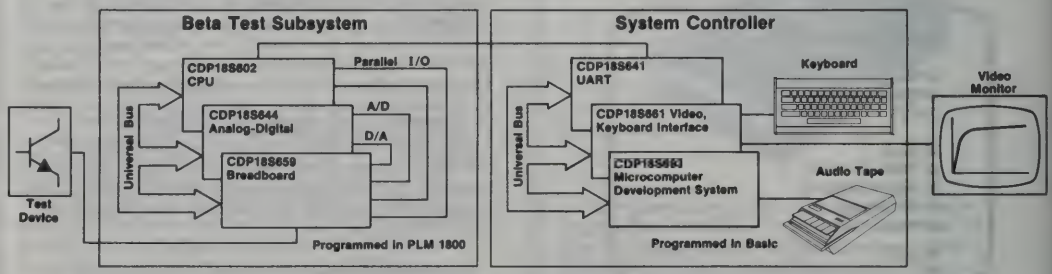
Microboard Expansion Modules. The user can add any of the many CPD18S600-series Microboards to provide I/O expansion or expanded peripheral interfacing. Microboards have a wide temperature range; normal operation is at −40 to +85°C with exceptions. (Booklet: COSMAC Microboard Computer Systems CMB-250)

Printer Option

With the CDP18S646 Microboard printer interface, the user can add a parallel Centronics-type printer and obtain hard copy output from cassette tape using the Editor P command. With a serial printer used in combination with a video terminal and connected to one of the CDP18S601 serial output ports, the user can obtain a hard copy output through the T command.

Components Available Separately for Replacement or Upgrading

CDP18S601 Microboard Computer
CDP18S652 Combination Memory and Tape I/O Control
CDP18S680 PROM Programmer Module and Software
CDP18S810 Audio Cassette Recorder Unit
CDP18SUT62 MCDS Monitor ROM
CDP18S841 MCDS Basic 3 Interpreter ROM set (development)
CDP18S842 MCDS Basic 3 Interpreter ROM set (run-time)
CDP18S843 MCDS Assembler/Editor ROM's
CDP18S646 Microboard Printer Interface, Parallel Centronics Type



Actual MCDS Application

This diagram illustrates a practical application of Microboards and the Microboard Computer Development System (MCDS) in custom production test equipment. This particular custom tester, in actual use in RCA's Malaysian plant, tests and sorts transistors. In addition to the Beta test shown, other processor-controlled subsystems test for saturation voltage, breakdown voltage, leakage, and switching parameters. High-level languages were used for rapid program development. For the test subsystems, PLM was chosen because it contains built-in constructs for programming the I/O Microboards. For the system controller, Basic was chosen because it provides the human interaction and the floating-point arithmetic needed for displays and report generation.

Note that the MCDS was both the basic development tool and the final control system.

CDP18S693, CDP18S694

Specifications

CDP18S693V1 and CDP18S693V3 System Components

CDP18S601 Microboard Computer
CDP18S652 Combination Memory and Tape I/O Control Module
5-Card Chassis with Protective Base and Cover
CDP18S023V1 or CDP18S023V3 Power Converter
CDP18S515 TTY Terminal Interface Cable (20 mA)
CDP18S516 EIA Terminal Interface Cable (RS232C)
CDP18SUT62 ROM-based Monitor Program
CDP18S841 Basic 3; ROM-base Extended Basic Interpreter
CDP18S810 Audio Cassette Recorder Unit
CDP18S529 Cassette Interface Cable
Technical Literature

CDP18S694V1 and CDP18S694V3 System Components

All the components of the CDP18S693 System plus:
CDP18S810 Audio Cassette Recorder Unit
Cassette Interface Cable
CDP18S680 PROM Programmer Module with PROM programmer software on cassette tape
Text Editor, ROM-based
Level I Assembler, ROM-based

Five-Card Chassis and Case

Dimensions:
Width 5-1/8 inches (130 mm)
Length 9-7/16 inches (240 mm)
Height — 3-7/16 inches (87 mm)

Operating Temperature Range:
0 to 70°C

Memory, I/O, and Control Specifications

RAM:
4 kilobytes on CDP18S601 at 0000H-0FFFH
1 kilobyte on CDP18S652 at 8C00H-8FFFH

ROM:
4 sockets for 8 kilobytes on CDP18S601
2 kilobytes preprogrammed with UT62 on CDP18S652 at 8000H-88FFH
12 kilobytes preprogrammed with Basic 3 on CDP18S652 at B000H-DFFFH
6 kilobytes preprogrammed with Editor/Assembler on CDP18S652 at 9000H-A7FFH

Parallel I/O:
20 lines, programmable
4 external flag inputs
1 Q line output

Serial I/O:
RS232C or 20-mA loop, software driven, automatic baud rate selection up to 1200
Two audio cassette tape unit channels with start/stop controls

System Control:
RESET/RUN switch linkable to start running at 8000H for UT62 or at 0000H for user program

Instruction Set

255 CDP1802 Microprocessor instructions

Power Converter CDP18S023V1

Input: 120 V, 50/60 Hz, 9 W
Output: +5 V dc, ±5 % at 600 mA, regulated
Dimensions: 2.7 x 2.1 x 1.6 inches
Weight: 12.5 ounces

Power Converter CDP18S023V3

Input: 210-250 V, 50 Hz, 9 W
Output: +5 V dc, ±5 % at 600 mA, regulated
Dimensions: 130 x 63.5 x 50.8 mm
Weight: 482 grams

PROM Programmer

Basic Operations:
Program a PROM from a RAM buffer or tape; automatically followed by a verification
Verify a PROM against RAM buffer or tape
Copy a PROM into RAM buffer, automatically followed by a verification
Fill RAM buffer with all 1's or 0's; used in verifying PROM erasure
Save RAM buffer onto a tape

Plug-In Module:
Dimensions: 4.5 x 7.5 inches (114.3 x 190.5 mm)
Three Zero-Insertion Force PROM Sockets:
1 for 1702/CDP18U42
1 for 2704/2708
1 for 2716/2758
Plugs into 5-Card Chassis
Assigned to Group Select 4

Power Supplies:
External-Programming Power:
+25 V ±0.1 V at 50 mA for 2716/2758
+26 V ±0.1 V at 20 mA for 2704/2708
-9 V ±5 % at 70 mA for reading 1702 PROM's
-5 V ±5 % at 50 mA (pin 11) for 2704/2708
+12 V ±5 % at 70 mA (pin 20) for 2704/2708
+22 V ±0.1 V at 10 mA for CDP18U42

LED Indicators
Power ON to PROM
External Programming Power ON
Programming ON

Switches:
Power to PROM ON/OFF
Selector Switch

Programming Times:
2704 — 1 minutes 25 seconds
2708 — 2 minutes 45 seconds
2716 — 1 minutes 45 seconds
2758 — 50 seconds
CDP18U42 — 3 seconds

Types of PROM's handled:
CDP18U42 256 word by 8 bit
1702 256 word by 8 bit-read only
2704 512 word by 8 bit
2708 1024 word by 8 bit
2758 1024 word by 8 bit
2716 2048 word by 8 bit-single voltage only
} Intel PROM's or equivalent

CDP18S810 Audio Cassette Recorder Unit

Model: Panasonic RQ-2309A, or equivalent
Power requirements: 110 or 220 V, 50/60 Hz, 6 W
Controls: tone control, volume control, play, record, rewind, fast forward, stop, eject buttons, tape counter

Literature Supplied

MPM-293	User Manual for the RCA COSMAC Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694
MPM-841	Use of Basic 3 Interpreter CDP18S841 with the RCA COSMAC Microboard Development Systems CDP18S693 and CDP18S694
MPM-920A	Instruction Summary for the CDP1802 COSMAC Microprocessor
MB-601	RCA COSMAC Microborad Computer CDP18S601

CDP18S693, CDP18S694

Here are some answers you might want while you are considering the many advantages of the MCDS.

Why CMOS?

The many advantages of CMOS (Complementary-Symmetry Metal-Oxide Semiconductor) include ultra-low power dissipation, high noise immunity, operation from a single power supply with a wide operating range or even from batteries, and a wide temperature range. RCA has been the leader in CMOS since its inception.

Why Microboards?

RCA Microboards are simple-to-use, small-size (4.5 x 7.5 inches), high-performance modules that take advantage of all the CMOS features. CMOS Microboards can provide reliable operation in high-noise process-control, automotive, or production environments and are especially effective in remote or portable applications. Because Microboards are designed to fit a compact universal backplane, you have a broad selection of readily interchangeable Microboards for performance expansion. To assure reliable operation, all Microboards are tested, burned-in for 72 hours at maximum rated temperature, and then retested.

Why should I use the MCDS?

MCDS is an economical highly versatile development system for CDP1802 CMOS Microprocessor hardware and software applications. With MCDS you can program with floating-point Basic 3 or the ROM-based Assembler/Editor and take advantage of the PROM programmer. You can expand your system with any of more than 45 different Microboard products, expand memory to 65 kilobytes, and extend the I/O with both analog and digital Microboards. MCDS can be not only your development system but also your final target system.

What's so unusual about MCDS Basic 3?

The Basic 3 Interpreter ROM features full floating-point arithmetic, line editing, trace debugging, cold or warm start, tape control, up to 6682 multiple-character variables, strings and arrays, plus access to CDP1802 I/O constructs. It allows calls to user machine-language routines and provides I/O instructions for any added Microboard. **Another big plus for Basic 3 is a special ROM-based run-time version for executing your program on any CDP1802 system. With run-time Basic 3 and the user program in memory (either RAM or ROM), your program will begin execution immediately after reset.**

How will the Editor/Assembler help me?

The ROM-based Editor supplied with the CDP18S694 will help you generate ASCII files in CDP1802 Assembly language, Basic 3 instructions with line numbers, or simply text. The Assembler converts source files into executable machine language programs. With the Editor/Assembler, you can write programs faster and more accurately using mnemonics instead of machine language. And you get error messages to speed up program debugging.

How much memory do I get?

With the MCDS you get 5 K of RAM and 4 sockets for up to 8 K of ROM. You also get 20 K of ROM containing the UT62 Monitor (2 K), Basic 3 (12 K), and, in the CDP18S694, the Editor/Assembler (6 K). Microboard Memories can be added and for mass memory storage you can use the tape cassettes.

Why audio tape cassettes?

Audio-type magnetic tapes on cassettes provide a low-cost, reliable means of mass memory storage. On a 60-minute tape you can store over 115,000 ASCII bytes per side. The record unit is software controlled and operated through the Monitor program. With two units, provided with the CDP18S694, the Editor/Assembler operations are supported at minimum cost.

Can I use this low-cost microcomputer as a dedicated controller?

Very definitely. Because of its relatively low cost, the optional run-time Basic, and its mass memory storage, the MCDS is an excellent choice for many dedicated control, custom testing, or data acquisition tasks. A practical example is shown on page 460.

How can I expand the MCDS capabilities?

An easy question. Just request a copy of **COSMAC Microboard Computers Systems CMB-250** and read about the more than 45 different CMOS Microboard products for your system. This comprehensive product guide describes Single-Board Computers, Memories, Digital I/O's, Video-Audio-Keyboard Interfaces, A/D Converters, D/A Converters plus accessory hardware. And our rapidly growing Microboard family always has more on the way.

Is the MCDS really "unbelievably" low cost?

This question you can best answer for yourself by making the same comparisons that we did. If you find any other system with comparable performance at anything near a comparable price, please let us know.

CDP18S693, CDP18S694

CDP18S695
RCA Color-Enhanced
Microboard Computer Development System

A Complete Stand-Alone Color System for CMOS Microcomputers at Unbelievably Low Cost

Hardware Features:

- CMOS Microprocessor Architecture
- CMOS Microboard Computer CDP18S601
- CMOS Microboard Memory and Tape I/O Module CDP18S652
- CMOS Microboard Video, Audio, Keyboard Interface CDP18S661B
- CMOS PROM Programmer CDP18S680
- Keyboard VP601
- 10-Inch Color Monitor
- 8-Card Industrial Chassis or 5-Card Chassis and Case
- 5-Volt Power Supply
- Two Audio-Cassette-Tape I/O Drives
- All Required Cables
- 20-Line Parallel I/O
- 2 Serial I/O Lines

Software Features:

- Floating-Point BASIC3 with 73 Statements and Functions plus CDP1802 I/O Constructs
- ROM-Based Editor
- ROM-Based Assembler
- ROM-Based Monitor Including 13 Utility Commands
- Dual Tape-Based PROM Programmer
- 5 K RAM and 30 K ROM Expandable to 64 K
- Tape-Based Mass-Memory Storage

plus

- Membership in RCA Software Users Group

What You Can Do With Color-Enhanced Microboard Computer Development System

- Develop Software for Any CDP1802 or Microboard Applications
- Use Color for Cursor and to Distinguish User Inputs from Computer Responses
- Use Background Color to Identify Monitor versus Program Development Modes
- Speed Up and Simplify Editing and Program Development
- Develop Software in Assembly Language or BASIC3 High-Level Language
- Write Your Entire Program in BASIC3 with Total I/O Handling
- Use Color for Your Application
- Expand with Any RCA Memory or I/O Microboard

Hardware Components (5-Card Chassis shown) of Color-Enhanced Microboard Computer Development System CDP18S695V1 (For domestic use).

CDP18S695

The RCA color-enhanced Microboard Computer Development System CDP18S695 is the world's first color software development system for RCA-1802 CMOS Microprocessor products. An economical and versatile system, it uses color not only to enhance the monitor display, but also to simplify and speed up screen editing. Color facilitates the separation of user input and computer responses, speeds up cursor and prompt location, and simplifies operating mode identification by background color.

The CDP18S695 uses the RCA Microboard Universal Backplane permitting expansion with any of the memory or I/O Microboards. For example, the addition of one Microboard CDP18S629 will fill the entire 64 kilobytes of memory. For hard copy output, a printer interface Microboard such as the CDP18S646 can be readily plugged in and used with a parallel Centronics-type printer. With a user-supplied program, the serial interface on the CDP18S601 Microboard, already part of the system, could be used for a serial printer.

Hardware Features

The **five-card chassis and case** houses the four Microboards provided with the CDP18S695 Color MCDS. Included is the CDP18S601 Microboard Computer with 4 kilobytes of RAM, sockets for 8 kilobytes of ROM, and 20 programmable parallel I/O lines. The CDP18S652 Combination Memory and Tape I/O Control Module interfaces the two audio cassette tape recorder units with one kilobyte of CMOS RAM, and 21 kilobytes of programmed ROM's containing the Monitor program, the extended BASIC3 Interpreter, the Assembler and Editor, and the video character-memory bit patterns.

The CDP18S661B Microboard provides the video and keyboard interface. The video display may be 40 characters per line by 24 lines, or double-size characters 20 per line by 12 lines. It provides up to 128 user-programmable characters in any 6 by 8 configuration. It has eight programmable colors for characters or background and provides graphics, motion, and hardware scrolling. A programmable tone or noise audio output is also available.

The PROM Programmer Microboard programs a variety of EPROM's including the 2708, CDP18U42, 2758, or 2716.

The **power supply** for the card nest is a wall-plug type wired to the universal backplane. The Monitor and the cassette recorder units are separately powered.

Both **cassette recorders** are connected to the CDP18S652 Control Module. The units use economical audio-type cassette tape. The cassette recorders have volume and tone controls; play, record, rewind, fast forward, stop, and eject buttons; and tape counters. The "remote" jack provides system control of the tapes. A 60-minute tape stores over 115,000 ASCII bytes per side.

The **VP-600-series keyboard** has 58 flexible-membrane light-touch keys in typewriter format and uses ASCII-encoded 128-character alphanumerics. The keys are rated for a contact life of greater than five million operations.

The **color video monitor** has a 10-inch diagonal screen and brightness, contrast, color, tint, and focus controls.

Software Features

The Color MCDS CDP18S695 has a number of programs for hardware and software development. Included are a full BASIC3 Interpreter with floating-point arithmetic, a resident ROM-based Monitor program, a ROM-based Editor, a ROM-based Assembler, cassette-tape-based PROM programmer software, and an optional ROM-based run-time BASIC3 for custom applications (CDP18S842).

BASIC3 is a 12-kilobyte high-level language that can be easily learned and readily used by the beginning programmer. Features of the BASIC3 Interpreter include full floating-point arithmetic, line editing capability, "trace" debugging for program creation, "cold or warm" start capability, tape control, up to 6682 multiple-character variables, 26 string variables or string arrays, and 26 one- or two-dimensional arrays. Because BASIC3 provides the CDP1802 microprocessor I/O constructs, interrupt vectoring, and DMA pointers, the user can develop his entire program in BASIC3. However, BASIC3 also allows calls to user machine-language subroutines if desired. A separate manual (MPM-841) describes the BASIC3 language and how to use the interpreter.

The ROM-based **Monitor** UT63 (2 kilobytes) (1) inspects and modifies memory, (2) stores and retrieves data on tape or displays ASCII tape files on the video monitor, (3) starts execution of the BASIC3

```
10  REM SET UP A/D AND START CONVERT
20  OUT(#30,6,0)
30  OUT(#30,5,4)
40  REM WAIT FOR CONVERT TO FINISH
50  IF EF1=0 GOTO 50
60  REM READ A/D CHANNEL 5
70  A=INP(#30,3)
80  REM COMPUTE THE OUTPUT
90  D=2.04*(SIN(A))!4
100 REM OUTPUT DATA TO D/A #1
110 OUT(#30,3,D)
120 GOTO 30
:■
```

BASIC3 Program Showing High-Level Language I/O Control

CDP18S695

Interpreter, the Editor, the Assembler, or a user-generated program at any address, and (4) debugs programs. The thirteen UT63 Monitor commands are Memory Move, Memory Fill, Memory Substitute, Memory Display, Memory Insert, Program Run, Read Tape, Write Tape, Rewind Tape, Copy Tape to Screen, Run Basic, Run Editor, and Run Assembler. Callable Read and Type routines permit communication between the video monitor and keyboard.

```
▶ D0-1F
  0000 F810 2A3C 7A30 2C4F;
  0008 22C4 6060 F018 12C2;
  0010 6300 6408 A33F 4500;
  0018 12D2 633A A367 3000

▶ I0 F822B3D4

▶ S100 83-12 46-34 2A-30
  0103 33-00 A9- B6-23

▶ F200-300 5A
▶■
```

Utility/ Monitor Debug Session

The resident ROM-based **Editor** program allows the user to create ASCII files on cassette tape. These files can be Level I CDP1802 language, BASIC3 instructions with line numbers, or simply text. The Editor Level I output file becomes the input file for the Assembler. The Editor commands include: Move pointer to beginning of buffer, Move pointer to end of buffer, Move pointer by n characters, Move pointer by n lines, Define input tape, Append lines, Insert text, Delete n lines, Save n lines, Get saved text, Find text, Substitute text, Define output tape, Type n lines, Write n lines to output tape, Write entire buffer to output tape, Print n lines, Return to UT63, and Quit session and restart Editor.

```
▶E
MCDS TAPE EDITOR VER. 0.0
—>I . . THIS IS A TEST
        LDI #34; PLO RF
        LDI #2C; PHI RF
$$
—>U$$
▶A
  MCDS ASSEMBLER VER. 0.0
READ?0
WRITE?1
  PRESS PLAY ON READ TAPE
TYPE ANY KEY■
```

Editor/ Assembler Program Start-up

The resident ROM-based **Assembler** program converts a Level I source file on tape (source code) into an executable machine language program on another tape (object code). The UT63 Monitor program loads the object code into memory for execution, or the PROM Programmer can put it into EPROM. The Assembler permits the user to write programs using convenient mnemonic expressions rather than machine language. Error messages assist in debugging.

The **PROM programmer software** enables the rapid copying, verifying, reading, and programming of the RCA CDP18U42, the Intel 2708, 2758, and 2716 UV-erasable PROM's, or equivalents.

Demonstration of Video Overlay - a Potential Application

Optional Software

The BASIC3 Run-time version CDP18S842 allows the user to execute his program in any CDP1802-based system. This version starts program execution automatically after reset. Thus, the user may develop his program using the BASIC3 development version supplied with the CMCDS and then for his final turnkey operation, use the BASIC3 Run-time version. (Part number CDP18S842)

The VIS Interpreter, CDP18S836 on cassette, is an interpretive language designed to control the video interface system of the CDP18S661B Microboard Video-Audio-Keyboard Interface. Its interpretive command set provides simple control of text, graphics, and motion on a color screen.

Fixed-point binary arithmetic subroutines are available on ROM CDPR582. This ROM contains a set of 16-bit 2's-complement arithmetic subroutines designed to operate on a CDP1802 microprocessor system.

Microboard Expansion Modules

The user can add any of the many CDP18S600-series Microboards to provide I/O expansion or expanded peripheral interfacing. Microboards have a wide temperature range; normal operation is at –40 to +85°C with exceptions. (Booklet: COSMAC Microboard Computer Systems CMB-250)

CDP18S695

CDP18S695 Specifications

System Components

CDP18S601 Microboard Computer
CDP18S652 Combination Memory and Tape I/O Control Module
CDP18S661B Video-Audio-Keyboard Interface Module
5-Card Chassis with Protective Base and Cover
CDP18S023 Power Converter
CDP18S680 PROM Programmer Module with PROM Programmer Software on Cassette Tape
Text Editor, ROM-based
Level I Assembler, ROM-based
CDP18SUT63 ROM-based Monitor Program
CDP18S841 BASIC3; ROM-based Extended Basic Interpreter
Two CDP18S810 Audio Cassette Recorder Units
Two CDP18S529 Cassette Interface Cables
Technical Literature

Eight-Card Industrial Chassis*

Dimensions:
Width 10.08 inches (256 mm)
Length 6.26 inches (159 mm)
Height 5.76 inches (146 mm)

Color Video Monitor

10-inch diagonal screen
Composite video; NTSC color
Bridged or terminated video input; video output
Controls: Front - Brightness, Color, Tint, Vertical Hold, ON/OFF; Rear - Screen, Focus, Horizontal Hold, Vertical Height, Sharpness

Keyboard

Model: VP601
128-character ASCII
58-key Typewriter Format
1-kilohertz audio-key-down signal

CDP18S810 Audio Cassette Recorder Unit

Model: Panasonic RQ-2309A, or equivalent
Power requirements: 110 or 220 V, 50/60 Hz, 6 W
Controls: tone control, volume control, play, record, rewind, fast forward, stop, eject buttons, tape counter

Power Supply

Molded plastic
Input: 110 volts, 60 Hz
Output: +5 volts at 1 ampere, regulated

Cables

Keyboard to CDP18S661B
Two Audio Cassette to CDP18S652
CDP18S661B to Video Monitor
Power supply to 5-card chassis

*May be supplied with 5-card chassis and case.

Memory, I/O, and Control Specifications

RAM:
4 kilobytes on CDP18S601 at 0000H-0FFFH
1 kilobyte on CDP18S652 at 8C00H-8FFFH

ROM:
4 sockets for 8 kilobytes on CDP18S601
2 kilobytes preprogrammed with UT63 on CDP18S652 at 8000H-87FFH
12 kilobytes preprogrammed with BASIC3 on CDP18S652 at B000H-DFFFH
6 kilobytes preprogrammed with Editor/Assembler on CDP18S652 at 9000H-A7FFH
1 kilobyte preprogrammed with character pattern for CDP18S661B at F400-F7FF

Video I/O:
Memory mapped in F400 to FFFF
Composite video output

Parallel I/O:
20 lines, programmable
4 external flag inputs
1 Q line output

Serial I/O:
RS232C or 20-mA loop, software driven
Two audio cassette tape unit channels with start/stop controls

System Control:
RESET/RUN switch linkable to start running at 8000H for UT63 or at 0000H for user program

Instruction Set

255 CDP1802 Microprocessor instructions

PROM Programmer

Basic Operations:
Program a PROM from a RAM buffer or file; automatically followed by a verification
Verify a PROM against RAM buffer or file
Copy a PROM into RAM buffer, automatically followed by a verification
Fill RAM buffer with all 1's or 0's; used in verifying PROM erasure
Save RAM buffer onto a file

Plug-In Module:
Dimensions: 4.5 x 7.5 inches (114.3 x 190.5 mm)
Three Zero-Insertion Force PROM Sockets:
1 for 1702 or CDP18U42
1 for 2708
1 for 2716 or 2758
Plugs into 5-Card Chassis
Assigned to Group Select 4

External-Programming Power:*
+25 V ± 0.1 V at 50 mA for 2716 or 2758
+26 V ± 0.1 V at 20 mA for 2708
—9 V ± 5% at 70 mA for reading 1702 PROM's
—5 V ± 5% at 50 mA (pin 11) for 2708
+12 V ± 5% at 70 mA (pin 20) for 2708
+22 V ± 0.1 V at 10 mA for CDP18U42
*Supplied by user

LED Indicators:
Power ON to PROM
External Programming Power ON
Programming ON

Switches:
Power to PROM ON/OFF
Selector Switch

Programming Times, (approx.):
2708 - 2 minutes 45 seconds
2716 - 1 minute 45 seconds
2758 - 50 seconds
CDP18U42 - 3 seconds

Types of PROM's handled:
CDP18U42, 256 word by 8 bit
1702, 256 word by 8 bit—read only
2708, 1024 word by 8 bit
2758, 1024 word by 8 bit
2716, 2048 word by 8 bit-single voltage only
} Intel PROM's or equivalent

Literature Supplied

MPM-295 User Manual for RCA COSMAC Color Microboard Computer Development Systems CDP18S695
MPM-841A BASIC3 High-Level-Language Interpreter CDP18S841 User Manual
MPM-920A Instruction Summary for the CDP1802 COSMAC Microprocessor
MPM-601 RCA COSMAC Microboard Computer CDP18S601
MB-661B RCA COSMAC Microboard Video-Audio-Keyboard Interface CDP18S661B

Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694

These economical and versatile Systems require only a user-supplied terminal and a black-and-white video monitor for RCA 1800-series hardware and software development. For information request Booklet PD13.

CDP18S695

Why the Low-Cost RCA Color Microboard Computer Development System (CMCDS) is Your Best Entry into Microcomputers

Here are some answers you might want while you are considering the many advantages of the CMCDS.

Why Microboards?

RCA Microboards are simple-to-use, small-size (4.5 x 7.5 inches), high-performance modules. Microboards can provide reliable operation in high-noise process-control, automotive, or production environments and are especially effective in remote or portable applications. Microboards are designed to fit a compact universal backplane and give you an extremely broad selection of readily interchangeable Microboards for performance expansion. To assure reliable operation, all Microboards are tested, burned-in for 72 hours at maximum rated temperature, and then retested.

What Does Color Enhancement Do for Me?

Color enhancement has several major benefits. It speeds up and simplifies editing and program development (1) by using a unique cursor color that quickly identifies it, (2) by using different colors for user keyboard input and for computer response and (3) by using different background colors to identify whether the utility program is in control or whether the system is in the program development mode. In addition, colors can be used in the display with your application.

Actual CMCDS Applications

This diagram illustrates a practical application of Microboards and the Color Microboard Computer Development System (CMCDS) in custom production test equipment that tests and sorts transistors. In addition to the Beta test shown, other processor-controlled subsystems test for saturation voltage, breakdown voltage leakage, and switching parameters.

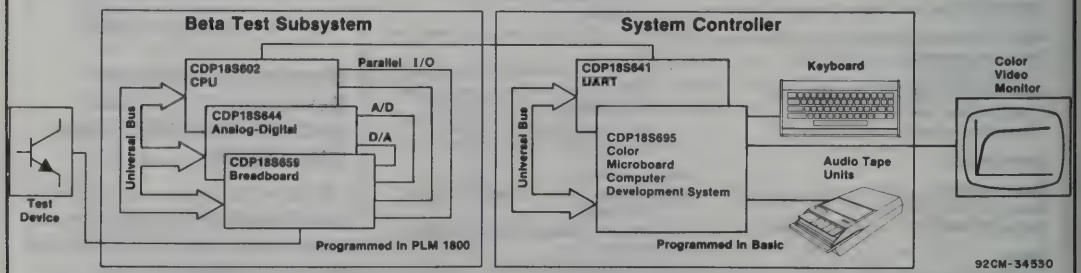
Can the CMCDS Be the Heart of My Final Product?

Because the CMCDS is a Microboard system expandable with any RAM or I/O Microboard, it can readily become your end product for control, testing, or data acquisition tasks. For example, with a CDP18S642 D/A Converter and suitable controllers you can make a remote control system that could have up to 115,000 instruction bytes on one cassette. Because of their low power, the CMCDS CPU Microboard and a CDP18S658 A/D Converter can comprise a battery-powered remote-data-acquisition system. And, if needed, the CDP18S653 MODEM Microboard can add a communications link between you and your remote system.

Your CMCDS can also be a field-programmable controller or data access system. Write your program in BASIC3 using the system in Run or Direct Execute mode as needed for debugging. Then, with the PROM Programmer put your program in EPROM and use Run-time BASIC for the final system. If a change in the program becomes necessary because of changing requirements, merely restore the BASIC3 ROM's and you can reprogram, debug, and remake EPROM's to meet the new requirements.

High-level languages were used for rapid program development. For the test subsystems, PLM was chosen because it contains built-in constructs for programming the I/O Microboards. For the system controller, Basic was chosen because it provides the human interaction and the floating-point arithmetic needed for displays and report generation.

Note that the CMCDS was both the basic development tool and the final control system.



CDP18S007V1, CDP18S007V3, CDP18S005

COSMAC DOS Development System CDP18S007V1 and CDP18S007V3
COSMAC Development System II CDP18S005

The COSMAC Development Systems are a family of support aids designed to facilitate the development of hardware and software for products based on the RCA-1800 series of CMOS microprocessor devices. The COSMAC Development Systems* offer a wide range of cost/performance features from a minimum tape-based system (CDS II - CDP18S005) to a full developmental system having floppy disk mass-memory storage and operating system software (CDS III - CDP18S007V1,V3). The systems have many common features so that upgrading from CDS II to CDS III is easily accomplished by means of Upgrade Package CDP18S837. Because the systems use a plug-in-card architecture providing space for additional I/O devices, they are convenient to use for hardware prototyping. A series of CDS modules, as well as the Microboard CDP18S600-series, is available for system expansion and prototyping. Various levels of software support, including resident editors, assemblers, and operating systems are also available to speed program development.

The CDS, designed for flexibility and expansion, provides PC module positions for spare memory and spare I/O. Extra memory and optional I/O modules are available, or the user may design and add his own. The RCA CDP18S600 Microboard series is compatible with the CDS backplane so that this broad selection of memory, I/O, and computer boards can be used for customization of the CDS.

Provision is made for two-level I/O in the systems so that I/O instructions normally reserved for CDS interfaces can be freed for user functions. I/O selection is under user program control.

Backplane wirewrapping permits easy reconfiguration to meet a particular system requirement. As delivered, the CDS is completely assembled and needs only the addition of a data terminal to become operational.

Interfacing for both 20-mA current loop and EIA RS232C terminals is standard so that a wide variety of terminals can be used with the CDS. Data terminals are handled by the CDP18S007 (CDS III) via a UART Interface Module CDP18S508 having switch-selectable baud rates of 110, 300, 1200, 4800, 9600, or 19,200 baud with full- or half-duplex operation. In the CDP18S005 (CDS II), data terminals are handled via a Terminal Interface Module CDP18S507 having automatically adjustable baud rates of 110, 300, and 1200 baud with full- or half-duplex operation.

*For information on the most complete, versatile, and powerful of RCA Development Systems, refer to the COSMAC Development System IV, CDP18S008.

Features Common to All Three Systems

The COSMAC Development Systems, CDP18S005, CDP18S007V1 and CDP18S007V3, are comprised of the following common elements:

- A 19-inch rack-mountable chassis with printed-circuit backplane
- Internal power supplies, clock, and controls
- A front panel with controls and display
- Plug-in printed-circuit modules including: CPU, Address Latch and Bank Select, RAM, ROM, I/O Decoder, and Terminal Interface Modules
- Blue metal case easily removable with four screws
- Resident ROM-based utility program

A ROM-based **System Utility** program allows the user to inspect and modify memory and start program execution at any location. When the Utility Program is started, it stores 13½ of the CPU's registers in its dedicated RAM from which the registers can subsequently be printed out. For debugging purposes, the CDS provides a single-step mode and a front-panel display showing current memory address and either the data bus or the last data byte transferred as the result of an I/O instruction. In addition, a full monitor facility may be provided by the optional Micromonitor CDP18S030A.

The Utility Program also provides various user-callable routines including disk and terminal I/O routines. In the CDS III various parameters (such as the presence or absence of parity) initialized by the Utility Program can be changed under software control to meet specific applications requirements.

System Description

The COSMAC Development Systems differ principally in the amount of RAM supplied and in the type of software support. Following is a brief description of the special features of each system. The preceding section gave the features common to all three systems.

CDP18S005, CDP18S007V1, CDP18S007V3

CDP18S005 - COSMAC Development System II (CDS II)

This system contains 4 kilobytes of static CMOS RAM and comes with a resident editor and Level-I assembler on paper tape (for operation on a Teletype* terminal) and on magnetic cassette (for operation on a TI Silent 700** terminal). The 4-kilobyte RAM supplied is sufficient to hold the Resident Editor program and provide a working buffer of about 1 kilobyte or to hold the Resident Assembler with storage for about 100 labels. Either program will automatically make use of any user-added memory.

The CDS II can be upgraded to the CDS III by the addition of (1) a floppy disk system CDP18S805, (2) eight or more kilobytes of RAM such as two CDP18S620 Microboard 4-Kilobyte RAM's, and (3) Upgrade Package CDP18S837. As an intermediate expedient to relieve the user of the burdens of paper-tape or cassette media, the floppy disk system CDP18S805 only can be added. With this expedient, however, the diskette files must be kept track of manually by track number.

CDP18S007V1 and CDP18S007V3 COSMAC DOS Development Systems

The COSMAC DOS Development System is the most powerful system of the series. It includes a CDS Central Processor containing 28 kilobytes of user-accessible RAM, a single-density dual-drive floppy-disk system, and a companion CDOS disk operating system. The additional system software includes an editor, a Level-II macroassembler, and various diskette utility programs.

Program development is considerably facilitated by the CDOS disk-file management and operating system. Because CDOS references files by file name rather than by track number, the user is provided rapid access to the files and need not be concerned about file size or disk space allocation. Assembler outputs can be directed to a disk file or to a line printer, if one is available, with symbol table and references either added or suppressed.

Versions for both domestic and overseas operation are available. Model CDP18S007V1 operates on 115 volts, 60 Hz; model CDP18S007V3 operates on 220 volts, 50 Hz.

Upgrade Options

Floppy Disk System CDP18S805. This system consists of a single-density, dual-drive floppy-disk mechanism plus an interface module that plugs into the CDS chassis. It is supplied as part of the CDS III (CDP18S007) system, but can be ordered separately to upgrade a CDP18S005. When ordered separately, the CDP18S805 is supplied with disk-based versions of the resident editor and various assemblers (including a macro assembler) and with various utility programs. These programs are non-CDOS versions of the software and require the user to keep file records by track number assignments. It is to the user's advantage to order an additional 8 kilobytes of RAM along with this system to be able to take full advantage of the software supplied. For a full upgrade to a CDS III system (CDP18S007), the user should order a Floppy Disk System CDP18S805, 8 kilobytes of additional RAM, and the Upgrade Package CDP18S837. (Part number: CDP18S805V1 for 115-volt, 60-Hz operation; CDP18S805V3 for 220-volt, 50-Hz operation; product description: PD17; instruction manual: MPM-217)

Upgrade Package CDP18S837. This package contains hardware, firmware, and software needed to upgrade a CDS II (CDP18S005) equipped with a floppy disk system and a minimum of 12 kilobytes of RAM to a CDS III (CDP18S007). The Package includes 16-kilobytes of static CMOS RAM, a UART terminal interface module, a replacement PROM for the Utility Program, a CDOS system diskette, and appropriate instruction manuals. (Part number: CDP18S837; product description: PD37)

Memory Expansion Modules. The memory of the COSMAC Development Systems may be readily expanded by use of standard plug-in module CDP18S205V1 four-kilobyte RAM, or by use of Microboard RAM modules. RAM expansion up to 60-kilobytes is provided for in the CDS II and CDS III. (Booklet: COSMAC Microboard Computer Systems CMB-250)

Optional Accessories

COSMAC Micromonitor CDP18S030A. The Micromonitor, a powerful self-contained debugging tool, may be used to considerable advantage with the COSMAC Development Systems. It permits in-circuit debugging in real time of both hardware and software. It significantly increases the speed with which hardware and software can be integrated and software debugged. It is specifically recommended for the development of programs of more than one kilobyte in length. (Part number: CDP18S030A; product description: PD18; instruction manual: MPM-218)

*Registered trademark, Teletype Corp.

**Registered trademark, Texas Instrument Corp.

CDP18S005, CDP18S007V1, CDP18S007V3

PROM Programmer CDP18S480. This hardware/software package when installed in the CDS enables the user to program the RCA CDP18U42, Intel 2704, 2708, 2758, 2716, or equivalent PROM's. In addition, it will read, but not program, 1702-type PROM's thereby providing a means of copying these PROM's onto other PROM's. The software is available on disk in both CDOS and non-CDOS versions, on paper tape, and on magnetic tape in cassette. (Part number: CDP18S480 -disk version, CDP18S480V1 - paper-tape version, CDP18S480V2 - cassette version; product description: PD22; instruction manual: MPM-222)

Microboard Expansion Modules. In addition to the Microboard Memory modules mentioned under **Upgrade Options**, the user can add other Microboards to provide I/O expansion or expanded peripheral interfacing. (Booklet: COSMAC Microboard Computer Systems CMB-250)

Optional Software

PLM 1800 High-Level-Language Compiler CDP18S839.

BASIC1 Compiler/Interpreter CDP18S834.

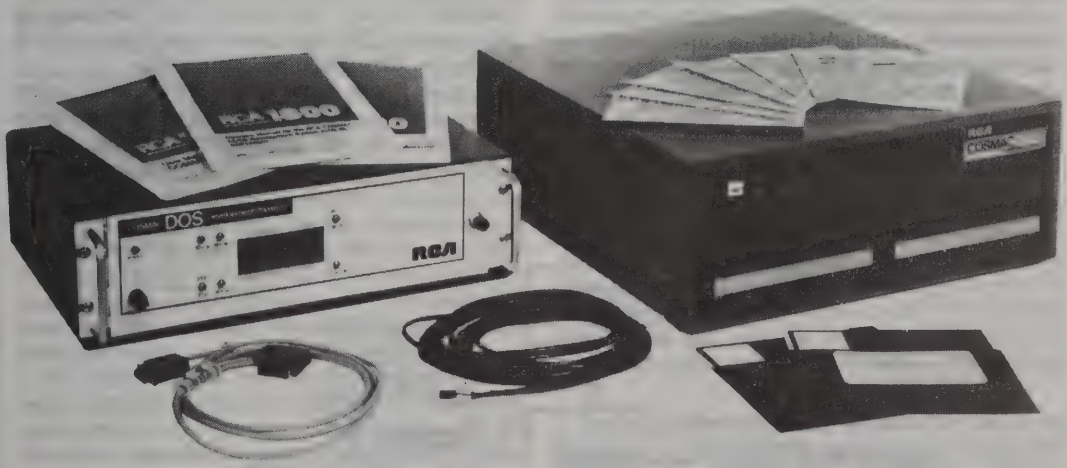
BASIC2 High-Level-Language Interpreter CDP18S840.

Micro Concurrent PASCAL (mCP) Cross Compiler CDP18S844 and Interpreter/Kernel CDP18S852 or CDP18S853.

Binary Fixed-Point Arithmetic Subroutines CDP18S826.

Binary Floating-Point Arithmetic Subroutines CDP18S827.

COSMAC Micromonitor Operating System (MOPS) CDP18S831.



CDP18S008

COSMAC Development System IV

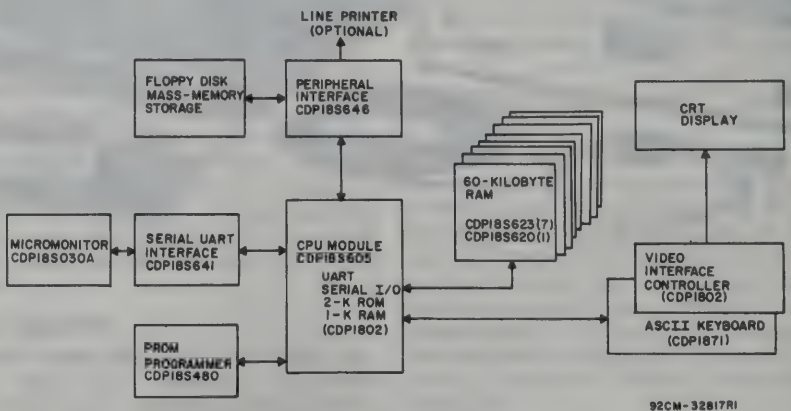
The COSMAC Development Systems (CDS IV) CDP18S008V1 and CDP18S008V3 are multiprocessor systems designed to facilitate the development of the hardware and software for applications based on the RCA 1800 series of microprocessor products. The CDP18S008 (V1 and V3) is the most complete, most versatile, and most powerful of RCA's COSMAC Development Systems. The CDP18S008 comprises (1) an integral CRT display; (2) a central processor using a static CMOS CDP1802 microprocessor; (3) a CDP1802 microprocessor-based video-keyboard controller interfacing the central processor; (4) a standard ASCII keyboard with 73 keys including 14 special-function keys; (5) 60 kilobytes of user-accessible static CMOS RAM; (6) a floppy disk dual-drive mass-memory-storage system; (7) the CDOS disk file-management and operating system; (8) a new higher-performance level II macroassembler, a full-screen editor, and a utility program; (9) a plug-in MOPS-augmented Micromonitor for extensive on-line and off-line debugging of both hardware and software; (10) a built-in PROM programmer; and (11) a built-in printer interface.

The RCA COSMAC Development Systems IV CDP18S008V5 and V7 are identical with the CDP18S008V1 and CDP18S008V3, respectively, except that they do not include the Micromonitor and the Floppy Disk Dual-Drive Mechanism. The CDP18S008V5 and CDP18S008V7 versions of the RCA COSMAC Development System IV have been made available for users who already have purchased the Micromonitor CDP18S030 and Floppy Disk Dual-Drive Mechanism CDP18S801 or CDP18S805.

A major feature of the CDP18S008 is its full-screen editing capability. Full-screen editing is an easy to use and faster form of text editing that provides instant verification of program development and changes.

Features

- **Full-Screen Editing Capability**
- **Integral CRT Display, Keyboard, and Central Processor**
- **Two Static CMOS CDP1802 Microprocessors**
- **Standard ASCII Keyboard**
- **14 Special-Function Keys for Rapid, Direct Full-Screen Editing**
- **Floppy-Disk Dual-Drive Mechanism**
- **60 Kilobytes of User-Accessible RAM**
- **CDOS Disk File Management and Operating System**
- **Resident Text Editor and Utility Programs**
- **Micromonitor for In-Circuit Real-Time Debugging (Not Just Emulation)**
- **Micromonitor Operating System (MOPS) for Hands-Off Disk-Operated Testing**
- **Built-In PROM Programmer**
- **Built-In Printer Interface**
- **Low-Power Static CMOS Microboard Components**
- **New Higher-Performance Level II Macroassembler**



Block diagram of COSMAC Development System IV

Integral Central Processor, Keyboard, and Display

The major component of the CDP18S008 is the integral central processor, keyboard and cathode-ray tube display. This unit includes a full ASCII keyboard, a CDP1802-based central processor with 60 kilobytes of static CMOS RAM, a CDP1802-based video-keyboard controller which interfaces the central processor, a PROM programmer, an interface for the MOPS-augmented Micromonitor, and an interface for an optional high-speed dot-matrix printer.

The **central processor** is based on a CDP1802 static CMOS microprocessor. The 60 kilobytes of user-accessible static CMOS read-write memory facilitate the operation of all the software provided with the CDP18S008 and permit the user to accommodate the higher-level languages such as BASIC and PLM 1800. The high noise immunity of the CMOS static components helps to assure stable operation even in the most demanding industrial environments.

The **cathode-ray tube** provided has a 12-inch (diagonal) display designed to minimize interference from ambient lighting; it is shielded to reduce specular reflections. The display provides 80 characters on each of the 24 lines for a total of 1920 characters. The flat faceplate helps to assure good readability of the white-on-dark background characters at the screen corners and edges as well as at the center.

The **keyboard** has 73 low-glare full-tactile keys and includes all the ASCII characters, both upper and lower case, and 14 special function keys. This large number of special function keys makes the data terminal one of the easiest and quickest on which to achieve high-speed efficient operation. The special keys provide the following functions directly: cursor positioning including tab, overtype, character or line insertion, character or line deletion, scrolling (next or previous line of buffer), and windowing (next or previous page of buffer). Provision is made through the control key for the lesser-used functions such as delete screen, tab set/clear, and additional cursor movement.

The **keyboard-video interface** is a microprocessor-based controller with its own CDP1802 that provides the inputs necessary to operate the keyboard and the cathode-ray tube display. It includes the CMOS Video Interface System and the CMOS Keyboard Encoder (CDP1871) to simplify control.

The **PROM programmer** built into the integral central processor, keyboard, and display is a very useful extra feature that permits the rapid programming of industry-standard PROM's including the CDP18U42, 2704, 2708, 2758, and 2716. The software necessary for programming is provided on diskette.

The **printer interface** is another built-in feature of the central processor, keyboard, and display unit. The interface enables the CDS IV to be used directly with a dot-matrix high-speed printer having a parallel Centronics-type interface.

Floppy Disk Dual-Drive Mechanism CDP18S801

The floppy disk dual-drive mechanism provided with the CDP18S008 is a mass-memory storage device with a 512-kilobyte capacity that facilitates rapid program development. It is supplied with a diskette containing the CDOS Operating System software.

COSMAC Micromonitor CDP18S030A

The Micromonitor CDP18S030A provided with the CDP18S008 is a powerful self-contained instrument that permits in-circuit debugging in real time of both hardware and software. The Micromonitor can incorporate its complete debugging capability within the development system to enable the programmer to debug software as it is being developed. It then can be used to download into any CDP1802-based breadboard or prototype for real-time in-circuit (not just emulation) debugging. The Micromonitor may also be used apart from the Development System for debugging, testing, or even field troubleshooting.

The Micromonitor includes a built-in portable full-ASCII tactile keyboard. Its commands permit the user to examine or modify memory and all CPU registers and flags. It also provides read/write capability to any I/O device and can generate signals to all CPU control, request, and flag inputs. It can either inhibit or allow system-generated requests to the DMA and interrupt lines.

Break conditions can be programmed for all of the following: external flag lines, auxiliary break input, idle interrupt response, and memory read/write. When a break occurs, the values of the principal CDP1802

CDP18S008

registers are recorded, providing a trace function. A log of the last 16 values of these registers is available to the user.

With MOPS, a Micromonitor Operating System on diskette, the debugging techniques available to the user are expanded to hands-off system testing with commands coming from disk files, thereby allowing the user to operate all Micromonitor functions from the CDP18S008.

CDP18S008 Software

Software provided with the CDP18S008 Development System includes a new higher-performance **level II macroassembler** having level I, level II, and macro capabilities. In addition to faster assembly time, the assembler provides verbal error messages and cross-reference listings. On diskette with the macroassembler are a resident editor for text editing and **full-screen editing**, the software for PROM programming, and the software for Micromonitor operation.

A ROM-based System **Utility Program** allows the user to inspect and modify memory and start program execution at any location. When the Utility Program is started, it stores 13½ of the CPU's registers in its dedicated RAM from which the registers can be subsequently printed out. The Utility Program also provides various user-callable routines including disk and terminal I/O routines. Various parameters such as the presence or absence of parity initialized by the Utility Program can be changed under software control to meet specific application requirements.

Program development on the CDP18S008 is also enhanced by the **CDOS disk file-management** and operating system. Because CDOS references files by names rather than by track number, the user is provided rapid access to the files and need not be concerned about file size of disk space allocations. In addition, the file has improved protection from inadvertent damage. Because the system can load binary files, it provides the user with considerably faster loading and reduced storage needs. Assembler outputs can be directed to a disk file or line printer with symbol table and references either added or suppressed.

Accessory and Expansion Options

Microboard Expansion Modules. The user can add up to three Microboards to provide I/O expansion or expanded peripheral interfacing. (Booklet: COSMAC Microboard Computer systems CMB-250)

Optional Software

PLM 1800 High-Level-Language Compiler CDP18S839. Provided on a diskette, this software package is designed to accelerate program development. It has features similar to those of the many well-known high-level languages such as PL/1, ALGOL, and PASCAL. Use of the PLM language encourages structured programming and, hence, provides easy readability and maintenance. Its scoped procedures and control structures also support modular programming. (Part number: CDP18S839; product description: PD39; instruction manual: MPM-239)

BASIC1 Compiler/Interpreter CDP18S834. This high-level language supplied on a diskette is also designed to facilitate rapid program development. It is an easily learned language for the beginning programmer and may be extended indefinitely by the addition of machine-language routines. The BASIC1 Compiler/Interpreter gives the user the option of (1) developing and running programs in BASIC1 directly, or (2) converting these programs to executable object code capable of running at a greater speed. (Part number: CDP18S834; product description: PD34; instruction manual: MPM-234)

BASIC2 Interpreter CDP18S840. This high-level language, more powerful than BASIC1, is also designed to facilitate rapid program development. Supplied on a diskette, it features floating-point and integer numbers, 80 statements and functions, one- or two-dimensional numerical arrays, one-dimensional string arrays, disk I/O, and trace function for debugging. In addition it has several enhanced features making use of the CDP1802 special capabilities including DMA capability, two-level input/output capability, statements to enable and disable interrupts, interrupt routines in BASIC2, and machine-language subroutines. (Part number: CDP18S840; product description: PD40; instruction manual: MPM-840)

Binary Fixed-Point Arithmetic Subroutines CDP18S826. This software package is a set of 16-bit 2's-complement fixed-point arithmetic subroutines including addition, subtraction, multiplication, and division. Also included are binary-to-BCD and BCD-to-binary conversion routines plus various utility routines. These subroutines are available on disk. (Part number: CDP18S826; product description: PD6; instruction manual: MPM-206)

Binary Floating-Point Arithmetic Subroutines CDP18S827. This software package is a set of 32-bit floating-point arithmetic subroutines including addition, subtraction, multiplication, division, sine, cosine, arctan, natural log, e^x, and square root. Also included are binary-to-BCD and BCD-to-binary conversion plus other utility routines. These subroutines are available on disk. (Part number: CDP18S827; product description: PD7; instruction manual: MPM-207)

Literature

Supplied with CDP18S008

MPM-235 - Operator Manual for the RCA COSMAC Development System IV CDP18S008
MPM-236 - Hardware Reference Manual for the RCA COSMAC Development System IV CDP18S008
MPM-201 - User Manual for the CDP1802 COSMAC Microprocessor
MPM-218 - Instruction Manual for the RCA COSMAC Micromonitor CDP18S030
MB-620 - Microboard 4-Kilobyte RAM
MB-621 - Microboard 16-Kilobyte RAM
MB-623 - Microboard 8-Kilobyte RAM
MB-641 - Microboard UART Interface
MB-646 - Microboard Parallel I/O Module
CMB-250 - COSMAC Microboard Computer Systems

Supplied with Available Options

MPM-206 - Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors
MPM-207 - Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors
MPM-234 - Use of Basic 1 Compiler/Interpreter CDP18S834 with the COSMAC DOS Development System (CDS III)
MPM-239 - User Manual for the RCA COSMAC PLM 1800 High-Level-Language Compiler
MPM-840 - BASIC2 High-Level-Language Interpreter CDP18S840 User Manual

Specifications

1. Integral Central Processor, Keyboard, and Display

Dimensions (with case)
Width 18.7 inches (475 mm)
Depth 21.2 inches (538.5 mm)
Height 11.5 inches (292.1 mm)
Weight 37 lbs. (16.8 kg.) approx.

Rear Panel
Controls: Power ON/OFF
Connectors: Disk, Printer, CRT EIA, SYS. EIA, MOPS EIA, Spare 1, Spare 2

Power Requirements
CDP18S008V1: 100-120 V ac, 60 Hz, 50 W
CDP18S008V3: 220-240 V ac, 50 Hz, 50 W
Fuse: 0.5 A

Internal Power Supplies (excluding CRT)
+5 V dc at 2.0 A, 5% regulation
–5 V dc at 0.4 A, 5% regulation
+12 V dc at 0.4 A, 5% regulation
+25 V dc at 0.4 A, 5% regulation

Operating-Temperature Range
0° to 43°C

Cabling Supplied
AC power cord: 8 feet
MOPS interconnecting cable
EIA jumper cable

Cathode-Ray Tube
Diagonal 12 inches (304.8 mm)

Keyboard
Keys: 73, full-tactile low-glare ASCII characters, upper and lower case.
14, special function, provide:
cursor positioning with tab
overtype
character insertion
line insertion
character deletion
line deletion
scrolling
windowing

Module Nest
Total slots: 16
Spare slots: 3

CDP18S008

Module Connector
44-pin; 0.156 in. pin spacing
pins 0.015 × 0.041 in.
0.6 in. connector spacing

Plug-in Modules Supplied

Function	Part Number
CPU, ROM, 2-K RAM, UART (1)	CDP18S605
4-Kilobyte RAM	CDP18S620
16-Kilobyte RAM	CDP18S621
8-Kilobyte RAM	CDP18S623
UART Interface-MOPS (1)	CDP18S641
Disk/Printer Interface (1)	CDP18S646
PROM Programmer (1)	CDP18S480

Plug-in Modules Available Separately
CDP18S600-series Microboard Modules—
See Booklet CMB-250
CRT/CPU Communication
Baud rate range: 300-19,200
Baud rate setting: 19,200 (factory set)
CRT Display
Characters per line: 80
Lines: 24
Total Characters: 1920
Word Size
Data: 8 bits
Address: 16 bits
Instruction: 1, 2, or 3 bytes
Instruction Set
225 CDP1802 Microprocessor instructions
Memory Size
65 kilobytes max.
Supplied RAM: 61 kilobytes (60 user-accessible)
Supplied ROM: 2 kilobytes
System Clock
2.4576 MHz
Internal Signal Lines
+5 V, TTL-compatible signal levels
Bidirectional data bus

2. Floppy Disk Dual Drive Mechanism

Power Requirements
CDP18S801V1: 100-120 V ac, 60 Hz, 250 W
CDP18S801V3: 220-240 V ac, 50 Hz, 250 W
Dimensions
Length 20¾ in. (527 mm)
Height 7¼ in. (184 mm)
Width 19¼ in. (489 mm)
Weight 75 lbs. (34 kg.) approx.
Cabling Supplied
AC power cord: 5 feet
CDS Interface: 4 feet
Number of Drives
2
Total System Capacity
512 kilobytes
Display Lights
BUSY, CRC ERROR, READY, DRIVE 0, DRIVE 1
Operation Timing
Seek:
Track to track: 10 ms
Head Load and Settling Time: 40 ms max.
Max. Seek Time: 820 ms
Read/Write:
Sector Read/Write Time: 6 ms
Average Latency: 83 ms
Diskette Format
IBM compatible — single density
77 tracks per diskette
26 sectors per track
128 bytes per sector
256 kilobytes per diskette

3. Micromonitor

Dimensions
Length 18.5 inches (470 mm)
Width 14.5 inches (368.3 mm)
Height 6 inches (152.4 mm)
Weight 16 lbs. (7.26 kg.) approx.
Controls
Crystal IN/OUT
Reset
Power ON/OFF
Connectors
CPU socket: 40 pin, zero insertion
Cable socket: 40 pin, zero insertion
Crystal socket: 14 pin, zero insertion
External memory connector: 44-pin edge connector; 0.156 in. pin spacing
Terminal input: 25-pin female Cinch connector

Terminal output: 25-pin male Cinch connector
External break input jack: dual banana
Memory disable output jack: dual banana

Terminal
Portable full-ASCII terminal

Power Requirements
110/220 V ac, 50/60 Hz

Power Supply
Micromonitor logic power supply tracks system under test from 4 to 10.5 volts. Presents input resistance of 9800 ohms to ground to user supply

Operating-Temperature Range
0° to 43°C

Cabling Supplied
AC power cord: 8 feet
Terminal cable

System Cable
40 wire, 3 feet long, terminated both ends in 40-pin Textool male connector
40 wire, 1 foot long, terminated both ends in 40-pin Textool male connector

Terminal Interface
20 mA or RS232C (EIA)
110, 300, or 1200 baud

System Clock
Uses clock from system under test to run user program
Internal clock: 2.112 MHz, crystal controlled

Self-Test Card
Plug-in card for checking Micromonitor operation

4. System Software

Full-Screen Editor Commands (Dedicated Keys)
Move Cursor TAB
Move Cursor ←
Move Cursor →
Move Cursor ↑
Move Cursor ↓
Move Cursor ↵
Insert Characters
Insert Lines
Delete Characters
Delete Lines
Display Next Page
Display Previous Page
Display Next Line
Display Previous Line

Text Editor Commands
Move Pointer
Delete
Append
Insert
Find
Save
Search & Substitute
Type
Output

CDOS Operating System Commands
List Directory
List Free Space on Disk
Copy Disk File to Terminal, Line Printer, or Another File
Delete File Name
Rename File
Convert ASCII-Hex File to Binary
Copy Pre-CDOS File to CDOS System
Format a New Disk
Verify Disk Files for Match
Merge File
Save CDS Memory under File Name
Examine Diskette File Contents

Resident Assembler Operation
Input: Sources files - Level I, II, Macro
Output to Disk, CRT, Printer, or Separate Terminal:
Full listing file
Hex listing file
Cross-reference listing
Error listing

Utility Program Commands
Read or Modify Memory
Read Saved State of 13½ CPU Registers
Start Program Execution at Given Location
Load CDOS Operating System

PROM Programmer Operations
Program a PROM from a RAM buffer or file; automatically followed by a verification
Verify a PROM against RAM buffer or file

CDP18S008

Copy a PROM into RAM buffer; automatically followed by a verification
Fill RAM buffer with all 1's or 0's used in verifying PROM erasure
Save RAM Buffer onto a file

Micromonitor User Functions

Examine or Modify Memory
Examine or Modify All CPU Internal Registers and Flags
Read or Write to I/O Devices
Generate Signals to All External Control, Request, and Flag Inputs to CPU
Inhibit External Request Signals
Set Break Conditions on External Flags, Auxiliary Break Input, Idle, Interrupt Response or Specified Memory Read/Write or Both
Data Log of D, X, P, and R(P) Made on Each Break or Single Instruction Cycle with Sixteen Previous Break States Held
Three Run Modes:
(1) Real time with multiple pass of break conditions
(2) Single/multiple instructions
(3) Single/multiple machine cycles
All Modes May Run from Specified Address of Present State

Micromonitor Operating System (MOPS) Command Types

Commands that allow the user to conveniently switch Micromonitor commands and responses to and from a variety of system peripherals
Single commands that allow a more complete interrogation of the CPU state
Commands for saving the system-under-test memory, registers, etc., in a disk file or for loading the system under test from a disk file
Commands that allow a degree of automation in system debugging and testing

CDP18S030A

COSMAC Micromonitor

The COSMAC Micromonitor CDP18S030A is a self-contained powerful debugging tool for use with any CDP1802 microprocessor system. It permits in-circuit debugging in real time of both hardware and software. The Micromonitor includes portable keyboard terminal and display, status indicator lights, and software debugging routines. Its primary use is for prototype-system software and hardware debugging. However, because of its easy portability, it is also useful as a field service tool. In addition, it can be used as a versatile production tester.

By means of a single cable connection, the Micromonitor, as shown in Fig. 7, can be interposed between the CPU of a system under test and all the interfaces of the CPU, giving the user control of both hardware interfaces and program execution. The Micromonitor is controlled by its own internal microprocessor, but uses the microprocessor, power supply clock, memory, etc., of the system under test to run a user program. In this way, the Micromonitor does not "emulate" the system but provides a reliable measure of true system performance.

The Micromonitor can be operated with the portable keyboard terminal supplied with the unit, or, if a hard copy record is desired, with any ASCII terminal having a 20-milliampere current loop or an EIA RS232C interface. Remote operation from a floppy disk file of commands is also possible when the Micromonitor is used with a COSMAC Development System, a Floppy Disk System and a Micromonitor Operating System—MOPS. With MOPS, the debugging techniques available to the user can extend to hands-off system testing with commands coming from disk files.

Fig. 1 - Micromonitor fully portable in attractive carrying case.

Features

- **Extensive set of debugging facilities.**
- **Operable from external terminal or from remote file.**
- **Useful for debugging prototypes, field servicing, or automated production or breadboard testing.**
- **Capable of bidirectional disk-to-system transfers of commands and data when operated with COSMAC Development Systems II, III, and IV, Floppy Disk Systems, and Micromonitor Operating System (MOPS) CDP18S831.**
- **Provision for external memory that can be substituted for the system memory for ROM simulation or system memory checkout.**
- **All address bits available and any size user-designed ROM or RAM may be added. A variety of Microboard plug-in modules listed under Available Options can be used.**
- **Tracking power supply automatically adjusts to the tested system's power supply over a range of 4 to 10.5 volts.**
- **Easy recovery from erroneous number entry in command modes built into the software.**
- **Continuous display of all CPU control lines.**
- **Break conditions automatically displayed when Micromonitor takes control.**
- **Parameter-pass feature permits display of X, R(X), and MR(X) or P, R(P), and MR(P) with only three key strokes.**
- **Accommodates terminals having rates of 10, 30, or 120 characters per second and 20-mA or RS232C interfaces.**
- **Self-test card simulates user system allowing verification of Micromonitor operation.**
- **Fully portable and self-contained in attractive carrying case.**
- **Usable worldwide on 110 or 220 volts, 50/60 Hz.**

System Features

The Micromonitor provides an extensive set of debugging capabilities. Its 43 commands permit the user to examine or modify memory and all CPU registers and

CDP18S030A

flags. The Micromonitor also provides read/write capability to any I/O device and can generate signals to all CPU control, request, and flag inputs and can either inhibit or allow system-generated requests to the DMA and Interrupt lines.

Break conditions can be programmed for all of the following: external flag lines, auxiliary break input, idle, interrupt response, or memory read/write. When a break occurs, the values of D,X,P, and R(P) are recorded, providing a trace function. A log of these values at the last 16 breaks is available to the user.

Three modes for running programs are available. One mode provides for real-time running, starting at a specified address or continuing from a break. The number of break conditions to be encountered before the Micromonitor takes control can be specified in this mode. Another mode provides for single or a specified number of instruction cycles. Data is logged after each instruction cycle in this mode. The third mode provides for a single or a specified number of machine cycles to be executed.

Specifications

User Functions

- Examine or modify memory.
- Examine or modify all CPU internal registers and flags.
- Read or write to I/O devices.
- Generate signals to all external control, request, and flag inputs to CPU.
- Inhibit external request signals.
- Set break conditions on external flags, auxiliary break input, idle, interrupt response or specified memory read/write, or both.
- Data log of D, X, P, and R(P) made on each break or single instruction cycle with sixteen previous states held.

  Three run modes:
  - — real time with multiple pass of break conditions
  - — single/multiple instructions
  - — single/multiple machine cycles

  All modes may run from specified address or present state.

Hardware

Dimensions:
- Length: 18½ inches (470 mm)
- Width: 14½ inches (368 mm)
- Height: 6 inches (152 mm)
- Weight: 16 lbs. approx. (7.3 kg)

Controls:
- Crystal In/Out
- Reset
- Power On/Off
- Baud Rate Selector

Connectors:
- CPU socket; 40-pin, zero insertion
- Cable socket; 40-pin, zero insertion
- Crystal socket; 14-pin, zero insertion
- External memory connector; 44-pin edge connector; 0.156-inch pin spacing
- Terminal input; 25-pin female Cinch connector
- Terminal output; 25-pin male Cinch connector
- External break input jack - dual banana
- Memory disable output jack - dual banana

Display:
- 14 status indicator LED's:
  IDLE, MONITOR IN CONTROL, SC1, SC0, WAIT, CLEAR, Q, INTERRUPT, DMAIN, DMAOUT, EF1, EF2, EF3, and EF4

Power Requirements:
- 110/220 V ac, 50/60 Hz

Power Supply:
- Micromonitor logic power supply tracks system under test from 4 to 10.5 volts at 500 milliamperes. Presents input resistance to user power supply of 9800 ohms to ground.
- +5 V dc at 500 mA for LED's
- +12 V dc at 200 mA for terminal interface
- −12 V dc at 100 mA for terminal interface
- Can supply up to 400 mA to external memory connector socket.

Operating Temperature Range: 0 to 43°C

Cabling Supplied: AC power cord - 8 feet

Systems Cable:
- CDP18S513: 40 wire, 3 feet long, terminated both ends in 40-pin Textool male connector
- CDP18S514: 40 wire, 1 foot long, terminated both ends in 40-pin Textool male connector
- EIA Terminal Interface, 6 wire, 8-foot long

Note: Use of 1-foot long system cable is recommended for reduced capacitive loading and maintenance of system operating speed.

Terminal Interface (input and output):
20 mA or RS232C (EIA)
110, 300, or 1200 baud

System Clock:
Uses clock from system under test to run user program
Internal clock: 2.112 MHz, crystal-controlled

Monitor Loading on System Under Test:
Power supply: 9.8 kilohms to ground
Bus loading: 25 picofarads (typ.), 1 megohm (min.)

Self-Test Card:
Plug-in card for checking Micromonitor operation.

Applications

Prototype Debugging

The Micromonitor can be used with any CDP1802-based user prototype system, as shown in Fig. 2. It provides a powerful tool for both hardware and software debugging of the prototype system. The terminal, if used, can be shared between the Micromonitor and the prototype system without moving cables.

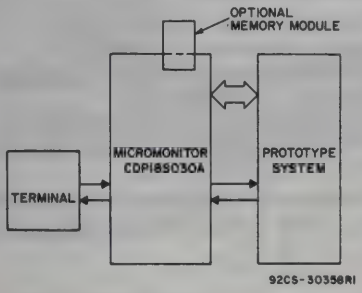


Fig. 2 - Use of Micromonitor as a prototype system debugging tool.

A user-designed memory module or any of the Microboard memories listed under Available Options may be used in the external memory socket to serve as prototype memory prior to prototype memory construction or commitment of code to ROM.

The Micromonitor can also be used with the COSMAC Development Systems II, III, and IV, as shown in Fig. 3, to form powerful hardware and software development systems. The CDS II, III, and IV have resident editor and assembler capability for rapid program development and spare slots for the addition of user-designed hardware. By controlling the CPU of these Systems with the Micromonitor, user programs and hardware can be most effectively debugged.

Programmable Automated Testing

An optional configuration, shown in Fig. 4, permits the Micromonitor to be operated by a CDS II (CDP18S005) equipped with Floppy Disk System

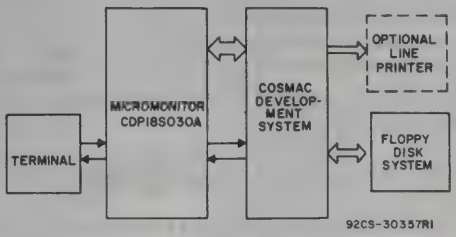


Fig. 3 - Use of Micromonitor as a prototype hardware and software debugging tool with COSMAC Development Systems CDS IV(CDP18S008), CDS III (CDP18S007), or CDS II (CDP18S005).

(CDP18S805) and Micromonitor Operating System (CDP18S831), and with COSMAC Development Systems CDS III (CDP18S007) and CDS IV (CDP18S008). The Micromonitor Operating System (MOPS) includes a UART module, an interface cable, and a Micromonitor Operating System diskette. With this system, lists of Micromonitor commands can be stored on a disk file and later be sent automatically to the Micromonitor. System responses can be directed to a user terminal, a floppy disk file, or both. Disk files can subsequently be sent to a line printer for high-speed print-out or to a user terminal.

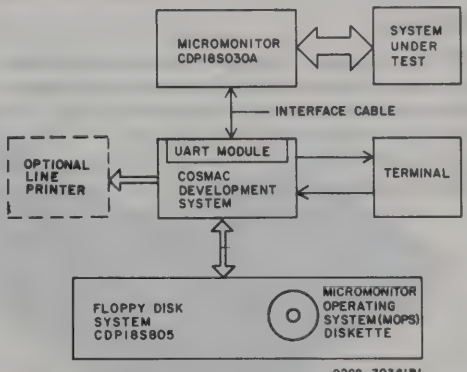


Fig. 4 - Use of Micromonitor as a programmable production or breadboard tester utilizing the Micromonitor Operating System (MOPS) CDP18S831.

CDP18S030A

Another technique for testing involves the installation of either a user-designed ROM/EPROM module or one of the Microboard memories listed under Available Options in the external memory socket of the Micromonitor. The memory can be loaded via the Micromonitor. The CPU of the system under test can then execute its own test program.

A paper tape or cassette containing test commands can be used as shown in Fig. 5 for a production or breadboard tester provided spaces are left on the tape for responses to the terminal.

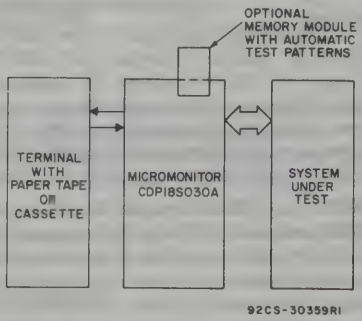


Fig. 5 - Use of Micromonitor as a programmable production or breadboard tester utilizing a data terminal equipped with paper tape or cassette.

Field Service

The Micromonitor is designed to be an effective field-service tool, as shown in Fig. 6. In its own carrying case, it weighs only 16 pounds and has a built-in tracking power supply. The complete debugging capability of the Micromonitor can be operated from the portable keyboard terminal supplied with the Micromonitor. No additional

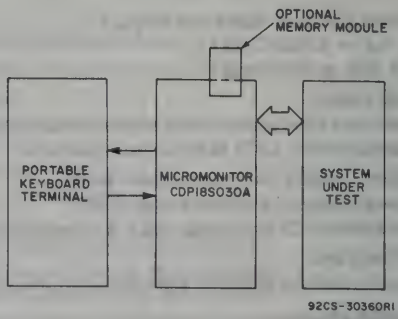


Fig. 6 - Use of Micromonitor as a field service tool.

components are required for its operation. In addition to manual operations, preprogrammed ROM-based test patterns can be exercised through an external memory socket on the Micromonitor.

Available Options

CDP18S620 4-Kilobyte RAM
CDP18S621 16-Kilobyte RAM
CDP18S622 8-Kilobyte Battery-Backup RAM
CDP18S623A 8-Kilobyte RAM
CDP18S625 8/16/32-Kilobyte ROM/PROM
CDP18S626 32/64-Kilobyte EPROM/ROM/RAM
CDP18S629 32-Kilobyte RAM

Micromonitor Operating System (MOPS) CDP18S831 including UART module, interface card, and system diskette.

Literature

Operation, installation, and application information is provided in the **Instruction Manual for the RCA COSMAC Micromonitor CDP18S030A**, MPM-218B.

CDP18S030A

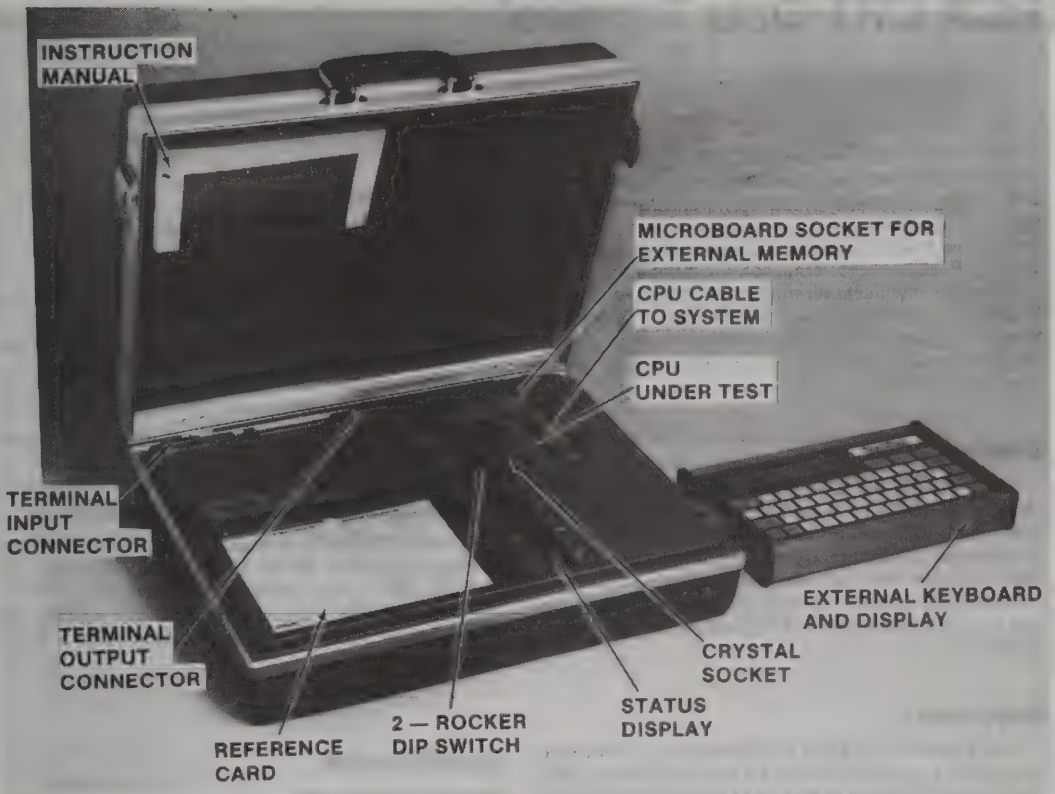
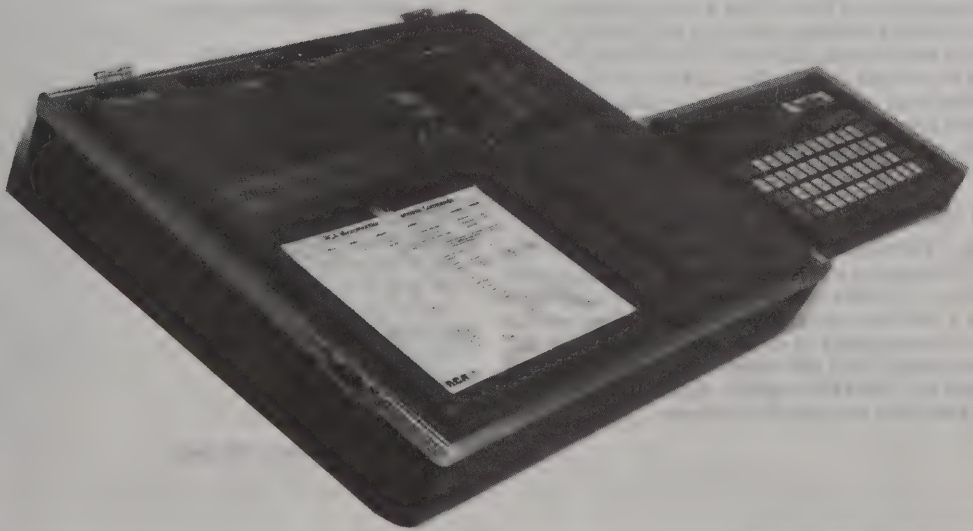


Fig. 7 - RCA COSMAC Micromonitor CDP18S030A.



Advance Data

CDP18S040

RCA CRT Data Terminal

The CRT Data Terminal CDP18S040 is a self-contained data terminal capable of both full-screen and disk editing. It consists of a cathode-ray tube display, a full ASCII keyboard with special function keys, and a multi-baud rate EIA interface. It is specially suited for use with CDP1800-series microprocessor systems or as a general purpose intelligent terminal. The terminal utilizes the CDP1802 CMOS microprocessor and all CMOS electronic components. As a result, it has excellent rf noise immunity and is, therefore, also useful in rugged industrial environments.

Features

- **Full-screen editing capability**
- **Disk editing capability**
- **Standard ASCII keyboard**
- **14 special function keys**
- **Selectable baud rates - 300 to 19,200**
- **Low-power static CMOS components**
- **Excellent rf noise immunity**
- **Useable in rugged industrial environments**
- **24-line by 80-character display**
- **Two-speed auto-repeat cursor movement**

Display

The CDP18S040 Data Terminal displays 24 lines of 80 characters each for a total of 1920 characters. The cathode-ray tube has a 12-inch diagonal and is designed to minimize interference from ambient lighting and specular reflection. Its flat faceplate helps to assure good readability of the light green on dark background characters at the screen corners and edges as well as at the screen center.

Domestic and Overseas Operation

The CDP18S040 is available for both domestic and overseas operation. Model CDP18S040V1 operates on 115 volts, 60 Hz and displays characters in an NTSC-compatible format. Model CDP18S040V3 operates on 220 volts, 50 Hz and displays characters in a PAL-compatible format.

Keyboard

The keyboard on the CDP18S040 has 73 low-glare full-tactile keys and includes all the ASCII characters, both upper and lower case, and 14 special function keys. This large number of special function keys makes the CDP18S040 terminal one of the easiest and quickest on which to achieve high-speed efficient operation. The special function keys provide the following functions directly: cursor positioning (including tab), overtype, character or line insertion, character or line deletion, scrolling (next or previous line of buffer), and windowing (next or previous page of buffer). Provision is made through the control key for the lesser-used functions such as delete screen, tab set/clear, and additional cursor movement.

I/O Interface

The CDP18S040 Terminal is provided with an EIA RS232C interface and has seven selectable baud rates in the 300- to 19,200-baud range. It is directly usable with RCA CDP1800 microprocessor-based systems and can aid in the upgrading of earlier systems to achieve full-screen editing.The CDP18S040 is specially suitable for use with the CDOS Development System III CDP18S007 with additional user-provided software.

Specifications

Dimensions (with case)
Width 18.7 inches (475 mm)
Depth 21.2 inches (538.5 mm)
Height 11.5 inches (292 mm)
Weight 37 lbs. (16.8 kg) approx.

Rear Panel
Controls: Power ON/OFF
Baud rate selector
CRT brightness
Connector: CRT EIA

Power Requirements
CDP18S040V1: 100-120 V ac, 60 Hz, 50 W
CDP18S040V3: 220-240 V ac, 50 Hz, 50 W
Fuse: 0.5 A

Internal Power Supplies
+5 V dc at 2.0 A, 5% regulation
-5 V dc at 0.4 A, 5% regulation
+12 V dc at 2.0 A, 5% regulation

Operating Temperature Range
0 to 43°C

Cabling Supplied
AC power cord: 8 feet

Cathode-Ray Tube
Diagonal: 12 inches (305 mm)

CDP18S040

Keyboard
- Keys: 73, full-tactile low-glare ASCII characters, upper and lower case
- 14, special function, provide:
  - cursor positioning with tab
  - overtype
  - character insertion
  - line insertion
  - character deletion
  - line deletion
  - scrolling
  - windowing

CRT/CPU Communication
- Baud rate range: 300 - 19,200

CRT Display
- Characters per line: 80
- Lines: 24
- Total characters: 1920

Word Size
- Data: 8 bits

Full-Screen Editor Commands (Dedicated Keys)
- Move Cursor TAB
- Move Cursor <-
- Move Cursor ->
- Move Cursor ↑
- Move Cursor ↓
- Move Cursor ↵
- Insert Characters
- Insert Lines
- Delete Characters
- Delete Lines
- Display Next Page
- Display Previous Page
- Display Next Line
- Display Previous Line

Text Editor Commands
- Move Pointer
- Delete
- Append
- Insert
- Find
- Save
- Search & Substitute
- Type
- Output

CDP18S480, CDP18S480V1, CDP18S480V2
PROM Programmer for COSMAC Development and Microboard Computer Systems

The Prom Programmer CDP18S480 is a hardware and software package for the rapid programming of industry-standard PROM's. It is designed to work with RCA COSMAC Microprocessor-based systems such as the COSMAC Development Systems CDP18S005 and CDP18S007 and Microboard Computer Systems. The CDP18S480 includes a plug-in module for interfacing the development or computer system to the PROM's to be programmed and a versatile operating program. The system will program CDP18U42, and Intel 2704, 2708, 2716, 2758, or any other equivalent PROM's. A further feature is that it facilitates the rapid programming of many PROM's from the same source. In addition, it can read but not program Intel 1702-type PROM's thereby providing a means of copying these PROM's onto other PROM's.

Three versions of the PROM Programmer are available differing in the software media with which they operate. The disk-based version is designated CDP18S480; the paper-tape version is designated CDP18S480V1; and the magnetic-tape cassette version is designated CDP18S480V2. The disk-based version CDP18S480 includes both CDOS and non-CDOS versions of the operating software.

Installation

In COSMAC Development Systems, a user-supplied external power supply is required for programming operations. In addition, a −9-volt supply is needed for reading 1702 PROM's. All other voltages needed are supplied from the CDS internal power supplies. Installation of the plug-in module is straightforward in that it only requires three jumpers to be added to the selected I/O slot. It can be plugged into any unused I/O slot in the CDS card nest. When the external power supply (and the −9 volt supply, if required) is connected and the program loaded, operation can begin.

In Microboard Computer Systems, the PROM Programmer is designed to work in a system of the following configuration:

1. Control and Display Module CDP18S640 or CDP18S640V1
2. Microboard Computer Module, such as CDP18S601 or CDP18S602
3. 4 kilobytes of RAM in the address range 0000-03FF$_{16}$ (supplied with the CDP18S601 or CDP18S602 Microboard Computer Systems)
4. Utility Program UT60 or UT61 (used with the CDP18S640 and CDP18S640V1 Control and Display Modules, respectively)
5. A Microboard Chassis, such as CDP18S675 or CDP18S676
6. A Microboard Extender CDP18S502 (when used in 5-card Microboard Chassis CDP18S675)

Microboard Prototyping Systems CDP18S691 and CDP18S692 supply the first five of the above items.

In addition to the external power supplies (programming power and −9 volts), voltages of +12 volts and −5 volts must be supplied to the Microboard Universal Backplane pins 20 and 11, respectively, when 1702, 2704, or 2708 PROM's are to be operated on.

One trace must be cut and jumpered on the Programmer plug-in module before it is installed in a Microboard Computer System.

Operation

The versatile operating program supplied with the PROM Programmer CDP18S480 provides many types of operation including:

- Programming a PROM from a file or by copying another PROM
- Verifying a PROM against a file or another PROM
- Verifying erasure of a PROM
- Combining two smaller PROM's to program a larger one
- Saving PROM data on a file in reloadable format that can also be used for masked ROM production
- Performing any of the above operations with either positive (non-inverted) or negative (inverted) logic.

The program is supplied in both object code and assembly language source. The PROM Programmer module is prewired for I/O Group Select 4 on the CDS but may be reassigned to a different Group Select by the user.

The program can run in a standard COSMAC Development System CDP18S005 or a COSMAC DOS Development System CDP18S007 with the supplied RAM. Any additional system memory available, however, can be used to advantage because the RAM buffer area for the various operations is user-definable.

Installation instructions and details of operation for this system are given in the **Operator's Manual for PROM Programmer CDP18S480**, MPM-222A.

CDP18S480, CDP18S480V1, CDP18S480V2

Specifications

Basic Operations:

- Program a PROM from a RAM buffer or file; automatically followed by a verification
- Verify a PROM against RAM buffer or file
- Copy a PROM into RAM buffer, automatically followed by a verification
- Fill RAM buffer with all 1's or 0's used in verifying PROM erasure
- Save RAM buffer onto a file

Operating Temperature Range:
0° to 43 °C

Plug-In Module
Dimensions: 4.5 x 7.5 inches (114.3 x 190.5 mm)
Three Zero-Insertion Force PROM Sockets
1 for 1702/CDP18U42
1 for 2704/2708
1 for 2716/2758
Plugs into any unused I/O slot
Assigned to Group Select 4

Power Supplies:
External—Programming Power:
+22 volts ±0.1 volt at 10 mA for CDP18U42
+25 volts ±0.1 volt at 50 mA for 2716/2758
+26 volts ±0.1 volt at 20 mA for 2704/2708
−9 volts ±5% at 70 mA for reading 1702 PROM's

From COSMAC Development Systems:
+5 volts at 200 mA
−5 volts at 50 mA
+12 volts at 70 mA

Required in Microboard Systems:
+5 volts ±5% at 200 mA (pin 21, Y)
−5 volts ±5% at 50 mA (pin 11)
+12 volts ±5% at 70 mA (pin 20)

System Configurations:
The following are suitable system configurations:

For CDP18S480—disk-based
1. COSMAC DOS Development System CDP18S007 plus Data Terminal
2. COSMAC Development System II CDP18S005 upgraded to COSMAC DOS Development System (see PD16 for details) plus Data Terminal
3. COSMAC Development System II CDP18S005 plus Floppy Disk System CDP18S805 plus Data Terminal

For CDP18S480V1—paper-tape-based
COSMAC Development System II CDP18S005 plus ASR33 Teletype Data Terminal† or equivalent.

For CDP18S480V2—cassette-based
COSMAC Developmental System II CDP18S005 plus TI "Silent 700"‡ Data Terminal or equivalent with tape cassette and "Remote Device Control" options.

LED Indications:
Power ON to PROM
External Programming Power ON
Programming ON

Switches:
Power to PROM ON/OFF
Selector Switch

Programming Times:
CDP18U42—3 seconds
2704—1 minute 25 seconds
2708—2 minutes 45 seconds
2716—1 minute 45 seconds
2758—50 seconds

PROM Programmer Components:
Plug-In Module—CDP18S402
Software:
Diskette (CDP18S480),
Paper tape (CDP18S480V1), or
Cassette (CDP18S480V2)
MPM-222A—**Operator's Manual for PROM Programmer CDP18S480**

Types of PROM's Handled:

CDP18U42	256 word by 8 bit	
1702	256 word by 8 bit—read only	Intel PROM's or equivalent
2704	512 word by 8 bit	
2708	1024 word by 8 bit	
2758	1024 word by 8 bit	
2716	2048 word by 8 bit—single voltage only	

†Registered trademark Teletype Corp.

‡Registered trademark Texas Instr. Corp.

CDP18S480, CDP18S480V1, CDP18S480V2

CDP18S508

COSMAC UART Interface Module

The UART (Universal Asynchronous Receiver/Transmitter) Module CDP18S508 is a printed-circuit card designed to provide the COSMAC Development System CDS II (CDP18S005) with a serial interface for operating a teletypewriter (TTY), a CRT, or any of various data terminals. The CDP18S508 UART Interface Module also provides a paper-tape control for use with a TTY, and serial interfaces for 20-mA loop and EIA RS232C data terminals. The CMOS UART CDP1854 is used in the Module to provide a byte interface to the system and a serial interface to the terminal. The UART is used in its Mode 1 configuration so that word length, parity, and stop bits are software-programmed. A switch is provided to permit selection of a baud rate of 110, 300, 1200, 4800, 9600, or 19,200 baud.

Installation

The UART Interface Module CDP18S508 may be installed in any I/O slot in the CDS Card Nest. Slot 24 is usually used for disk and 14 for the terminal interface. Locations 14 through 18 and 21 through 24 provide all the signals required by this Module except the I/O address lines. These lines are chosen by the user. The combination of Select and N-Decode lines chosen must be unique so that no combination is used twice in the system. They are connected as follows:

Select – Wire-wrap to pin T the I/O select line chosen from SEL1 through SEL7 (SEL0 is assigned a specific I/O function).

N Decode – Wire-wrap to pins M and N the two decoded N lines chosen from N=1 through N=7. The connection to pin N fixes the N code for data read and write. The connection to pin M determines the N code for setting the control register or for reading the status register.

Paper-Tape Control – Wire-wrap pin W to N=7, if paper-tape control is needed. Location 14 in the CDS is prewired to this signal.

Various links or jumpers may be installed on the printed-circuit card for optional connections to the system. The interrupt signal from the CDP1854 may be jumpered at LK1 to INT on the CDS backplane. The CDP1854 signals DA, THRE, PE/OE, and FE may be jumpered in any order to EF1, EF2, EF3, and EF4. Because these bits are also available in the UART status register, the connections to the EF's are optional. Serial data in (SDI) may also be linked to EF1, EF2, EF3, or EF4.

Two connections are provided for the serial interface. J1 contains the 20-mA loop interface and J2 the EIA RS232C interface. These connections are right-angle headers and are labelled TTY and EIA, respectively. In addition, they are keyed by having one pin removed: pin 1 on J1 (TTY) and pin 5 on J2 (EIA). The mating socket for the connector should have the corresponding hole plugged so that the two connectors cannot be inadvertently misconnected.

Operation

Reference should be made to the technical data sheet for the CDP1854 UART for Mode 1 operation details.

The crystal-controlled oscillator circuit and the divide-by-N counter CD4059AE provide a clock for the UART at a frequency 16 times the rate selected by the user via the baud rate switch, as required by the UART.

The clear-to-send-in signal CTS-IN from the connector J2 to the UART may be left floating if desired, and it will assume the true state at the UART. The clear-to-send-out signal CTS-OUT is driven by the data-available signal DA from the UART with a trailing-edge delay. This signal may be used for handshaking, for example, between two UART Modules. This output may be made true all the time by changing Link 6 (LK6) to the A position.

To operate the paper-tape reader, an output instruction 67 is issued with the data byte containing a one in bit 7 (most significant bit). The J-K flip-flop U12 is triggered to the set state by this command, making the signal PT RDR low, which enables the tape reader. As soon as the tape reader starts to transmit data, the signal Serial Data In (SDI) causes the J-K flip-flop (U12) to be triggered to the reset state. As a result, one byte is transmitted to the UART and the tape is stopped before the next byte. Another 67 instruction, therefore, must be issued for each successive byte.

Literature

Operator Manual for the RCA COSMAC Development System II CDP18S005, MPM-216.

Technical Data for the CDP1854, Universal Asynchronous Receiver/Transmitter (UART).

CDP18S508

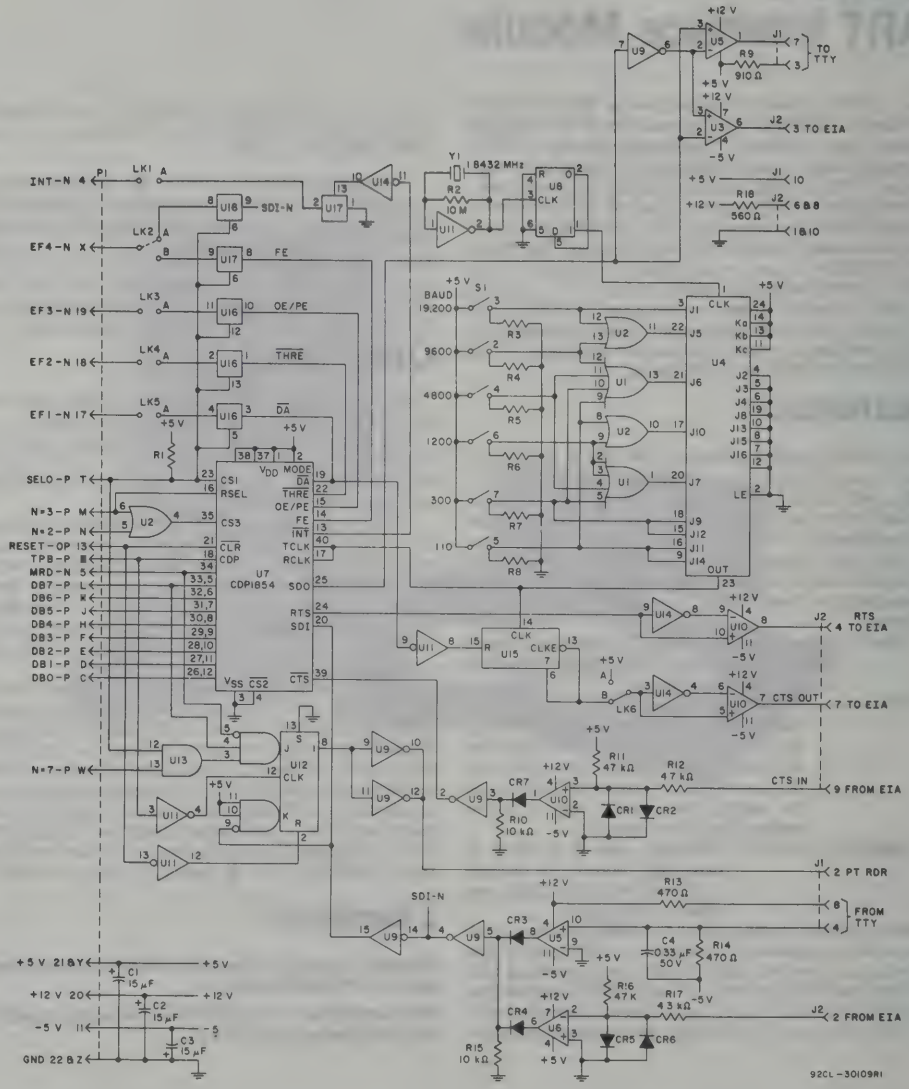


Fig. 1 — UART Interface Module CDP18S508 Logic Diagram

Parts List

C1, C2, C3 = 15 μF, ± 20%, 50 V
C4 = 0.33 μF, ± 20%, 50 V
CR1 through CR7 = 1N914
J1, J2 = connector (mates with connector comprised of
housing – AMP 1-86148-2
contact – AMP 86016-1
keying plug – AMP 87077-1)
R1, R3 through R8 = 22 kilohms, ± 5%, ¼ W
R2 = 10 megohms, ± 5%, ¼ W
R9 = 910 ohms, ± 5%, ¼ W
R10, R15 = 10 kilohms, ± 5%, ¼ W
R11, R16 = 47 kilohms, ± 5%, ¼ W
R12 = 4.7 kilohms, ± 5%, ¼ W
R13, R14 = 470 ohms, ± 5%, ¼ W
R17 = 4.3 kilohms, ± 5%, ¼ W
R18 = 560 ohms, ± 5%, ¼ W
S1 = DIP, 7 position
U1 = CD4072BE, dual 4-input OR gate
U2 = CD4071BE, quad 2-input OR gate
U3, U6 = CA3140S, op amp
U4 = CD4059AE, programmable divide-by-N counter
U5, U10 = CA324E, quad op amp
U7 = CDP1854, UART
U8 = CD4013BE, dual D-type flip-flop
U9 = CD4049BE, hex buffer/converter
U11, U14 = CD4069BE, hex inverter
U12 = CD4096BE, hex inverter
U13 = CD4081BE, quad 2-input AND gate
U15 = CD4017AE, decade counter/divider
U16, U17 = CD4016BE, quad bilateral switch
Y1 = 1.8432-MHz crystal

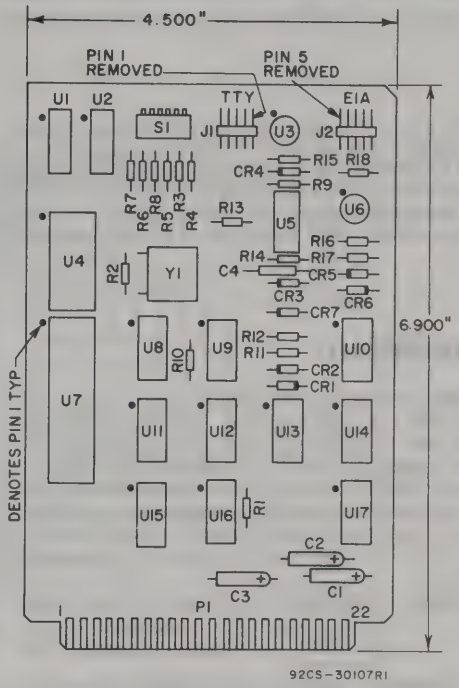


Fig. 2 – UART Interface Module CDP18S508 Layout Diagram

CDP18S510
COSMAC Byte I/O Module

The Byte I/O Module CDP18S510 is a printed-circuit card designed to provide the COSMAC Development System CDS II (CDP18S005) with four input-output channels, each one-byte (8 bits) wide. The Module provides two connectors with identical pin designations, each providing a one-byte input port and a one-byte output port as well as handshaking lines.

Installation

The Byte I/O Module CDP18S510 may be installed in any I/O slot in the CDS Card Nest. Slot 24 is usually used for disk and 14 for the terminal interface. Locations 14 through 18 and 21 through 24 provide all the signals required by this Module except the I/O address lines. These lines are chosen by the user. The combination of Select and N-Decode lines chosen must be unique so that no combination is used twice in the system. They are connected as follows:

Select – Wire-wrap to pin T the I/O select line chosen from SEL2 through SEL7 (SEL0 and SEL1 are assigned to specific I/O functions).

N Decode – Wire-wrap to pins M and N the decoded N lines chosen from N=1 through N=7. Pin M enables input port A and output port A; Pin N enables input port B and output port B.

Multiple Byte I/O Modules may be installed as required up to the availability of unique select addresses.

Operation

System Reset clears all ports.

The output ports latch the data at the trailing edge of TPB. The strobe output (OUT STB) signals that the data is latched. This pulse lasts until the leading edge of the next TPB (4 μs). A clear line is provided for resetting the data latches if desired. Two flag lines are provided to signal the system via EF2 and EF4. These signals may be used as data request signals, ready signals, or as two additional data bits.

The input ports latch the data at the trailing edge of the input strobe signal. When the input strobe is high, the latches are data following. A pull-up resistor is provided, therefore, so that this line may be unused. With the pull-up resistor, the input data is always available to the system. When an input strobe signal is used, the system is notified via EF1 or EF3 that a byte has been latched into the port. This flag line is also sent to the input device as INDA-N and its positive edge indicates that the system has taken the byte. If the input strobe is not used, no flags are generated.

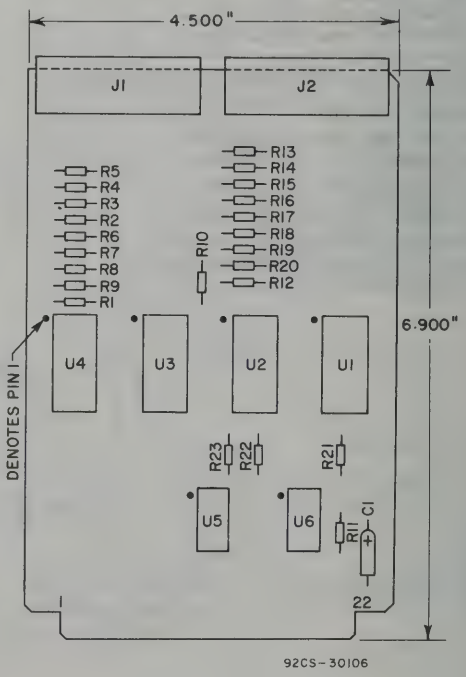


Fig. 1 – Byte I/O Module CDP18S510 Layout Diagram

Parts List

C1 = 15 μF, ± 20%, 20 V
J1, J2 = connector (mates with 26-contact ribbon cable connector 3M#3429-1002 or equivalent.
R1 through R23 = 22 kilohms, 5%, ¼ W
U1 through U4 = CDP1852D, 8-bit I/O port
U5 = CD4081BE, quad 2-input AND gates
U6 = CD4016AE, quad bilateral switch

Literature

Operator Manual for the RCA COSMAC Development System II CDP18S005, MPM-216.

Technical Data for the CDP1852D, 8-Bit Input/Output Port.

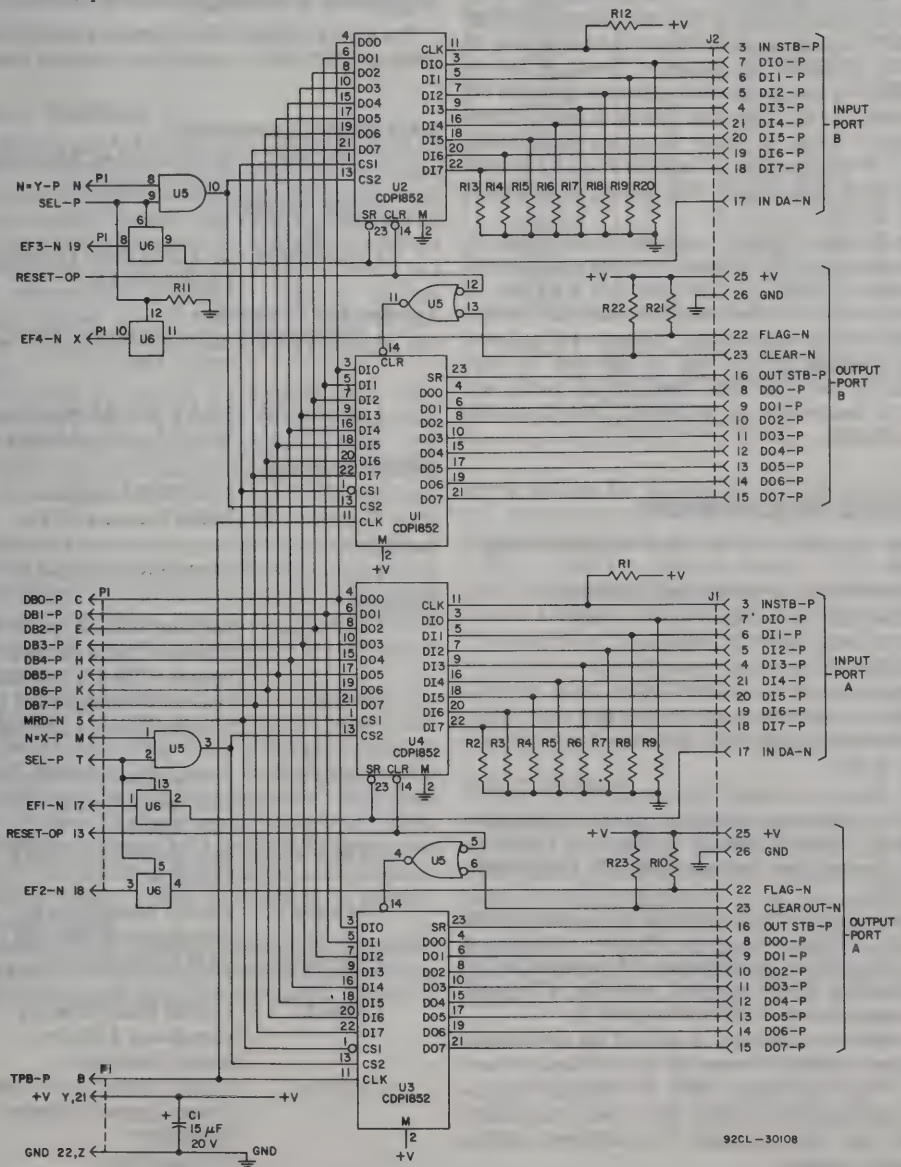


Fig. 2 – Byte I/O Module CDP18S510 Logic Diagram

CDP18S837

RCA COSMAC Disk Operating System Upgrade Package

This booklet discusses the components of RCA COSMAC Disk Operating System Upgrade Package CDP18S837 and gives instructions for modification of the RCA COSMAC Development System (CDS II) CDP18S005 to incorporate and utilize the software for the COSMAC Disk Operating System (CDOS). These instructions apply to CDS II model CDP18S005 having a RAM complement expanded to 12 kilobytes and equipped with Floppy Disk System (CDP18S805 V1, V2, or V3).

After the data terminal requirements are discussed, the components of the Upgrade Package are described and details of installation and assembly are given. A startup procedure is then described, and the booklet concludes with a description of hardware and software options available to the user to enhance the performance of the COSMAC Development System upgraded to incorporate the COSMAC Disk Operating System (CDOS).

Terminal Requirements

A data terminal having the following characteristics is required:

1. EIA RS232C or 20-mA loop interface.
2. Selectable baud rates (110, 300, 1200, 4800, 9600, or 19,200 baud).
3. Parity disable feature (parity is not generated or checked by CDS).
4. ASCII code with eight data bits and one or more stop bits (CDS generates two stop bits).

NOTE: Item four is under software control and may be changed by the user program. For further information consult the **Operator Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007**, MPM-232.

To assure more reliable operation of all types of data terminals utilizing the EIA RS232C interface, a modification should be made at the P1 connector on the EIA Interface Cable supplied with the COSMAC Development System CDP18S005 (CDS II).

The cable wire connected to pin 7 of the ten-terminal P1 connector should be moved to pin 8 of the same connector. With this change, Data Set Ready, Clear-to-Send, and Data Carrier Detect will be held permanently high for the data terminal. No additional cabling changes are required.

Upgrade Package CDP18S837

The RCA COSMAC Disk Operating System Upgrade Package CDP18S837 includes the following items:

RAM Memory Components

1 CDP18S621 or 1 CDP18S621V1	RCA COSMAC Microboard 16-Kilobyte RAM,
or	
2 CDP18S623	RCA COSMAC Microboard 8-kilobyte RAM

Terminal I/O Components

1 CDP18S508	RCA COSMAC UART Interface Module
or	
1 CDP18S641	RCA COSMAC Microboard UART Interface Module

PROM Component

1 UT21	2708 PROM programmed with Utility Program UT21

Software

1	CDOS System Diskette

Literature

1 MPM-232	**Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**
1 PD19	Product Description for UART Interface Module CDP18S508
or	
1 MB-641	Product Description for Microboard UART CDP18S641
1 File No. 1193	Data Bulletin for UART CDP1854
1 MB-621 or 1 MB-621V1	Product Description for Microboard 16-Kilobyte RAM CDP18S621, V1,
or	
1 MB-623	Product Description for Microboard 8-Kilobyte RAM CDP18S623
1 PD37A	RCA COSMAC Disk Operating System Upgrade Package CDP18S837
1	Warranty Card

Description of New Components

The modifications required to incorporate the CDOS Disk Operating System software with the CDS II include the installation of memory modules, the extraction of the Terminal Interface Module, the insertion of the UART Module, and the addition of PROM UT21, a programmed 2708 containing Utility Program UT21. A brief description of the functions of these new components follows.

Memory Modules

The minimum RAM required for CDOS operation includes 12 kilobytes in the address range 9000 -BFFF and 12 kilobytes in the address range 0000 -2FFF. Any additional memory in the area below address 8000 will be used by the Editor to expand its buffer area or by the Macroassembler as extra area for symbol tables and macro definitions. It is necessary, however, to keep RAM contiguous in the area below 8000. In this upgrade, 16 kilobytes of RAM will be located in low memory.

CDOS loads and runs in the upper memory area. Other system programs, such as the Macroassembler and Editor, load starting at address 0000. The CDP18S837 Upgrade Package includes 16-kilobytes of RAM but assumes that the system to be modified already has at least 8 kilobytes of additional RAM beyond the 4 kilobytes supplied with the basic CDS. If additional RAM is needed, extra RAM modules such as the CDP18S205V1 4-Kilobyte RAM, the CDP18S620 Microboard 4-Kilobyte RAM, or the CDP18S623 Microboard 8-Kilobyte RAM should be ordered and installed.

For non-Microboard modules, such as the CDP18S205V1, that do not contain on-board bank-select decoding, the Bank Select Signals generated by the CDS Address Latch and Bank Select Module CDP18S206 must be used as board enables. Refer to the section "Memory Addressing and Expansion" in the **Operator Manual for the RCA COSMAC Development System II CDP18S005, MPM-216**, for more details on this subject. Table I gives a summary of the Memory Bank Select signals.

Microboard RAM modules contain on-board address latches and decoding and require the setting of switches to select the address range of the module. Tables of switch settings for the various modules supplied with this upgrade package are given in the section **Installation and Assembly**.

Table I - Memory Bank Select Signals

Signal Name	Slot 10 Pin No.	Address Range Enabled	Notes
BS0-P	W	0000-0FFF	1
BS1-P	20	1000-1FFF	1
BS2-P	19	2000-2FFF	1
BS3-P	L	3000-3FFF	
BS4-P	K	4000-4FFF	
BS5-P	J	5000-5FFF	
BS6-P	H	6000-6FFF	
BS7-P	F	7000-7FFF	
BS8-P	E	8000-8FFF	2
BS9-P	C	9000-9FFF	3
BSA-P	5	A000-AFFF	3
BSB-P	4	B000-BFFF	3
BSC-P	3	C000-CFFF	
BSD-P	M	D000-DFFF	
BSE-P	A	E000-EFFF	
BSF-P	N	F000-FFFF	

Notes: 1. Required minimum.
2. Do not use; assigned to Utility Program.
3. Required for CDOS.

Fig. 1 shows a memory map of CDS after the modifications described in this booklet have been made. The 16 kilobytes of RAM supplied with this Upgrade Package will be located in low memory and the existing 12 kilobytes of RAM, assumed to be in modules of 4 kilobytes each, will be moved to upper memory. Installation instructions for this changeover are given in the subsequent section **Installation and Assembly**.

UART Module

Terminal communications for the upgraded CDS II are performed through the UART Interface Module CDP18S508 or CDP18S641. The original Terminal Interface Module CDP18S507 must be removed from slot 14 to avoid conflict between the two interfaces. If more than one UART Module is used in the system, the one used as the terminal interface should be appropriately marked.

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The UART Module will be under Group 1 control, just as the original Terminal Interface Module was, and will not interfere with any other modules under different Group Select numbers.

The following I/O assignments are made for the UART Module:

Instruction		Action
62	OUT 2	Writes data to the Transmitter Holding Register.
6A	IN 2	Reads data from the Receiver Holding Register.
63	OUT 3	Writes a Control byte to the UART.
6B	IN 3	Reads Status bytes from the UART.
67	OUT 7	Controls PT RDR output; not presently used.

Signals between the UART module and the terminal are given in Table II. Note that not all UART signals are actually sent through the standard cables.

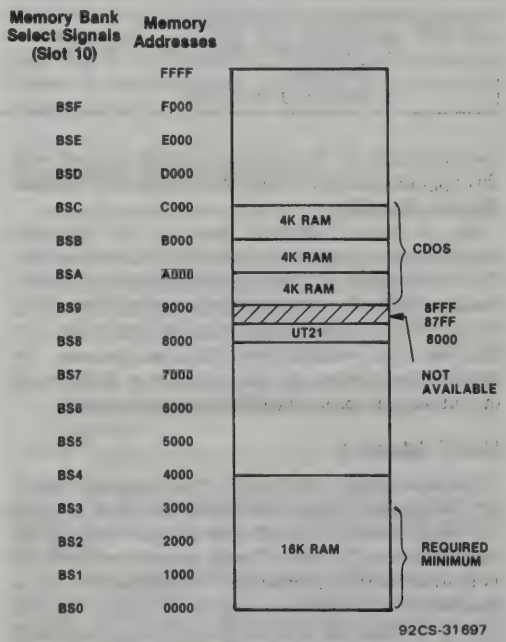

Fig. 1 - CDS III memory map.

Table II - Terminal Interface Cabling

	Teletypewriter Terminal (TTY)	
CDS Side P1	Terminal Side P2	Signal
8	6	Data from TTY (Current Source)
7	8	Data to TTY (Current Source)
3	7	Data to TTY (Current Return)
4	5	Data from TTY (Current Return)
10	15	$+V_{DD}$
2	13	Paper Tape Control
	EIA RS232C Terminal	
P1	**P2**	**Signal**
1	1	Ground
2	2	Data to CDS
3	3	Data to Terminal
10	7	Signal Ground
8*	8	Clear to Send, Data Set
6	6,5	Ready, and Data Carrier Detect - all held high by CDS

*Note: After suggested modification.

Utility Program UT21

To handle the data terminal interfacing via the UART module, a new Utility Program UT21 is provided in the UT21 PROM (a programmed 2708). Details of this new Utility Program are given in the **Operator Manual for the RCA COSMAC DOS Operating System (CDS III) CDP18S007**, MPM-232. In summary, all old commands such as ?M and $U are identical. A new command, $C, causes CDOS to load automatically if the system diskette is in drive 0. It is equivalent to the $L command with unit 0 and track 01 used automatically.

A second difference is that a carriage return or line feed character is not necessary after the RESET, RUNU sequence to establish the terminal baud rate. That rate is established in hardware by switches on the UART module. The asterisk prompt character "*" will appear immediately after a RESET, RUNU sequence and the CDS will be ready for operation in the full-duplex mode. If half duplex is desired instead, the **first** character typed must be a Line Feed. Operation will

then proceed in half duplex. Thus, the startup procedure for UT21 is identical to that of UT20 for half-duplex operation. For full-duplex operation, however, the initial Carriage Return can be omitted.

The routines in the UT20 concerned with terminal timing have been eliminated from the UT21, and READ operations may be immediately followed by TYPE's without a delay. Consequently, the routines TIMALC, DELAY, and TYPE5D are not shown in the **Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-232. The effects of calling DELAY (for example, from a previously written program) will simply be an immediate return to the caller without any delay being generated. Calling TYPE5D is the same as calling TYPE5. Register RC must still contain #80EF, as before, when UT21 routines are called. Programs using TIMALC will require modification to permit use with UT21.

Floppy Disk Interface

No change is required to the Floppy Disk interface. If the CDS is not already equipped with a Floppy Disk System, one should be ordered (CDP18S805V1 for 115 V, 60 Hz operation or CDP18S805V3 for 220 V, 50 Hz) and installed in accordance with the instructions given in the **RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual**, MPM-217.

Installation and Assembly

This section provides detailed installation and assembly instructions for modifying a CDS II equipped with Floppy Disk Option for operation with the COSMAC Disk Operating System (CDOS) software. Because many of the slots in the CDS backplane are keyed, it may be necessary to remove or adjust the keys to accommodate the new modules when the modifications described below are made.

Table III is a list of CDS II backplane wiring before modification. It is reproduced here for convenient reference. It should be noted that CDS backplane connections have unusual sized pins — 0.015″ by 0.041″. For wiring, equipment such as OK Machine (Bronx, N.Y.) electric-powered wire-wrapping tool Model EW 7D or Model G-100 with bit WB2644M and sleeve P3032LN, or equivalent, should be used. Cards inserted in these connectors should have beveled edges to avoid deforming the contacts.

Utilization of UT21 Utility Program

UT20 is contained in its entirety in two PROM's (U7 and U9) on the ROM/RAM module CDP18S401. Only one of these PROM's (U7), however, needs to be changed to upgrade to UT21. Two procedures are provided for modifying a CDS II to utilize the UT21 Utility Program. Procedure A substitutes the UT21 for the UT20 program and permits utilization of the Microterminal CDP18S021 option. Procedure B adds the UT21 capability and permits switching to either UT20 or UT21 by means of S1. Procedure B, however, does not permit use of the Microterminal CDP18S021.

Procedure A - Substitution of UT21 for UT20

1. Remove the ROM/RAM module CDP18S401 from slot 9 of the CDS II module nest.
2. Remove ROM U7 from its socket on the module. See Fig. 2.
3. Install the PROM UT21 provided with the Upgrade Package into socket U7. Be careful to observe polarity.
4. Make sure Switch S1 is in the down position.
5. Re-insert the modified ROM/RAM module CDP18S401 into slot 9.

Procedure B - Addition of UT21

1. Remove the ROM/RAM module CDP18S401 from slot 9 of the CDS II module nest.
2. Install PROM UT21 into socket U8. Be careful to observe polarity.
3. Re-insert the modified ROM/RAM module CDP18S401 into slot 9.
4. Switch S1 into the up position.

Installation of Memory Modules

The Upgrade Package contains either one CDP18S621 16-kilobyte RAM, one CDP18S621V1 16-kilobyte RAM, or two CDP18S623 8-kilobyte RAM's. The installation instructions for these components are given in Steps B-E below. It is assumed that the RAM modules present in the CDS II are the CDP18S205V1 4-kilobyte RAM's. The instructions for the relocations of the addresses, in accordance with the memory map given in Fig. 1, for the CDP18S205V1 RAM's are given in Step A below.

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Table III - CDS CDP18S005 Backplane Wiring Schedule Before Modification (cont'd on next page)

Pin No.	Memory	Address Latch and Bank Select	CPU	I/O Decode	I/O [3]	Control	Pin No.
Location →	(1-9)	(10)	(12)	(13)	(14-18,21-24)	(25)	
A	—	BSE-P	TPA-P	TPA-P	TPA-P	TPA-P	A
B	SPARE	—	TPB-P	TPB-P	TPB-P	TPB-P	B
C	DB0-P	BS9-P	DB0-P	DB0-P	DB0-P	DB0-P	C
D	DB1-P	RNU-P	DB1-P	DB1-P	DB1-P	DB1-P	D
E	DB2-P	BS8-P	DB2-P	DB2-P	DB2-P	DB2-P	E
F	DB3-P	BS7-P	DB3-P	DB3-P	DB3-P	DB3-P	F
H	DB4-P	BS6-P	DB4-P	DB4-P	DB4-P	DB4-P	H
J	DB5-P	BS5-P	DB5-P	DB5-P	DB5-P	DB5-P	J
K	DB6-P	BS4-P	DB6-P	DB6-P	DB6-P	DB6-P	K
L	DB7-P	BS3-P	DB7-P	DB7-P	DB7-P	DB7-P	L
M	A0-P	BSD-P	A0-P	SEL0-P	—	A0-P	M
N	A1-P	BSF-P	A1-P	SEL1-P	—	A1-P	N
P	A2-P	A15-P	A2-P	SEL2-P	N = 4-P	A2-P	P
R	A3-P	A14-P	A3-P	SEL3-P	N = 5-P [4]	A3-P	R
S	A4-P	A13-P	A4-P	SEL4-P	N = 6-P	A4-P	S
T	A5-P	—	A5-P	SEL5-P	—	A5-P	T
U	A6-P	—	A6-P	SEL6-P	—	A6-P	U
V	A7-P	—	A7-P	SEL7-P	—	A7-P	V
W	MWR-N	BS0-P	MWR-N	N = 7-P	N = 7-P [5]	—	W
X	BSN-P [1]	MBDS-N	CPU PWR	N = 6-P	EF4-N	RUN-N	X
Y	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Y
Z	GND	GND	GND	GND	GND	GND	Z

Notes
[1] BSN-P: No printed wires. Wire-wrap to user's choice, BS0 through BSF. See Wire-Wrap Connections Below.
[2] Location 8 only.
[3] Locations 19 and 20: all pins open except V_{DD} and GND.
[4] Location 24 only (Disk interface).
[5] Location 14 only (Terminal interface).

These instructions are necessarily typical and are based on the assumption that the CDS II is equipped with 4-kilobyte RAM's. For other combinations of RAM modules and address ranges, the user should refer to (1) the installation information in the instruction booklets for the specific Microboard RAM modules used; or, (2) the section "Memory Addressing and Expansion" in the **Operator Manual for the RCA COSMAC Development System II CDP18S005**, MPM-216, for non-Microboard or user-designed RAM modules.

Step A - Module CDP18S205V1 (4 kilobytes)

1. Remove the three RAM modules from the CDS II module nest.
2. Perform the following CDS II backplane modifications:
   a. Connect slot 10, pin C to slot 8, pin X (BS9)

Table III - CDS CDP18S005 Backplane Wiring Schedule Before Modification (continued)

Pin No.	Memory	Address Latch and Bank Select	CPU	I/O Decode	I/O [3]	Control	Pin No.
Location →	(1-9)	(10)	(12)	(13)	(14-18,21-24)	(25)	
1	TPA-P	TPA-P	DMAI-N	N = 1-P	DMAI-N	—	1
2	TPB-P [2]	UA15-N	DMAO-N	N = 2-P	DMAO-N	DMAO-N	2
3	SPARE	BSC-P	ANY I/O-P	N = 3-P	—	ANY I/O-P	3
4	—	BSB-P	INT-N	N = 4-P	INT-N	RNU-P	4
5	MRD-N	BSA-P	MRD-N	MRD-N	MRD-N	MRD-N	5
6	A12-P	A12-P	Q-P	N = 5-P	Q-P	Q-P	6
7	A11-P	A11-P	SC0-P	—	SC0-P	SC0-P	7
8	A10-P	A10-P	SC1-P	—	SC1-P	SC1-P	8
9	A9-P	A9-P	CLEAR-N	TLIO-N	—	CLEAR-N	9
10	A8-P	A8-P	WAIT-N	—	—	WAIT-N	10
11	−5 V	A0-P	—	—	−5 V	EX CLR-P	11
12	EX WAIT	A1-P	EX CLK	—	—	EX WAIT-P	12
13	CLK OUT	A2-P	CLK OUT	RESET-OP	RESET-OP	RESET-OP	13
14	—	A3-P	N0-P	N0-P	—	N0-P	14
15	—	A4-P	N1-P	N1-P	—	N1-P	15
16	RESET-OP	A5-P	N2-P	N2-P	—	N2-P	16
17	—	A6-P	EF1-N	—	EF1-N	—	17
18	—	A7-P	EF2-N	—	EF2-N	—	18
19	V_{DD} [2]	BS2-P	EF3-N	—	EF3-N	EF3-N	19
20	+12 V	BS1-P	EF4-N	+12 V	+12 V	+12 V	20
21	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	21
22	GND	GND	GND	GND	GND	GND	22

Notes

Wire-Wrap Connections

RAM SELECT	BS0-P	10-W to 8-X
ROM SELECT	BS8-P	10-E to 9-X
TERM. SELECT	SEL0-P	13-M to 14-M
DISK SELECT	SEL0-P	13-M to 24-W
2-LEVEL I/O	TLIO-N	13-9 to 13-22 (Jumper)
I/O DECODE	RNU-P	13-7 to 24-4

b. Connect slot 10, pin 5 to slot 7, pin X (BSA)

c. Connect slot 10, pin 4 to slot 6, pin X (BSB)

3. Insert CDP18S205 RAM modules into slots 6, 7, and 8.

Step B - Microboard RAM Link Connections

CDP18S621 - Connect pins 1 and 16 of link LK2A.

CDP18S621V1 - Connect pins 3 and 6 of link LK 1A.

CDP18S623 - Connect pins 1 and 16 of link LK2A.

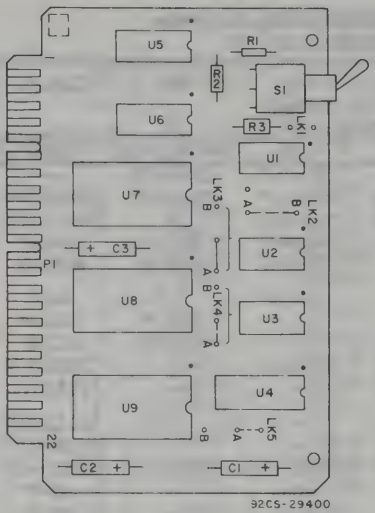
Step C - CDS Backplane Modification

Add a jumper wire from slot 10, pin D to pin 3 of any slot 1 - 9 (RNU-P signal).

Step D - Address Range Selection

This step selects the address 0000 to 3FFF for the CDP18S621 and CDP18S621V1, and 0000 to 1FFF for one of the two CDP18S623's and 2000 to 3FFF for the second CDP18S623. Table IV

CDP18S837



C1, C2, C3 = 15 μF, ±20%, 20 volts
R1, R2, R3 = 22 kilohms, ±5%, ¼ watt
S1 = SPDT
U1 = CD4023BE U5, U6 = CDP1856D
U2 = CD4069BE U7, U9 = 2708
U3 = CD4012BE U8 = Socket for Micro-
U4 = CDP1824D terminal or UT21 ROM
Note: S1 UP enables ROM in U8.
S1 DOWN enables ROM in U7.

Fig. 2 - ROM/RAM Module CDP18S401 layout diagram.

shows the switch settings for other address ranges.

CDP18S621 - Set both rockers of switch S1 to open.

CDP18S621V1 - Set both rockers of switch S1 to open.

CDP18S623 - On one board, set all three rockers of switch S1 to open. On the other board, set rockers 2 and 3 of S1 to open, and rocker 1 to closed.

Step E - Installation in CDS

Install the memory modules(s) in any unused memory slots (1 to 5).

Table IV - RAM Board Address Range Assignments

CDP18S621 or CDP18S621V1

Switch S1		Address Range
Rocker 1	Rocker 2	Enabled
O	O	0000-3FFF
C	O	4000-7FFF
O	C	8000-BFFF
C	C	C000-FFFF

CDP18S623

Switch S1			Address Range
Rocker 1	Rocker 2	Rocker 3	Enabled
O	O	O	0000-1FFF
C	O	O	2000-3FFF
O	C	O	4000-5FFF
C	C	O	6000-7FFF
O	O	C	8000-9FFF
C	O	C	A000-BFFF
O	C	C	C000-DFFF
C	C	C	E000-FFFF

O = OPEN C = CLOSED

Installation of UART Interface Module CDP18S508

For the installation of the UART Interface Module CDP18S508 or CDP18S641 some simple modifications are required on the module and on the CDS II backplane. These modifications are described below.

Procedure A - For CDP18S508

Modifications to CDS II

1. Remove Terminal Interface Module CDP18S507 from slot 14.
2. On backplane, remove the wire connecting slot 13, pin M to slot 14, pin M.
3. On backplane add jumper wires as follows:

From Slot 14 Pin No.	To Slot 13 Pin No.	Signal Name
T	M	SEL0-P
M	3	N=3-P
N	2	N=2-P

Modifications to UART Module CDP18S508

1. Connect A and C of link LK2 together. See Fig. 3.
2. Set switch S1 to match baud rate of terminal to be used.
3. Insert the UART Module in CDS II I/O slot 14.

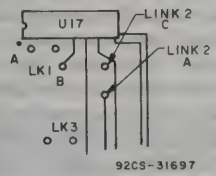


Fig. 3 - Location of A and C of link LK2 on UART Interface Module CDP18S508.

Procedure B - For CDP18S641

Modifications to CDS II

1. Remove Terminal Interface Module CDP18S507 from slot 14.
2. On backplane, add jumper wires as follows:

From Slot 14 Pin No.	To Slot/ Pin No.	Signal Name
9	Slot 14/Pin 13	RESET-OP
14	Slot 13/Pin 14	N0-P
15	Slot 13/Pin 15	N1-P
16	Slot 13/Pin 16	N2-P

Modifications to UART Module CDP18S641

1. Connect pins 7 and 8 of link LK24.
2. On link LK14, short pins 5-6 and open pins 7-4.
3. Set switch S1 to match the baud rate of the terminal to be used.
4. Insert the UART Module in CDS II I/O slot 14.

Startup Procedure

After the modifications and additions to the CDS II are made to enable it to utilize the software for the COSMAC Disk Operating System, the following startup procedure should be undertaken.

Connect the EIA or TTY (20 mA) cable between the newly installed UART Module and the data terminal. Put the terminal in the line mode and check that the baud rate set by the UART Module switch and that of the terminal are matched. CAUTION: The maximum recommended baud rate for 20-mA operation is 1200 baud. Set the terminal for full-duplex operation. Connect the Floppy Disk Dual-Drive Mechanism CDP18S801 to the CDS II in accordance with the instructions given in the **RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual**, MPM-217.

Power on the CDS II, the data terminal, and the Floppy Disk Dual-Drive Mechanism, in that order. Press the RESET and then the RUNU switches on the CDS II. The asterisk prompt character "*" should appear immediately indicating that the Utility Program UT21 is running. Place the CDOS system diskette in Drive 0 and then type $C. The operating system should load and sign on with a ">" prompt in a few seconds. Follow the procedures given in the **Operation Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-232, for using CDOS commands.

Upgrading Pre-CDOS Software

Programs developed for earlier CDS systems which do not use disk I/O routines can be upgraded to run under CDOS by use of a CDOS copy routine provided for this purpose. Versions of the software for the PROM Programmer CDP18S480 and for the Micromonitor Operating System (MOPS) CDP18S831 modified for use under CDOS are available from your local RCA sales or field engineering representative or from RCA Microprocessor Systems Marketing, Somerville, N.J.

User Options

Optional Accessories

COSMAC Micromonitor CDP18S030. The Micromonitor, a powerful self-contained debugging tool, may be used to considerable advantage with the COSMAC Development Systems. It permits in-circuit debugging in real time of both hardware and software. The Micromonitor includes a built-in 28-key keyboard with an 8-digit LED display, 14 status indicator lights, and software debugging routines. It significantly increases the speed with which hardware and software can be integrated and software debugged. It is specifically recommended for the development of programs of more

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than one kilobyte in length. (Part number: CDP18S030; product description: PD18; instruction manual: MPM-218)

PROM Programmer CDP18S480. This hardware/software package when installed in the CDS enables the user to program the RCA CDP18U42, Intel 2704, 2708, 2758, 2716, or equivalent PROM's. In addition, it will read, but not program, 1702-type PROM's thereby providing a means of copying these PROM's onto other PROM's. The software is available on disk, paper tape, and magnetic tape in cassette. (Part number: CDP18S480—disk version, CDP18S480V1—paper-tape version, CDP18S480V2—cassette version; product description: PD22; instruction manual: MPM-222)

Optional Software

PLM 1800 High-Level-Language Compiler CDP18S839. Provided on a diskette, this software package is designed to accelerate program development in COSMAC DOS Development System (CDS III) CDP18S007V1 or CDP18S007V3. It has features similar to those of the many well-known high-level languages such as PL/1, ALGOL and PASCAL. Use of the PLM language encourages structured programming and, hence, provides easy readability and maintenance. Its scoped procedures and control structures also support modular programming (Part number: CDP18S839; product description: PD39; instruction manual: MPM-239)

Basic 1 Compiler/Interpreter CDP18S834. This high-level language supplied on a diskette is designed to facilitate rapid program development with the COSMAC CDOS Development Systems (CDS III) CDP18S007V1 and V3. Basic 1 is an easily learned language for the beginning programmer and may be extended indefinitely by the addition of machine language routines. (Part number: CDP18S834; product description: PD34; instruction manual: MPM-234)

Binary Fixed-Point Arithmetic Subroutines CDP18S826. This software package is a set of 16-bit 2's-complement fixed-point arithmetic subroutines including addition, subtraction, multiplication, and division. Also included are binary-to-BCD and BCD-to-binary conversion subroutines plus various utility routines. These subroutines are available on disk, paper tape, or magnetic tape on cassettes. (Part number; CDP18S826—disk version, CDP18S826V1—paper-tape version, CDP18S826V2—cassette version; product description: PD6; instruction manual: MPM-206)

Binary Floating-Point Arithmetic Subroutines CDP18S827. This software package is a set of 32-bit floating-point arithmetic subroutines including addition, subtraction, multiplication, division, sine, cosine, arctan, natural log, e^X, and square root. Also included are binary-to-BCD and BCD-to-binary conversion plus other utility routines. These subroutines are available on disk, paper tape, or magnetic tape on cassettes. (Part number; CDP18S827—disk version, CDP-18S827V1—paper-tape version, CDP18S827V2—cassette version; product description: PD7; instruction manual: MPM-207)

COSMAC Micromonitor Operating System (MOPS) CDP18S831. This software package enhances the capabilities of the Micromonitor by providing interfacing to disk files. MOPS provides the user with such options as saving the state of the CPU for subsequent reloading and driving the Micromonitor with commands from a disk file to perform automated testing. (Part number: CDP18S831; product description: PD31; instruction manual: MPM-231)

CDP18S837

COSMAC Disk Operating System
Upgrade Package CDP18S837
RCA
COSMAC
UART Interface Module
CDP18S508
RCA 1800
MICROPROCESSORS
Operator Manual for the RCA COSMAC
CDOS Development System (CDS III)
CDP18S007

Software

CDP18S827
COSMAC Floating-Point Arithmetic Subroutine Diskette

The COSMAC Floating-Point Arithmetic Subroutine package on a floppy diskette CDP18S827 is a set of 32-bit arithmetic subroutines designed to be operated on COSMAC CDP1802 Microprocessor Systems including the COSMAC Development System (CDS) CDP18S005. The subroutines are coded in Level I assembly language and require approximately 2 kilobytes of memory space. The floating-point binary number is represented by eight exponent bits and 24 mantissa bits. The most significant bit of each indicates the sign. The range of decimal numbers that can be represented by the 32 bits is $0.294 \times 10^{-38} \leq FPN \leq 1.7014 \times 10^{38}$

A detailed description of these subroutines is given in the Manual **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207. The subroutines are available in source language on a floppy diskette CDP18S827 for use with RCA Floppy Disk System CDP18S805, a mass memory storage unit designed to work with the CDP18S005 COSMAC Development System (CDS). The Floating-Point Arithmetic Subroutine Diskette can also be used with Floppy Disk System CDP18S800 and the CDP18S004 COSMAC Development System.

Functions

The Floating-Point Arithmetic Subroutine Diskette CDP18S827 includes 18 subroutines. Ten are arithmetic subroutines, six are utility subroutines, and two are for format conversion. Appropriate selections from the set of subroutines may be made for the calculations required in a specific application.

Floating-Point Arithmetic Subroutines. The arithmetic functions included in this floating-point arithmetic package are:

1. 32-bit addition
2. 32-bit subtraction
3. 32-bit multiplication yielding 32-bit products
4. 32-bit division yielding 32-bit quotient
5. Transcendental function: sine
6. Transcendental function: cosine
7. Transcendental function: arctan
8. Natural log
9. e^x
10. Square root

Utility Subroutines. A set of special utility subroutines allows the user to save and restore a group of registers on a stack. These registers are used by the arithmetic function subroutines to store an operand. Other utility subroutines allow constants to be pushed onto the stack.

Format Conversion Subroutines. Two format-conversion subroutines are included for interfacing the system to binary-coded-decimal-oriented peripheral hardware. These subroutines provide BCD-to-floating-point and floating-point-to-BCD conversions.

The Standard Call and Return Technique described in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201, can be used for all the subroutines.

Timing

Timing measurements at a 6.4-MHz clock rate for the best and worst cases of the various arithmetic and format conversion subroutines for the CDP1802 are given in the tabulation below. The timing, however, can be rescaled by a change in the system clock rate.

Arithmetic Function	Best (ms)	Worst (ms)	Format Conversion	Best (ms)	Worst (ms)
Add	0.53	7.8	Floating-		
Subtract	0.81	8.1	Point-BCD	2.3	7.5
Multiply	43.8	47.5	BCD-Floating-		
Divide	30	32.5	Point	7.5	1600
Sine	113	116			
Cosine	102	113			
Arctan	85.9	109			
Natural log	78.1	188			
e^x	71.9	125			
Square root	155	312			

Literature

Further information on the Floating-Point Arithmetic Subroutine Package CDP18S827, including data storage convention and register allocation, is provided in the Manual **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors** MPM-207. General information on the RCA1800 microprocessor series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor** MPM-201. Another software package encompassing 16-bit 2's-complement arithmetic is described in the manual **Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206.

CDP18S831

COSMAC Micromonitor Operating System (MOPS)

The Micromonitor Operating System (MOPS) is a software package developed to enhance the capabilities of the RCA CDP18S030 or CDP18S030A Micromonitor. The Micromonitor is a self-contained, powerful debugging tool for use with any system based on the CDP1802 COSMAC Microprocessor. It permits in-circuit debugging in real time so that both hardware and software problems can be efficiently identified. The Micromonitor Operating System (MOPS) CDP18S831 enhances Micromonitor performance with COSMAC Development Systems CDS IV (CDP18S008), CDS III (CDP18S007, or CDS II (CDP18S005) equipped with Floppy Disk System CDP18S805.

The Micromonitor Operating System CDP18S831 includes a MOPS Diskette CDP18S830, a UART Module CDP18S508, and a Connecting Cable CDP18S511.

System Functions

The Micromonitor Operating System CDP18S831 provides an extended Micromonitor-type command set with commands of the following types:

1. Commands that allow the user to conveniently switch Micromonitor commands and responses to and from a variety of system peripherals.
2. Single commands that allow a more complete interrogation of the CPU state.
3. Commands for saving the system-under-test memory, registers, etc., in a disk file or for loading the system-under-test from a disk file.
4. Commands that allow a degree of automation in system debugging and testing.

With MOPS, the debugging techniques available to the user range from simple terminal-Micromonitor dialog to fully automated hands-off system testing with commands coming from disk files.

System Operation

The user system configuration required for the utilization of MOPS is shown in Fig. 1. Depending on user directives, commands to the system are input at the terminal or are taken from command files on disk. Likewise, system responses can be directed to the terminal, to a disk file, or to both.

Standard Micromonitor commands entered to the system are directed to the Micromonitor through its serial interface, UART Module CDP18S508. Commands from the extended MOPS command set are "trapped" and processed by the operating system. In either case, the Micromonitor Operating System provides line-by-line command editing capability.

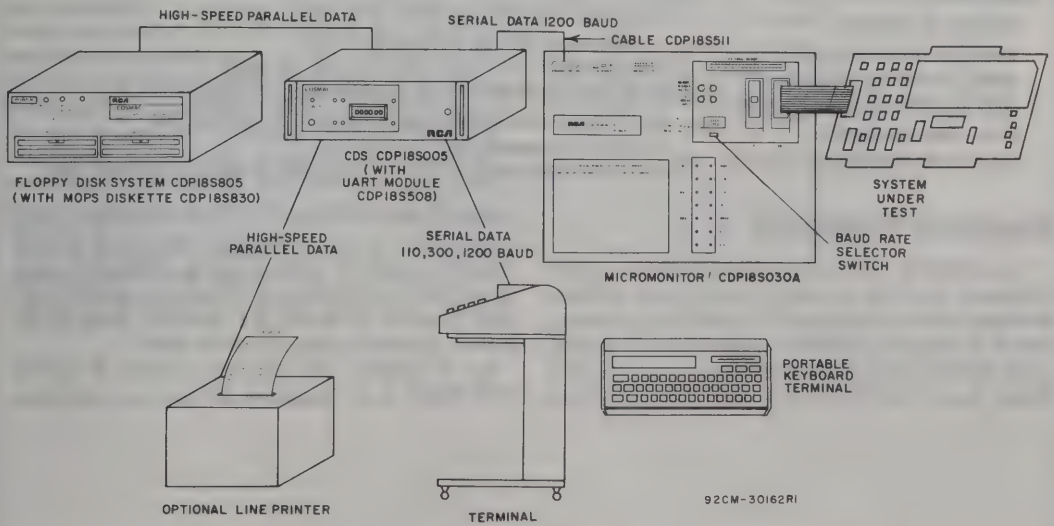


Fig. 1 - System configuration for utilization of MOPS software.

CDP18S831

Summary of MOPS Commands

$TI	Set the terminal as the input device
$TO	Set the terminal as the output device
$DKI FILENAME#	Set the disk as the input device
$DKO FILENAME#	Set the disk as the output device
$DKC	Close a disk file
$O FILENAME#	Set both terminal and disk as output devices
?CPU	Dump the CPU state to the output device(s)
?MRn hhhh	Dump memory pointed to by register n for hhhh bytes
$Haaaa$_1$ aaaa$_2$ FILENAME#	Hold the state of the machine on disk
$L FILENAME#	Load a disk file
$MSG	Type a message to the terminal
$WB	Wait for a break condition
$WT dddd	Wait for dddd (decimal) seconds
◆ $MB	Force a manual break
!J hhhh	Set the index J to hhhh
!J+	Increment the index J
!J-	Decrement the index J
?J	Question the current value of the index J
◆ !BP aaaa . . .	Declare software breakpoints on executable addresses
◆ !BR aaaa . . .	Remove breakpoint addresses from current list
◆ ?BP	Question the current software breakpoint addresses
$GO TO %*label*	Search forward for %*label* and if found continue at that point, else end
* $IF v_1 *op* v_2 THEN GO TO %*label*	If the relation is true, execute "go to", else proceed
$DKW FILENAME#	Write a command sequence to a disk file
$DKL FILENAME#	List a disk file to the terminal
$DKP FILENAME#	Print a disk file to the line printer
$U	Return to CDOS##

NOTES:
aaaa is an address
aaaa$_1$ is starting address
aaaa$_2$ is ending address
uutt denotes unit uu, track tt
d is a decimal digit
label is an alphanumeric label

◆ In MOPS version 2.0 requiring an 8K system.
* *v* is one of [Rn, D, F, X, P, IE, T, Q, W, C, EM, IR, EFf, Ip, J, #hhhh, PROMPT, ., %]
op is one of [=, >, <, EQ, LT, GT, LE, GE, NE]
MOPS is supplied with the unitrack (uutt) version, also, for use with Development System (II) CDP18S005 where uutt denotes unit uu track tt.
In the unitrack (uutt) version, $U returns to the monitor program.

Support Systems

The COSMAC Micromonitor CDP18S030A is a self-contained, real-time, in-circuit hardware and software debugging tool for use with any CDP1802 Microprocessor system. It has a portable keyboard terminal and display, status indicator lights, software debugging routines, and a 20-mA loop or EIA RS232C interface for auxiliary serial communication. Its primary use is for prototype-system software and hardware debugging. Because of its easy portability, however, it is also useful as a field service tool. In addition, it can be used as a versatile production tester. (Part number: CDP18S030A; Product Description: PD18D; Instruction Manual: MPM-218B).

The COSMAC Development System II (CDS) CDP18S005 is an interactive software and hardware

prototyping system for the development of products based on the RCA 1800 family of microprocessor parts. It uses the CDP1802 Microprocessor as the CPU and includes a RAM-based resident Editor and Assembler. The CDS has space for additional I/O devices so that it can be used for hardware prototyping as well as program development. In small-volume applications it can be used as the major building block for dedicated microcomputers. Optional equipment frequently ordered to expand the system's capabilities include the CDP18S030A, CDP18S480, CDP18S837, CDP18S805, CDP18S831, various software packages, and any standard terminal. (Part number: CDP18S005; Product Description: PD16C; Instruction Manual: MPM-216).

The COSMAC Floppy Disk System II CDP18S805 is a dual-drive single-density, 500-kilobyte mass-memory storage unit designed to work with the CDP18S005 COSMAC Development System II to facilitate rapid program development. In comparison with systems using other media, the Floppy Disk System reduces program development time significantly. The system includes the CDP18S801 disk-drive mechanism, the CDP18S813 interface module, the CDP18S825 system software, a CDP18S829 blank diskette, and various manuals. Various software packages and blank disks may be used with this product. (Part number: CDP18S805; Product Description: PD17; Instruction Manual: MPM-217).

The COSMAC Development System CDS III, CDP18S007V1, CDP18S007V3 (Overseas Version) is a packaged software/hardware development system that includes a chassis with associated electronics, a dual floppy-disk drive, a disk management system, a macroassembler, an editor, utilities, 28 kilobytes of RAM, and terminal interfaces. Sockets are available for expansion of memory and I/O. This expansion can be accomplished using accessory modules listed in this section or any CDP18S600 series product. The system is typically expanded by adding the CDP18S030A, CDP18S480, CDP18S831, various software packages, and a CRT (CDP18S040). Part number: CDP18S007; Product Description: PD16C; Instruction Manual: MPM-232.

The COSMAC Development System CDS IV CDP18S008V1, CDP18S008V3 (Overseas Version) is a software development system that includes the Micromonitor Operating System (MOPS). The CDP18S008 consists of a development station, dual floppy-disk drive, and a Micromonitor (in-circuit-emulator). The development station includes a 12-inch CRT that provides a green-on-dark background of 80 characters by 24 lines, power supplies, full ASCII keyboard with 14 special function keys for full-screen editing, 60 kilobytes of RAM, two CMOS CDP1802 microprocessors, a disk interface (PERTEC), line-printer interface (Centronics parallel), MOPS (Micromonitor Operating System) interface, and built-in PROM programmer. Additional hardware consists of a Micromonitor for in-circuit real-time debugging and a 500-kilobyte floppy disk system for mass storage. Software included is the standard utility in ROM, a new high-power level II macroassembler, resident text editor, full-screen editor in ROM, CDOS disk file management and operating system, and software for MOPS and the PROM Programmer. Part number: CDP18S008, Product Description: PD-8; Instruction Manual: MPM-235.

Literature

The Micromonitor Operating System (MOPS) CDP18S831 Users' Guide MPM-231A, describing the installation, startup, and use of MOPS, is included with the unit.

System Components

Supplied as part of the Micromonitor Operating System (MOPS) CDP18S831 package are the following items:

MOPS Diskette CDP18S830 (Containing both 4- and 8-kilobyte RAM versions)

UART Module CDP18S508

Interconnecting Cable CDP18S511

Micromonitor Operating System (MOPS) CDP18S831 User's Guide, MPM-231A

CDP18S831

RCA 1800
Micromonitor Operating System
(MOPS) CDP18S831
Users' Guide

CDP18S834

BASIC1 High-Level Language Compiler/Interpreter

The BASIC1 Compiler/Interpreter, provided on a diskette, is a high-level language software package designed to simplify program development on the COSMAC DOS Development System (CDS III) CDP18S007 and on COSMAC Development System IV CDP18S008. An excellent language for the beginner, BASIC1 is easily learned and facilitates the rapid development of elementary application programs. A feature of BASIC1 is that it can form the core of a system whose facilities, limited only by the system memory, may be extended indefinitely by the addition of machine language routines.

The Compiler/Interpreter gives the user the option of (1) developing and running programs in BASIC1 directly, or (2) converting these programs to executable object code capable of running at a greater speed.

The interpreter allows the user to write programs in BASIC1 with line numbers for later execution or without line numbers for immediate execution. The disk-related statements incorporated in the interpreter allow the programmer to save programs on a floppy disk for later recall.

The compiler enables the programmer to take any stored program written in BASIC1 and translate it into assembly language, giving the user the flexibility of specifying where in memory the program, variables, and stack are to reside. The output of the compiler is assembled by the COSMAC assembler (ASM8) to produce the executable object code. Programs compiled and assembled run at speeds much greater than those run directly through the interpreter.

Features

The BASIC1 Compiler/Interpreter can handle lines of up to 77 characters in length. Line numbers can range from 1 to 32767. Multiple statements per line are accepted. Numbers can be entered in decimal (—32767 to +32767) or hexadecimal (#0000 to #FFFF). Variables are designated by any single capital letter.

BASIC1 performs fixed-point arithmetic. Expressions are composed of one or more numbers, variables, and/or functions joined together by operators (+, —, /, *, @) and possibly grouped by parentheses. Expressions are evaluated modulo 2^{16}.

The functions BASIC1 has in its repertoire include MOD, AND, OR, XOR, MAX, MIN, SGN, ABS, HEX, RND, INP and USR. The USR function is important in that it allows the user to extend the features of BASIC1 by means of machine language subroutines and allows for the exchange of data between the assembly language subroutines and the BASIC1 program. BASIC1 also allows direct CDP1802 input and output port control within the language itself. This control is accomplished by the INP (port) function and the OUTPUT (port) statement.

The types of statements available to the programmer include the following:

Comments and Declarations: REM, !
Assignment: LET
Control: GOTO, GOSUB, RETURN, END
Conditional: IF
Input/Output: INPUT, PRINT, OUTPUT,
Disk Related: WFLN, RFLN, DOUT, DIN,
CLOSE, WEOF, TIN, TOUT,
NOUT
System Control: NEW, RUN, LIST, RDOS

Loading and Operating BASIC1

Loading and operating BASIC1 on a COSMAC Development System is a simple procedure. To load the interpreter, the user places the disk in one of the disk drives and types BASIC1.INT:X where X is the drive (0 or 1) the disk has been placed in. This command loads the interpreter. The program initializes itself and th delivers its colon prompt ":" to indicate it is now in the enter mode and the user can begin entering a BASIC1 program.

To load the compiler, the user places the disk in one of the disk drives and types BASIC1.CMP:X, where X is the drive (0 or 1) the disk has been placed in. This command loads the compiler and beings execution. The compiler then issues its normal user prompts.

Error Messages and Program Debugging

Whenever the BASIC1 interpreter detects an error in a statement, it generates an error message consisting of an exclamation point "!" followed by a decimal number. The number signifies the type of error. If an error is detected during program execution, the line number of the offending statement is also given. BASIC1 lends itself to the use of dummy stop or print statements to reveal whether the flow within the program is proper or to permit the examination of variables at convenient points during program execution.

CDP18S834

Literature

Further information on BASIC1 Compiler/Interpreter is given in the Manual **Use of BASIC1 Compiler/Interpreter CDP18S834 with the RCA COSMAC DOS Development System (CDS III)**, MPM-234.

Information on the RCA COSMAC DOS Development System CDP18S007V1 and V3 is given in the manuals **Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-232, and in the **Hardware Reference Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-233.

Information on the RCA COSMAC Development System IV CDP18S008 is given in the manuals **Operator Manual for the RCA COSMAC Development System IV CDP18S008**, MPM-235, and in the **Hardware Reference Manual for the RCA COSMAC Development System IV CDP18S008**, MPM-236.

General information on the RCA 1800 Microprocessor Series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

Binary arithmetic software packages on disk are also available for use on the COSMAC Development Systems. The COSMAC Microprocessor Fixed-Point Binary Arithmetic Subroutines (CDP18S826) are described in Product Description PD6 and the COSMAC Microprocessor Floating-Point Arithmetic Subroutines (CDP18S827) are described in Product Description PD7. Additional information on these arithmetic diskettes is given in the manuals **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206, and in **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207.

Other languages available for use on COSMAC Development Systems include BASIC2 High-Level-Language Interpreter CDP18S840, PLM-1800 High-Level-Language Compiler CDP18S839, and Micro Concurrent Pascal (Cross Compiler CDP18S844 and Interpreter/Kernel CDP18S852 and CDP18S853.)

BASIC2 is described in Product Description PD40. Additional information is given in the **BASIC2 High-Level-Language Interpreter CDP18S840 User Manual**, MPM-840.

PLM-1800 is described in Product Description PD39. Additional information is given in the **User Manual for the RCA COSMAC PLM-1800 High-Level-Language Compiler**, MPM-239.

MicroConcurrent Pascal is described in Product Description PD44.

CDP18S834

for use with
COSMAC Development Systems

CDP18S835
VIS Interpreter

The VIS Interpreter, on diskette CDP18S835 and on cassette tape CDP18S835V2, is an interpretive language developed specifically to support the CDP1869 and CDP1870/CDP1876 Video Interface System (VIS). The interpretive commands allow the user to control the VIS to provide displays of text, graphics, and motion on a cathode-ray tube screen in black and white or color. The Interpreter is useful on any system containing the VIS chip set and is particularly supportive of the CDP18S661, Microboard Video-Audio-Keyboard Interface.

The VIS Interpreter is open ended, allowing the user to add interpretive commands for special purposes. By use of the supplied source, routines that are not required for the particular application may be deleted. The source routines may also be adapted to the user's own program and are documented to provide a guide to the programming of the VIS. The Interpreter as delivered is a 3-kilobyte program and requires a minimum of 64 bytes of RAM.

The source file for the VIS Interpreter is provided on diskette compatible with the CDP18S008 Development System (CDOS Operating System). It is capable of both NTSC and PAL operation. The CDP18S835V2 is intended for use with the CDP18S694 and CDP18S695 Microboard Computer Development Systems.

Structure

The VIS Interpreter is based on:

1. Sixteen general-purpose, eight-bit variables.
2. An eight-bit accumulator and overflow flag.
3. A page memory pointer.
4. A character memory pointer.
5. A main memory pointer.
6. A hitflag.

Variables. The sixteen eight-bit variables are usable for general data storage. They are also usable as objects of arithmetic and logical operations. This use includes operations involving two variables or one variable with the accumulator (ACC). The variables are also used to contain control information for some interpretive instructions. Additional data storage may be accomplished by the use of instructions that allow direct storage and load from memory. Instructions are provided to test the content of the variables including comparisons against constants, ACC, and other variables.

Accumulator (ACC). A single eight-bit accumulator is provided in the interpreter. This accumulator is used as an operand and to store the result in arithmetic and logical operations. Instructions are provided to display the contents of the ACC by copying it to the page memory in two methods. In the first method, the contents of the ACC are placed in the page memory unchanged except the most significant bit is set equal to one. In the second method, the contents are taken and treated as two hexadecimal digits and the two ASCII codes for the digits are placed in page memory. Transfers to and from main memory, the variables, and the page memory are supported.

Overflow Flag. A flag is provided to indicate overflow on all arithmetic operations. After addition, the flag is a one if a carry occurs and a zero if no carry occurs. After subtraction, the flag is a one if no borrow occurs and a zero if a borrow occurs. Instructions for testing the value of the flag are provided.

Page Memory Pointer (PMP). The Interpreter references the page memory by means of the page memory pointer (PMP). The PMP is a sixteen-bit memory pointer into the page memory. The value of the PMP normally ranges from FC00H to FCEFH for half resolution and FC00H to FFBFH for full resolution. (H indicates hexadecimal notation.) The PMP is initialized to FC00H and the initial home address is zero, which results in the PMP pointing to the upper left screen location. The PMP may be directly accessed or loaded by use of interpretive instructions.

Character Memory Pointer (CMP). The Interpreter references the character memory by means of the character memory pointer (CMP). The CMP is an eight-bit pointer into the character memory. In order to reference a given character, the CMP must be loaded with the same value that, if stored in page memory, would display the character. Instructions are provided for the transfer of the CMP to and from the ACC and variables, along with increment and decrement instructions. No checks are made or limits placed on the value of the CMP, and thus it may be used in systems that allow up to 256 characters.

Main Memory Pointer (MMP). The Interpreter allows direct references to memory by means of the main memory pointer (MMP). The MMP is a sixteen-bit pointer into the system memory. Instructions are provided to load, save, and decrement its value. All Interpreter instructions that involve direct memory reference use the MMP. Instructions are provided to store and load the variables, ACC, and other pointers by means of the MMP. No checks are provided on the value of the MMP.

Hitflag. The Interpreter provides instructions that allow the user to display characters on the screen and to move these characters. In order to check for "colliding" objects, the interpreter maintains a hitflag. This hitflag is set true if any write to page memory or character memory is addressed to a non-zero location. The hitflag is cleared when an interpreter instruction performs a write to page or character memory locations that are zero. Instructions are provided to test the hitflag.

Instructions. The Interpreter is provided with 109 instructions.

Literature

Further information on the VIS Interpreter is provided in the manual VIS Interpreter CDP18S835 User Manual, MPM-835A. Information on the Video Interface System (VIS) CDP1869 and CDP1870/CDP1876 is available in data sheet file number 1197.

CDP18S839

PLM-1800 High-Level-Language Compiler

The PLM-1800 High-Level Language Compiler CDP18S839, provided on a diskette, is a software package designed to accelerate program development on the COSMAC DOS Development System (CDS III) CDP18S007V1 or CDP18S007V3 and on the COSMAC Development System IV CDP18S008V1, V3, V5, and V7. It has features similar to those of many well-known high-level languages such as PL/1, ALGOL, and PASCAL. Use of the PLM language encourages structured programming and, hence, provides easy readability and maintenance. Its scoped procedures and control structures also support modular programming.

The PLM Compiler automatically creates code for complex conditions and signed sixteen-bit arithmetic expressions, and it performs systematic register and storage allocations. Because of these features, the programmer has more time to concentrate on the application requirements.

The PLM Compiler also supports CDP1802 features. It contains built-in functions such as shift operations (SHL, SHR, SCL, SCR), data conversions (LOW, HIGH), and declaration-based information functions (ADDR, LENGTH). Other built-in functions or predeclared variables (Q, MEMORY, DMAPTR, STACKPTR, EF1, EF2, EF3, EF4, CARRY) allow access to CDP1802-based hardware. Data transfers through the I/O ports are supported by INPUT and OUTPUT. The interrupt mechanism is programmable with the INTERRUPT attribute for procedures and the ENABLE and DISABLE statements. A built-in procedure, TIME, allows time delays based on the microprocessor clock.

Code written in PLM may be integrated with assembly code through the Compiler's in-line-code feature. In addition, the Compiler produces CDP1802 assembly code that can be combined with other assembly-time code.

PLM operates directly with the COSMAC Development System CDP18S008. When used with a CDP-18S007 COSMAC Development System, PLM requires 60 kilobytes of read-write memory and a data terminal or console. Required software is the CDOS System Diskette, version 2.2 or later (supplied with the CDP18S007), and the PLM-1800 High-Level-Language Compiler on diskette CDP18S839. Documentation is provided with the CDOS Development System and with the PLM-1800 High-Level-Language Compiler diskette.

Features of PLM

The features of the PLM-1800 High-Level-Language Compiler CDP18S839 include the following.

Data Description:

CONSTANTS – decimal, hexadecimal, octal, binary numbers, and strings of characters.

VARIABLES – two types; may be aggregated into arrays or initialized.
BYTE – 8-bit value
ADDRESS – 16-bit value; may contain the address of another variable.

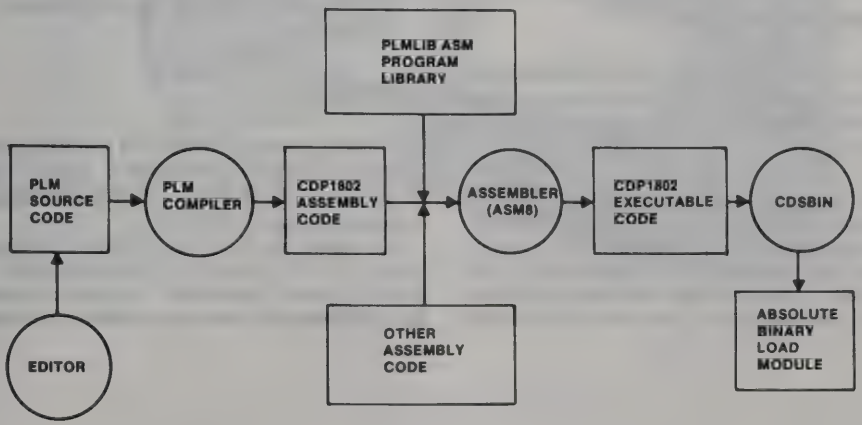


Fig. 1 - Block diagram of program development cycle using the PLM Compiler.

CDP18S839

EXPRESSIONS – permit the following operations:
arithmetic +, –, *,/, MOD
logical AND, OR, XOR, NOT
equality and ordering =, <>, <,>, < =, >=.

Statement Description:

ASSIGNMENT – allows replacement of variable's value by evaluation of an expression; multiple assignments are possible in one statement.

IF..THEN..ELSE – allows execution of a group of statements based on a condition. IF statements may be nested.

DO..END – allows execution of a group of statements.

ITERATIVE DO – allows looping based on an interative variable whose increment is controllable with an optional BY clause.

DO..WHILE – allows looping based on a condition.

PROCEDURE – contains executable instructions and local variable declarations. Procedures may be recursive if declared with REENTRANT attribute. Procedures may take on function attribute.

CALL – subroutine invocation.

GO TO, GOTO – branching capability to labels within scope rules of the language.

Compiler Features:

In-line assembly code capability
Output listing controls
Assembly code output

Operating with PLM

After a program is generated in the PLM language, the first step for using the Compiler is to place the PLM diskette in disk drive 0. The user then invokes compilation of the file by typing

PLM fname.ext:x

where fname.ext is the user's file name and x is the drive. If errors occur during compilation, they are transmitted to the development system terminal device as well as to an output file of PLM source code interlisted with CDP1802 assembly code. Another output file equating assembly names and PLM names is also generated by the Compiler. The error messages indicate the nature of the error, the number of the line in which the error occurred, and where in the line the error was detected.

A program development cycle using the PLM-1800 High-Level-Language Compiler is given in Fig. 1. The Compiler accepts source code written in the PLM language, and generates the equivalent assembly code that can subsequently be assembled into CDP1802 executable code.

Sample Program

A sample program using PLM is given in Fig. 2. This program will sort an array by means of a method called "bubblesort."

```
DO;
/*THIS IS A BUBBLESORT PROGRAM*/
DECLARE A(10) ADDRESS INITIAL
  (33, 10,99,60, 162,3,3,272,98,2);
DECLARE (I, SWITCHED,J) BYTE, TEMP ADDRESS;
  SWITCHED = 1;
  DO WHILE SWITCHED = 1;
    SWITCHED = 0;
    DO I = 1 TO 9;
        J = I + 1;
        IF A(I) > A(J) THEN
            DO;
              SWITCHED = 1;
              TEMP = A(I);
              A(I) = A(J);
              A(J) = TEMP;
            END;
    END;
  END;/*OF WHILE*/
END;
/*NOW COMPLETED SCAN WITHOUT SWITCHING*/
EOF
```

Fig. 2 - PLM "bubblesort" program.

Literature

Further information on the PLM-1800 High-Level-Language Compiler CDP18S839 is given in the **User Manual for the RCA COSMAC PLM-1800 High-Level-Language Compiler**, MPM-239.

Information on the RCA COSMAC Development System IV CDP18S008V1, CDP18S008V3, CDP-18S008V5, and CDP18S008V7 is given in two manuals **Operator Manual for the RCA COSMAC Development**

System IV CDP18S008, MPM-235, and **Hardware Reference Manual for the RCA COSMAC Development System IV CDP18S008**, MPM-236.

Information on the RCA COSMAC DOS Development System CDP18S007V1 and CDP18S007V3 is given in the two manuals **Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-232, and **Hardware Reference Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-233.

General information on the RCA 1800 Microprocessor Series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

Binary arithmetic software packages on disk are also available for use on the COSMAC DOS Development System CDS III. The COSMAC Microprocessor Fixed-Point Binary Arithmetic Subroutines (CDP18S826) are described in Product Description PD-6, and the COSMAC Microprocessor Floating-Point Arithmetic Subroutines (CDP18S827) are described in Product Description PD-7. Additional information on these arithmetic diskettes is given in the manuals **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206 and **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207.

Two application notes are available for PLM. They are ICAN-6928 "Interfacing PLM Code to CDOS System Functions" and ICAN-6918 "A Methodology for Programming COSMAC 1802 Applications Using Higher-Level Languages."

CDP18S840

BASIC2
High-Level Language Interpreter

The BASIC2 Interpreter CDP18S840 is a high-level-language software package on diskette designed to simplify program development on COSMAC Development System IV (CDP18S008V1 and V3). With additional RAM it may also be used with COSMAC DOS Development System III (CDP18S007V1 and V3). BASIC2 is a high-level interactive language that is easily learned and readily used by beginning programmers. BASIC3, a tape-based counterpart to BASIC2, is provided with the Microboard Computer Development System MCDS (CDP18S693 and CDP18S694).

A special Run-time BASIC, the CDP18S842, is available on ROM for use in custom applications not requiring disk I/O. With Run-time BASIC the user obtains a 4-kilobyte savings in the memory required. Run-time BASIC provides an excellent way to generate software quickly in a high-level language for use in any Microboard system. The system can be configured to suit the application. The software for the application is generated by the user in a development system (COSMAC Development System III or IV using BASIC2, or the Microboard Computer Development System MCDS using BASIC3) and installed in memory (RAM or ROM). Then with Run-time BASIC in the system, execution of the user program can begin immediately.

BASIC2 provides full access to the CDP1802 I/O constructs including two-level I/O, interrupt, DMA, external flags, and the Q output. It allows calls to user machine-language routines and provides I/O instructions for any added Microboards.

Features

- **Floating-Point and Integer Numbers**
- **Line-Editing Capability**
- **More than 70 Statements and Functions**
- **One- or Two-Dimensional Numerical Arrays**
- **Disk I/O**
- **Trace Function for Debugging**
- **Memory-Saving ROM Version for Turnkey Applications**
- **Uses CDP1802 Microprocessor Constructs**

Enhanced Features Using CDP1802 Special Capabilities

- **DMA Capability**
- **Two-Level Input/Output Capability**
- **BASIC Statements to Enable and Disable Interrupts**
- **Vectored Interrupts and Interrupt-Handling Routines in BASIC**
- **Flag and Q Status Commands**
- **Set Q Statement**
- **Machine Language Subroutines**
- **Easy Multi-Station Operation**

Description

The BASIC2 Interpreter features over seventy statements and functions including both transcendental and string functions. It provides both immediate and program modes of operation. It features one- or two-dimensional numerical arrays up to a maximum size of 255 x 255 and one-dimensional string arrays up to 255. It has direct memory access capability and can handle two-level input and output statements. For programming ease, it also has line-editing capability.

The **statements** and **functions** available on BASIC2 are shown in Table 1.

Arithmetic Capabilities

BASIC2 is capable of handling both integer and floating-point numbers. Both types are stored as 32-bit signed numbers. In the case of floating-point numbers, eight bits define the exponents and 24 bits the mantissa. The range of numbers is:

Integer: -2147483648 to +2147483647
Floating point: -.17E38 to +.17E38

Integer numbers are accurate over the entire range, but floating-point numbers are accurate to approximately six mantissa digits, although up to nine digits are allowed on data entry. Two- or four-digit hexadecimal numbers can also be entered directly.

Memory Requirements

BASIC2 requires a development system that is equipped with the COSMAC Disk Operating System (CDOS) and with an additional 16 kilobytes of memory for the BASIC2 Interpreter. The interpreter is loaded into the 16-kilobyte block of memory that is above the block used by CDOS; that is, C000H through FFFFH (H indicates hexadecimal notation). The memory can be either RAM or ROM. The interpreter requires additional RAM in low memory beginning at 0000H. The amount of RAM available in low memory controls the size of the programs that may be written. The locations 0000H through 040FH are used as work space by the interpreter. When the system is first initialized, the interpreter begins a search of

Table I - Statements and Functions

Command		
BYE	ENINT	NEW
CLD	EOD	MEM
CLS	EOP	RENUMBER
DISINT	FORMAT	RUN
EDIT	LIST	TRACE
Comment and Definition		
DEFINT	DIM	RAD
DEFUS	FIXED	REM
DEG	LET	
Control		
END	GOSUB	NEXT
EXIT	GOTO	RETURN
FOR	IF	WAIT
Program Data		
DATA	READ	RESTORE
I/O		
INP	INPUT	POKE
OUT	PRINT	PEEK
QST	TIN	DMAPT
STQ	TOUT	EF
Disk		
CLOSE	DOUT	PSAVE
DIN	DSAVE	RFLN
DLOAD	PLOAD	WFLN
Machine Language Subroutine		
CALL	USR	
Arithmetic		
ABS	INT	RND
ATN	INUM	SGN
COS	LOG	SIN
EXP	MOD	SQR
FNUM	PI	
String		
ASC	LEN	STR$
CHR$	MID$	TAB
FVAL		

memory from 7FFFH downward for RAM and establishes a stack at the top of the last page. The user program and program-generated data are located between the work space and the stack. The map of memory is shown in Fig. 1.

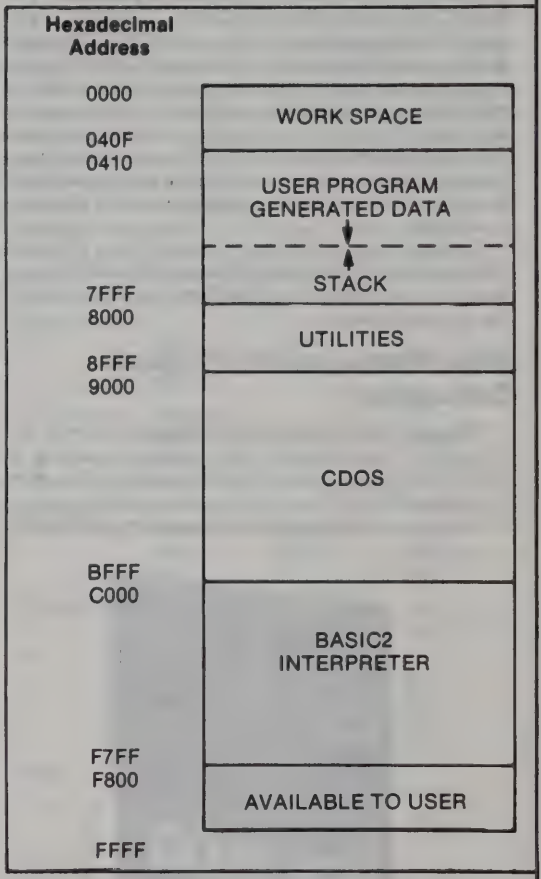


Fig. 1 - Memory Allocations

Creating and Editing Programs

BASIC2 programs can be created and edited by either of two methods. One is by use of the BASIC2 Interpreter; the other is by use of the CDOS editor.

CDP18S840

When the interpreter is used, a program is created by the writing of one or more statements, separated by a colon, on a line and assigning the line a number. While the interpreter is being used, the lines of code can be easily modified by use of the EDIT command statement. The BASIC2 interpreter allows the lines to be entered in any order, but for execution it will automatically rearrange them in numerical sequence. For example, line 10 may be entered before line 5, but in execution line 5 will be executed first. This facility enables the programmer to leave unused numbers between lines so that additional lines can be inserted at a later time. The interpreter always executes the lines in numerical order starting with the lowest line number, thus providing one method of editing a program.

The second method of creating and entering programs is by use of the CDOS editor. This method is described in detail in the manuals for the CDP18S007 and CDP18S008 Development Systems.

Error Messages and Program Debugging

Whenever the BASIC2 interpreter detects an error in a statement, it generates an error message consisting of ERR CODE and a two-digit decimal number followed by the message READY and the : prompt symbol. A listing of the error numbers and their corresponding meanings is provided in the BASIC2 instruction manual. If the error is detected during program execution, the error code is followed by the words AT LINE followed by the line number of the offending statement.

The TRACE command statement is a useful tool for debugging because it allows the user to follow the flow of the program.

Literature

Further information on the BASIC2 Interpreter and on Run-Time BASIC is given in the Manual **BASIC2 High-Level-Language Interpreter CDP18S840 User Manual,** MPM-840A.

Information on the RCA COSMAC DOS Development System CDP18S007V1 and V3 is given in the **Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007,** MPM-232, and in the **Hardware Reference Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007,** MPM-233.

Information on the RCA COSMAC Development System IV CDP18S008V1 and V3 is given in the **Operator Manual for the RCA COSMAC Development System IV CDP18S008, MPM-235,** and in the **Hardware Reference Manual for the RCA COSMAC Development System IV CDP18S008,** MPM-236.

CDP18S842

Run-time BASIC High-Level Language Interpreter

Run-time Basic CDP18S842 is a variant of BASIC2 CDP18S840 and of BASIC3 CDP18S841. It is available in six EPROMs and is especially suited for custom Microboard applications not requiring disk I/O. Run-time BASIC provides an excellent way to generate software quickly in a high-level language for use in any Microboard system. The system can be configured to suit the application. The software for the application is generated by the user in a development system (COSMAC Development System III or IV using BASIC2, or the Microboard Computer Development Systems MCDS using BASIC3) and installed in memory, RAM or ROM. Then, with Run-time BASIC in the system, execution of the user program can begin immediately.

The primary difference between BASIC2 or BASIC3 and Run-time BASIC, other than that there is no program input mode for Run-time BASIC, is that the latter cannot execute PLOAD or PSAVE. See Table I for a list of statements and functions available on Run-time BASIC. The statements CLOSE, DLOAD, DSAVE, WFLN, RFLN, DIN, and DOUT in Run-time BASIC apply to a tape I/O system such as the Microboard Computer Development System MCDS CDP18S693 or CDP18S694. The CDP18S652 Combination Memory and Tape I/O Control Microboard is required for tape I/O with Run-time BASIC.

Memory Requirements

The Run-time BASIC Interpreter is located in memory from 0000H to 2FFFH (H denotes hexadecimal notation) as shown in Fig. 1. The Interpreter starts execution of a user program at 3000H in ROM and generates data in RAM at 9000H. There must be at least 1 kilobyte of RAM available at 9000H for the Interpreter to run. The work pages for Run-time BASIC are at 9000H and 9100H. Any references to the work pages in the user program should be to these addresses and not to the ones for BASIC2 or BASIC3.

Using Run-time BASIC

To generate a Run-time BASIC program from a BASIC2 or BASIC3 program, proceed as follows.

1. Save the BASIC program on tape or disk in ASCII.
2. Determine the RAM requirements for the program.
3. Make a ROM or EPROM containing the program for use with the Run-time Interpreter.

Detailed information on the development of a Run-time Basic program on the CDP18S008 Development System is given in the BASIC2 High-Level-Language Interpreter CDP18S840 User Manual, MPM-840A. Information on the development of a Run-time BASIC program on the CDP18S693, CDP18S694, or CDP-18S695 series of Microboard Computer Development Systems (MCDS) is given in the BASIC3 High-Level Language Interpreter User Manual, MPM-841A.

Table I - Statements and Functions available in Run-time BASIC.

Command			
	CLD	ENINT	
	CLS	FORMAT	
	DISINT		
Comment and Definition			
	DEFINT	FIXED	REM
	DEG	LET	
	DIM	RAD	
Control			
	END	GOSUB	NEXT
	EXIT	GOTO	RETURN
	FOR	IF	WAIT
Program Data			
	DATA	READ	RESTORE
I/O			
	DMAPT	OUT	QST
	EF	PEEK	STQ
	INP	POKE	TIN
	INPUT	PRINT	TOUT
Tape			
	CLOSE	DOUT	WFLN
	DIN	DSAVE	
	DLOAD	RFLN	
Machine Language Subroutine			
	CALL	USR	
Arithmetic			
	ABS	INT	RND
	ATN	INUM	SGN
	COS	LOG	SIN
	EXP	MOD	SQR
	FNUM	PI	
String			
	ASC	FVAL	MID$
	CHR$	LEN	

CDP18S842

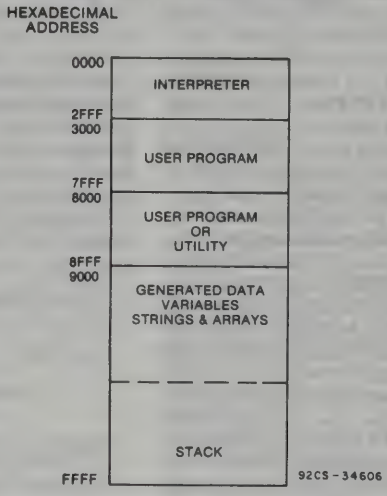


Fig. 1 – Typical memory configuration for Run-time BASIC.

CDP18S843

Assembler/Editor Upgrade Firmware

The Assembler/Editor Upgrade Firmware CDP-18S843 is provided in three 2716 EPROM's and is intended only for upgrading the Microboard Computer Development System (MCDS) CDP18S693 to the CDP-18S694. (Use of the Assembler requires two cassette tape units.) These EPROM's fit the CDP18S652 Microboard Combination Memory and Tape I/O Control Module provided with the CDP18S693 and provide Editor and Assembler capability.

The Text Editor allows the user to generate ASCII files on cassette tape. These files can be Level I CDP1802 language, BASIC3 instructions with line numbers, or simply text. The Editor output file becomes the input file for the assembler. The Editor commands include: Move pointer to beginning of buffer, Move pointer to end of buffer, Move pointer by n characters, Move pointer by n lines, Define input tape, Append lines, Insert text, Delete n characters, Delete n lines, Save n lines, Get saved text, Find text, Substitute text, Define output tape, Type n lines, Write n lines to output tape, Write entire buffer to output tape, Print n lines, Return to UT62, and Quit session and restart Editor.

The Assembler allows the user to convert a Level I source file on tape (source code) into an executable machine language program on another tape (object code). The object code can then be loaded into memory by the UT62 Monitor program for execution, or it can be placed in an EPROM by a PROM programmer. The Assembler permits the user to write programs using convenient mnemonic expressions rather than machine language. It is a two-pass assembler with CDP1800-series Level I syntax. The Assembler also provides error messages to assist in debugging.

Micro Concurrent Pascal

Cross-Compiler CDP18S844 and Interpreter/Kernel CDP18S852 and CDP18S853

Micro Concurrent Pascal (mCP)*, a Pascal dialect, is a high-level language having multi-task capability that is specially suited for program development not only for COSMAC Development Systems or other systems using the RCA 1800 microprocessor series, but also for many other 8-and 16-bit microprocessors. Pascal is a language that is easily written, read, and maintained. mCP has the additional feature that it enables the programmer to solve problems requiring concurrency. RCA Micro Concurrent Pascal, available on either tape or disk media, includes a cross-compiler CDP18S844 and a target system interpreter/kernel CDP18S852 for 8-bit microprocessor systems and CDP18S853 for 16-bit systems. In addition to providing the capabilities of mCP, this package gives the programmer access to the unique features of the RCA 1800-series microprocessors.

The Language

The mCP language provides the user with a Pascal extension that offers the readability, maintainability, and control structures of standard sequential languages plus the flexible data typing of Pascal. Most significantly, however, it offers process and monitor constructs that permit multiple processes to run independently but at the same time to share data and communicate with each other. Interrupt response routines, device drivers, and bit-level manipulations are all programmed in mCP without having to use assembly code. But, for those time-critical routines, resort to assembly code is provided in the language.

Interrupts are programmable in the mCP language through specification of an interrupt table. This table orders the priority of the interrupts and allows proper association of the interrupts with the group number and external flags of the RCA 1800-series two-level I/O convention. In addition to static specification, interrupt priorities may be dynamically altered by means of a single mCP instruction.

RCA 1800 series microprocessor features are directly accessible by means of built-in routines. The mCP programmer may access the external flags, the DMA pointer, and the Q flag. In addition, the mCP input and output instructions (INN and OUT) may be coded for either one-level or two-level I/O. Fig. 1 is an example of an mCP program fragment that transmits a line of characters to the CDP18S641 Microboard UART Interface.

Features of the mCP language include:

1. **Pascal syntax with language constructs for concurrency.**
2. **RCA 1800-series-dependent routines allow the programmer to test external flags, set and test the DMA register, test and set the Q flag, and perform one- or two-level I/O.**
3. **Ability to specify and dynamically alter interrupt priorities for RCA 1800-series microprocessor interpreter/kernels.**
4. **Floating-point arithmetic.**
5. **Bit-level manipulation intrinsics.**
6. **Ability to use assembly language.**
7. **Structured data types.**
8. **Data typing flexibility.**
9. **Separate data types for 8- and 16-bit integers for efficient data storage.**
10. **String manipulation intrinsics.**
11. **Hexadecimal constants.**
12. **Direct hardware addressing (PEEK, POKE, INN, OUT).**

The Cross-Compiler CDP18S844

The mCP package is implemented by a cross-compiler and an interpreter/kernel. The cross-compiler creates mCP pseudo code (mCP p code) which may then be executed by the interpreter with the kernel acting as the program executive performing process switching, process synchronization, and interrupt vectoring. The compiler is free from any target machine dependencies.

The mCP compiler performs extensive compile-time checking, capturing many real-time errors. It offers many compile-time directives such as listing and output code options to ease development and debugging of programs.

The code produced is position-independent, reentrant, and ROMable. An INCLUDE directive allows merging of mCP source files at compile time. mCP cross-compilers are available for Hewlett-Packard, DEC, Data General, and IBM mainframes.

*Micro Concurrent Pascal and mCP are registered tradenames of Enertec, Inc.

They are also available for use on CP/M or UCSD microcomputer systems.

Features of the cross-compiler include:

1. **Operation on many host computers (See Table I).**
2. **Produces reentrant ROMable code.**
3. **Many compile-time options.**
4. **Emission of code for run-time bounds checking.**
5. **Compacted mCP p code.**
6. **Debug options.**
7. **Extensive compile-time checking.**

The Interpreter/Kernel CDP18S852 and CDP18S853

The mCP interpreter/kernel executes p codes from the mCP cross-compiler. The interpreter fetches, decodes, and executes the p codes corresponding to the mCP program. The kernel performs the multiplexing among concurrent processes. It controls access to shared procedures and data that are protected by monitors, the interprocess communication mechanism of the mCP language. Unique to the interpreter/kernel for the RCA 1800-series microprocessor is its ability to handle code to access the external flags, DMA pointer, Q flag, and either one-level or two-level I/O. Another special feature of the 1800 interpreter/kernel is its ability to handle run-time changes of the interrupt priorities. The interpreter/kernel for the CDP1802 microprocessor is 3.6 kilobytes and with **floating-point arithmetic** it is 4.6 kilobytes.

Features of the interpreter/kernel include:

1. **Real-time multi-tasking.**
2. **Interrupt vectoring.**
3. **Relocatability to any memory location of target system.**
4. **Source code provided for customization.**
5. **Portability; because of interpretive approach, mCP programs are portable, thus protecting software investment.**
6. **Compact; typically 3 to 5 kilobytes.**
7. **Stands alone, easily installed, requires no operating system under which to run.**
8. **Unique features of interpreter/kernel for RCA 1800-series microprocessors include routines to access external flags, Q flag, DMA pointer, and either one- or two-level I/O. Also, interrupt priorities may be dynamically altered.**
9. **In addition to the CDP1802, interpreters are available for the Z80, 8080/8085, 8086/88, Z8000, and 68000 microprocessors (mCP interpreter/kernel 8-bit, CDP18S852, for CDP1802, Z80, and 8080/8085; 16-bit, CDP18S853, for 8086/88, Z8000, and 68000).**

Download Circuit

The diagram on the front cover shows a typical program development sequence using mCP. The downloading may be readily accomplished by the use of a switchbox circuit such as that shown in Fig. 2. This circuit, which is also described in the **mCP User's Guide**, may be connected to a COSMAC Development System IV CDP18S008, a COSMAC DOS Development System (CDS III) CDP18S007, a Microboard Computer Development System (MCDS) CDP18S693 or CDP18S694, or through a CDP18S030 Micromonitor to any target system.

The purpose of the switchbox circuit is to permit a terminal to be shared between the cross-compiler system and the target system. The three normal modes of operation of the switchbox circuit are:

1. Connect terminal to target system only.
2. Share MODEM output between the target system and the terminal for downloading.
3. Connect terminal to MODEM for cross-compiler system only.

If the terminal is a 20-milliampere current-loop type, the user should be sure to include the optional components shown in the circuit diagram. P1, a 25-pin EIA male connector, may be plugged into COSMAC Development Systems, the Micromonitor, or the Microboard Computer Development Systems. The Development Systems should be set up for half-duplex operation for downloading. Half-duplex operation is established by setting the duplex switch S3 on the switchbox circuit to the half-duplex position (switch closed —local echo on) and then typing a "line feed" character immediately after the utility program is started.

CDP18S844, CDP18S852, CDP18S853

mCP Compared with Sequential Pascal

mCP has been extended from sequential Pascal in constructs to support concurrency, microprocessor input/output, and interrupt handling. To improve the efficiency of the mCP Compiler, some features of sequential Pascal were deleted. These deletions are dynamic storage, file types, and the GOTO statement. Because predefined functions and procedures in mCP are tailored for concurrency, bit handling, and access to machine features, some functions and procedures are different from the ones found in sequential Pascal. Many, however, are the same.

Literature

A Micro Concurrent Pascal (mCP) User's Guide is supplied with every purchase of mCP. This manual contains twelve chapters which include syntax and semantics of mCP, operating instructions for compilation, description of the mCP interpreter/kernel, debugging hints, examples of mCP programs, and interpreter/kernel details particular to the target system.

A useful reference is the book **The Architecture of Concurrent Programs** by Per Brinch Hansen, Prentice-Hall, Englewood Cliffs, 1977. This book describes the construction of operating systems using the Concurrent Pascal language with which mCP shares the process, monitor, and class constructs.

```
TYPE UART_WRITE=DEVICE_MON (SELECTOR: INT);
PROCEDURE ENTRY WRITE(MESSAGE: LINE; DISP: LINE_DISP);
  VAR I: INT;
      THROWAWAY: INTEGER;
  BEGIN
    I:=1;
    OUT(#BD, CTRL_WORD) (*XMIT REQ., INT. EN., 8 DATA, 2 STOP, NO PARITY*);
    DOIO;
    WHILE (MESSAGE[I] <> NUL) AND (I < LINELENGTH) DO
    BEGIN
      OUT( ORD(MESSAGE[I]), DATA_WORD);
                          (*SEND A CHARACTER*)
      DOIO;
      INC(I);
    END;
    IF (DISP=PROMPT) OR (DISP=NEWLINE) THEN
      BEGIN OUT(ORD(CR), DATA_WORD); DOIO;
            OUT(ORD(LF), DATA_WORD); DOIO;
      END;
    IF DISP=PROMPT THEN
    BEGIN OUT(ORD('>'), DATA_WORD); DOIO; END;
      OUT(#3D, CTRL_WORD); (*TRANSMIT INHIBIT OTHERWISE SAME AS ABOVE*)
      THROWAWAY :=INN(CTRL_WORD);
  END;
BEGIN
  OUT(#3D, CTRL_WORD);
END;
```

Fig. 1 - Sample mCP program. This routine writes a line to the CDP18S641 Microboard UART Interface.

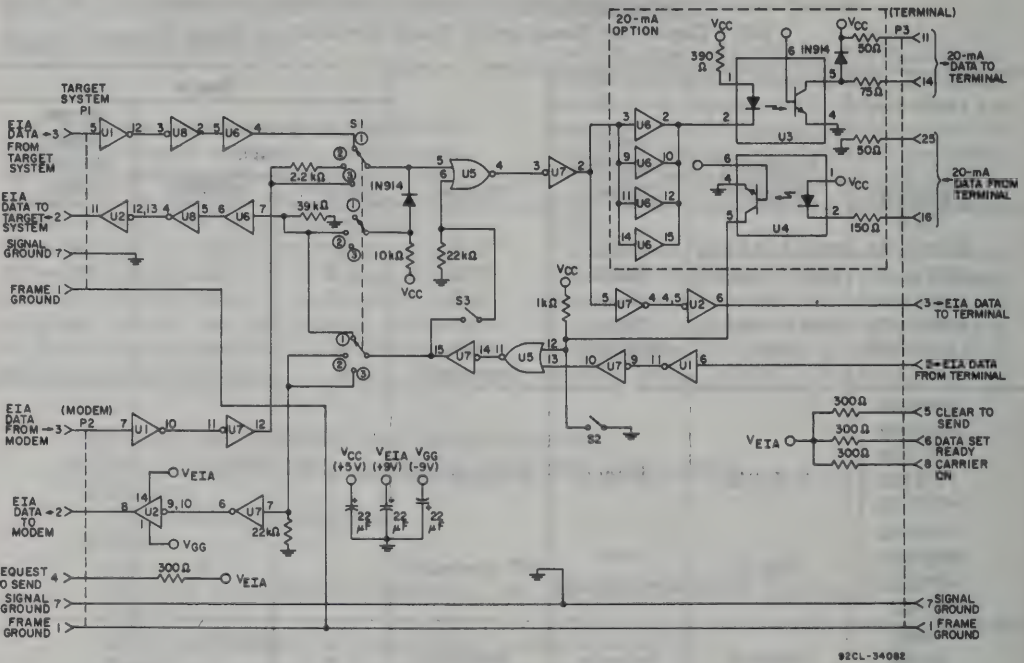
CDP18S844, CDP18S852, CDP18S853

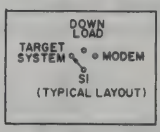
Table I - Host Systems and Distribution Media for which Ready-to-Run Micro Concurrent Pascal (mCP) Cross-Compilers are Available.

Computer	Operating System	Pascal Run-Time System	Format	Media		
				9-Track Tape		Single-Density Floppy Disk
				800BP1	1600BP1	
DEC						
PDP11/34	RSX-11/M(3.2)	OMSI	FLX	x	x	x[1]
PDP11/45	RSX-11/M(3.2)	OMSI	FLX	x	x	x[1]
PDP11/70	IAS	OMSI	FLX	x	x	x[1]
PDP11/70	RSX-11/M(3.2)	OMSI	FLX	x	x	x[1]
VAX11/780	VMS	DEC VAX	Copy Command	x	x	
Hewlett-Packard						
HP1000, HP2100, HP21MX	RTE-IVB	HP1000	ST Command	x		
HP3000, HP3000 III, HP30/33, HP44	MPE-III	HP Users Group	ST Command		x	
IBM						
3033N, 370 Series	CMS(5.0) CP(6.0)	Imperial College of London	EBCDIC	x	x	
Data General						
microNova, Nova, Eclipse, etc.	AOS, RDOS, DOS, MP/OS	Rational Data System	—	x[2]	x[2]	
Micro-computers						
Z80, 8080	CP/M(V1.4 or higher	SORCIM	—			x[3]
Z80, 8080, LS1-11, 6502, 6800, 6809, 9900	UCSD (version II.0 or higher)					x[4]

[1] Disk is RX01
[2] Requires license and purchase of RDS interpreter
[3] 8" Floppy Disk
[4] UCSD-compatible 8" Floppy Disk

CDP18S844, CDP18S852, CDP18S853



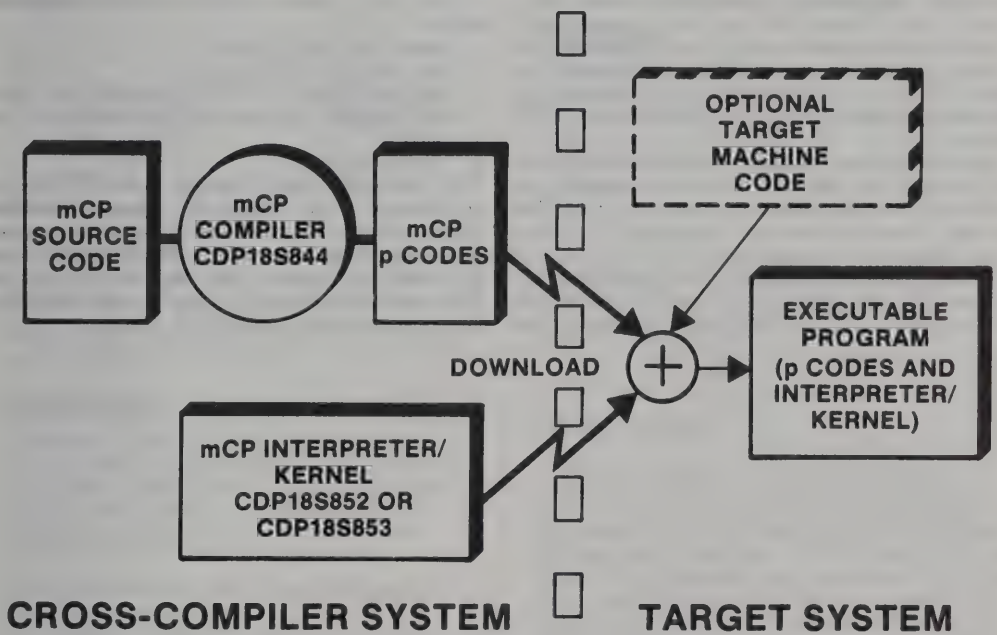


SWITCH IDENTIFICATION	
S1	① TARGET SYSTEM
	② DOWNLOAD
	③ MODEM
S2	↑ 20 mA
	↓ EIA
S3	↑ LOCAL ECHO OFF
	↓ LOCAL ECHO ON

CONNECTOR IDENTIFICATION		PLUG TYPE
P1	TARGET SYSTEM (EIA)	25-PIN CINCH (MALE)
P2	MODEM (EIA)	25-PIN CINCH (MALE)
P3	TERMINAL (EIA)	25-PIN CINCH (FEMALE)

INTEGRATED CIRCUIT	
U1	SN75154 (EIA LINE RECEIVER)
U2	SN75188 (EIA LINE DRIVER)
U3, U4	MCA230 (OPTO ISOLATOR)
U5	CD4001AE (NOR GATE)
U6	CD4050AE (BUFFER)
U7, U8	CD4049AE (INVERTER)

Fig. 2 - Download switchbox circuit.


OPTIONAL
TARGET
MACHINE
CODE
mCP
SOURCE
CODE
mCP
COMPILER
CDP18S844
mCP
p CODES
EXECUTABLE
PROGRAM
(p CODES AND
INTERPRETER/
KERNEL)
DOWNLOAD
mCP INTERPRETER/
KERNEL
CDP18S852 OR
CDP18S853
CROSS-COMPILER SYSTEM
TARGET SYSTEM

CDP18SUT60, CDP18SUT61, CDP18SUT62 Utility Firmware

The CDP18SUT60 is a Utility Program on a 2758 EPROM designed for use with a CDP18S601, CDP18S603, CDP18S606, or CDP18S608 Microboard Computer in systems such as the COSMAC Microboard Prototyping System CDP18S691. The CDP18SUT61 is a Utility Program on a 2758 EPROM designed for use with a CDP18S602, CDP18S605, CDP18S607, or CDP18S610 Microboard Computer in systems such as the COSMAC Microboard Prototyping System CDP18S692. The CDP18SUT62 is a Utility Program on a 2716 EPROM designed for use with a CDP18S601, CDP18S603, CDP18S606, or CDP18S608 Microboard Computer in systems such as the Microboard Computer Development System (MCDS) CDP18S693, or CDP18S694.

The Utility Program on the CDP18SUT60 and the CDP18SUT61 are designed to examine memory, alter memory, and begin program execution at a specified location. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions described include memory insert !M, memory display ?M, memory move $M, memory fill $F, memory substitute !S, and run program $P. The move and fill functions can also be called by user programs. Also included are read and type routines that provide communication with the user terminal by means of the UART on the Microboard Computer. Other user-callable routines that help to simplify programming include routines providing register initialization, variable delays, text output, and subroutine call and return. Some debugging capability is provided by a register save operation.

The Utility Program on the CDP18SUT62 allows the user to :

1. Inspect and modify memory.
2. Store and retrieve data on tape.
3. Start execution of the BASIC3 Interpreter, the Editor, the Assembler or a user-generated program at any address.
4. Debug programs.

The twelve commands available on the CDP18SUT62 are Memory Move, Memory Fill, Memory Substitute, Memory Display, Memory Insert, Program Run, Read Tape, Write Tape, Rewind Tape, Run BASIC, Run Editor, and Run Assembler. Also included are Read and Type routines for communications between the systems and the data terminal and for I/O transfers.

COSMAC Microprocessor Fixed-Point Binary Arithmetic Subroutines

ROM CDPR582 Paper Tape CDP18S826V1

Diskette CDP18S826 Cassette CDP18S826V2

The Binary Arithmetic Subroutine Package is a set of 16-bit 2's-complement fixed-point arithmetic subroutines designed to be operated on COSMAC CDP-1802 Microprocessor systems. The subroutines are coded in Level I assembly language and require 1 kilobyte of memory space. A detailed description of these subroutines is given in the Manual **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206A.

The subroutines are available on a floppy diskette, paper tape, cassette, and on a ROM. In source language, they are available on floppy diskette CDP18S826 for use with RCA Floppy Disk System CDP18S805, a mass memory storage unit designed to work with the CDP18S005 COSMAC Development System (CDS II). The subroutines are also available on paper tape, CDP18S826V1, and on a magnetic-tape cassette, CDP18S826V2, for a TI Silent 700 Data Terminal*. In object code, the package is available in a single 1-kilobyte ROM, CDPR582CD (4- to 6.5-volt operation) or CDPR582D (4- to 10.5-volt operation). In addition to the binary arithmetic subroutines, the ROM contains the code for the Standard Call and Return Technique. The ROM contains its own address latch and is located in memory at hexadecimal locations C000 through C3FF.

Functions

The Binary Arithmetic Subroutine Package includes 31 subroutines. Fifteen of these are binary arithmetic subroutines, fourteen are utility subroutines, and two are for format conversion. Appropriate selections from the set of subroutines may be made for the calculations required in a specific application.

Arithmetic Functions. The arithmetic functions included in this package are:

1. 16-bit 2's-complement addition
2. 16-bit 2's-complement subtraction
3. 16-bit 2's-complement multiplication yielding 32-bit products
4. 32-bit 2's-complement division yielding 16-bit quotient and remainder.

Format Conversion. In addition to the arithmetic functions, two format-conversion subroutines are included for interfacing the system to binary-coded-decimal-oriented peripheral hardware. These subroutines provide BCD-to-binary and binary-to-BCD conversions.

Utility Subroutines. A set of special utility subroutines allows the user to save and restore a group of registers on a stack or at a user-defined RAM area. These registers are used by the arithmetic function subroutines to store an operand and to point to an operand in memory. Other utility subroutines compare 16-bit operands and give indication if a register is greater than or equal to an operand.

The Standard Call and Return Technique, described in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201, is used for all the subroutines.

Timing

Timing measurements at a 6.4-MHz clock rate for the best and worst cases of the various arithmetic and format conversion subroutines for the CDP1802 are given in the tabulations at the right. These times were determined by taking an ad hoc sample of large and small numbers and performing an operation upon them. Absolute best and worst case values may vary from the values listed here.

Arithmetic Function	Best (ms)	Worst (ms)	Format Conversion	Best (ms)	Worst (ms)
Add	0.041	0.068	Binary to BCD	1.33	2.82
Subtract	0.039	0.078			
Multiply	0.851	1.29	BCD to Binary	0.094	0.81
Divide	1.37	1.78			

Literature

Further information on the Fixed-Point Binary Arithmetic subroutines, including a complete listing for all the subroutines, is given in the Manual **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206A. General information on the RCA 1800 microprocessor series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

Another arithmetic software package is described in Product Description PD7 for the COSMAC Floating-Point Arithmetic Subroutine Diskette CDP18S827. Additional information on the Floating-Point Package is given in the Manual **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207.

*Registered trademark, Texas Instruments Corporation.

CDPR582, CDP18S826, CDP18S826V1, CDP18S826V2

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AB-001

Using the A/D Microboard

The CDP18S643 Microboard is a 16 single ended or 8 differential input analog to digital conversion system with 8 or 12 bit resolution. It has a programmable gain amplifier, on board sample and hold amplifier, analog to digital converter and CMOS control logic. It has the standard two level I/O address latching and decode logic of the Microboard systems. For detailed information see MB-643.

A simple sensor system was designed to take a reading from a thermocouple connected directly to an input of the CDP18S643 A/D Microboard. The reading was scanned for limits and the Q line of the CDP1802 was set if the value was outside preset limits. A debounced momentary contact switch was connected to the flag, EF-3, to tell the system to take a sample reading and the value of the reading was finally stored in memory for later use.

The system consisted of a CDP18S601 CPU board with its on board RAM linked to be at memory location 0000; a CDP18S640 control and display board with UT60; a CDP18S676 chassis to hold the Microboards and a CDP18S659 bread board with the CD4069 and a momentary contact switch. The inverters were used to debounce the switch. A standard ASCII terminal was connected to the TTY connector on the 601 board for program loading and final data collection. An iron-constant thermocouple was connected to Channel 1, pins 1 and 17 of connector P-2, on the 643 board. Suitable power supplies for the +5 and ±15 volts were used.

Since the output of the thermocouple is on the order of millivolts, the most sensitive arrangement was used on the 643 board. The output mode was linked for single ended, straight binary, 0 to +5 volt operation. An I/O select code of 30 was used and EF1 was connected to the conversion complete signal.

The assembly language listing below shows the program to control the system. After initialization, the program loops at line 30 waiting for the momentary contact switch to be depressed. After depression and release of the switch a reading of the thermocouple is taken through the multiplexer, amplified in the PGA and held in the sample and hold amplifier for conversion by the A/D. The reading is sensed for out of range and then stored in memory. Pointers are advanced and the program loops back awaiting input.

Before taking actual measurements, the gain and offset adjustment as shown on page 6 of MB-643 were done. With this system it was possible to resolve and reproduce less than 1° Centigrade.

The concept shown here can be extended to use multiple channels of the 643 board for additional sensors by duplicating the code in the program and using either the scan mode on the board or by a software scan.

```
!M
0000 ;                  0001 ..........................................................................
0000 ;                  0002 ..  THIS PROGRAM SETS UP THE A/D MICROBOARD, INPUTS A READING
0000 ;                  0003 ..  FROM A THERMOCOUPLE, STORES IT, AND TURNS ON A LIGHT
0000 ;                  0004 ..  (THE Q LINE) IF THE VALUE IS OUT OF A GIVEN RANGE
0000 ;                  0005 ..........................................................................
0000 ;                  0006          ..DEFINE CONSTANTS
0000 ;                  0007          ..
0000 ;                  0008 BDSEL=#01
0000 ;                  0009 LSB=#02
0000 ;                  0010 MSB=#03
0000 ;                  0011 BEGIN=#05
0000 ;                  0012 RES=#06
0000 ;                  0013 CTR=#03
0000 ;                  0014 STK=#02
0000 ;                  0015 CNT=#09
0000 ;                  0016 OUTRNG=#0400
0000 ;                  0017          ..
0000 ;                  0018          ..MAIN PROGRAM
0000 ;                  0019          ..
0000 7100;              0020 DIS, #00                 ..DISABLE INTERRUPTS
0002 F800A9F80BB9;      0021 #00->CNT.0; #0B->CNT.1   ..INITIALIZE COUNT POINTER
0008 F800B3;            0022 A.1(START)->CTR.1        ..LOAD THE START ADDRESS
000B F80FA3;            0023 A.0(START)->CTR.0        ..INTO THE PROGRAM COUNTER
000E D3;                0024 SEP CTR                  ..START COUNTING IN THE COUNTER REGISTER
000F ;                  0025
000F E3;                0026 START:   SEX CTR         ..SET X FOR IMMEDIATE BYTE OUTPUT
0010 6130;              0027          OUT BDSEL ,#30  ..GROUP SELECT FOR A/D BOARD
0012 6600;              0028          OUT RES ,#00    ..SET RESOLUTION TO 12 BITS AND
0014 ;                  0029                          ..FIXED CHANNEL
0014 3614;              0030          B3 *            ..WAIT FOR SWITCH
```

AB-001

```
0016 3E16;          0031          BN3 *              ..ON FLAG LINE
0018 7A;            0032          REQ                ..TURN WARNING LIGHT OFF
0019 65E0;          0033          OUT BEGIN ,#E0     ..SET P0A AT X1024, SET CHANNEL 1, BEGIN CONVERSION
001B F80002;        0034          #0B->STK.1         ..INITIALIZE HIGH BYTE OF STACK POINTER
001E 09FEFC01;      0035          @CNT+2+1           ..PUT TWICE THE COUNT PLUS ONE INTO
0022 A2;            0036          ->STK.0            ..THE LOW BYTE OF STACK POINTER
0023 E2;            0037          SEX STK            ..SET X TO THE STACK
0024 3C24;          0038          BN1 *              ..WAIT FOR CONVERSION TO FINISH
0026 6B;            0039          INP MSB            ..INPUT THE MOST SIGNIFICANT 8 BITS FROM THE
0027 ;              0040                             ..A/D BOARD, AUTOMATICALLY PUT ON STACK
0027 606A;          0041          IRX; INP LSB       ..INCREMENT REGISTER X TO NEXT STACK LOCATION
0029 ;              0042                             ..AND PUT THE LEAST SIGNIFICANT BITS ONTO THE STACK
0029 09FC0139;      0043          @CNT+1->@CNT       ..ADD 1 TO THE VALUE OF THE COUNT IN MEMORY
002D C00100;        0044          LBR TMPCHK         ..BRANCH TO TEMPERATURE CHECK ROUTINE
0030 ;              0045
0030 ;              0046                  ..
0030 ;              0047                  ..CHECK FOR LESS THAN AMBIENT TEMPERATURE
0030 ;              0048                  ..OR OVER 125 DEG F.
0030 ;              0049                  ..
0030 ;              0050
0030 ;              0051          PAGE               ..START AT NEXT PAGE BOUNDRY
0100 22;            0052 TMPCHK:  DEC STK            ..MOVE STACK POINTER TO MSB
0101 F07E;          0053          LDX; SHLC          ..BRING MSB INTO ACCUMULATOR AND SHIFT LEFT
0103 ;              0054                             ..TO LOOK AT THE MOST SIGNIFICANT BIT
0103 CB0400;        0055          LBNF OUTRNG        ..IF IT IS 0 GO TO OUT OF RANGE ROUTINE
0106 F0FFD0;        0056          #-#D0              ..IF MSB IS GREATER THAN D0 HEX
0109 C30400;        0057          LBDF OUTRNG        ..GO TO OUT OF RANGE ROUTINE
010C C0000F;        0058          LBR START          ..GO BACK FOR ANOTHER READING
010F ;              0059
010F ;              0060                  ..
010F ;              0061                  ..OUT OF RANGE ROUTINE
010F ;              0062                  ..


010F ;              0063
010F ;              0064          ORG OUTRNG         ..START AT ADDRESS 0400
0400 7B;            0065          SEQ                ..TURN ON LIGHT
0401 C0000F;        0066          LBR START          ..GO BACK FOR ANOTHER READING
0404 ;              0067
0404 ;              0068          END                ..END OF THE PROGRAM
0000
```

AB-002
The CPU Board Line—A Comparison

Four different complete computer systems are now available on single 4.5″ × 7.5″ microboards. Each contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, an expansion interface, and sockets for user-selected read-only memory.

The characteristic features are summarized in Table 1. Note that the CDP18S601 and CDP18S603 boards are different only in the amount of on-board RAM.

The CDP18S602 board is distinguished from the others by having an on-board UART with selectable baud rates to 19.2 k baud. The CDP18S602 also offers selectable crystal-controlled clock frequencies up to 2.45 MHz which is higher than the others which have fixed clock frequency of 2 MHz. The available low clock frequencies on the CDP18S602 are useful in extreme low-power applications.

The CDP18S604 board is a low-cost computer board. It has the same parallel I/O features as the CDP18S602 board but without the UART. Serial in and out is available using the External Flag and Q line and can be driven by a software UART routine. The CDP18S604 board also has a user area for general breadboarding or a signal conditioning of the parallel I/O ports. Typically, a TTY or EIA interface can be implemented in this area.

Table 1
Microboard Computer Characteristic Features

Microboard Computer	Clock Frequency (MHz)	RAM (bytes)	ROM (bytes)	Serial I/O Port	I/O Lines	Power (V)	Power (ma)
CDP18S601	2	4K	4K (CDP1834) 4K (2708) 4K (2758) 8K (2716)	Software-driven; Q output; flag input; EIA and TTY drivers	25: 20 programmable I/O (CDP1851); 4 flag inputs, 1Q Output	+5	10
CDP18S602	Selectable: 2.4576, 1.2288, 0.6144 or 0.3072	2K	2K (CDP1834) 2K (2758) 4K (2716)	UART 15 Selectable baud rates from 50 to 19200 baud; EIA and TTY drivers	21: 8 inputs (CDP1852) 8 outputs (CDP1852), 4 flat inputs, 1Q output	+5	8
CDP18S603	2	1K	4K (CDP1834) 4K (2708) 4K (2758) 8K (2716)	Software driven; Q output; flag input; EIA and TTY drivers	25: 20 program. I/O (CDP1851); 4 flat inputs; 1Q output	+5	7
CDP18S604	2	512	512 (CDP1832) 1K (CDP1834) 1K (2758) 2K (2716)	Software driven; Q output; flag input	21: 8 inputs (CDP1852) 8 outputs (CDP1852), 4 flag inputs, 1Q output	+5	4

AB-003

Make Your CDS IV Really Rubout

The program below modifies CDOS to make a CDS IV or a CDP18S040 terminal do a real rubout of a character when the "RUBOUT" key is depressed. This program will work with CDOS 3.0 or CDOS 2.2. It can be either an overlay to CDOS which you call in after entering the operating system or you can modify the disk permanently using the DISK program. If you modify the disk, do it carefully and pay attention to the addresses.

```
!M
0000 ;                  0001
0000 ;                  0002            ..THIS PROGRAM MAKES THE 008 OR 040 RUBOUT KEY
0000 ;                  0003             .ACTUALLY DO A RUBOUT OF THE CHARATER TO THE
0000 ;                  0004            ..LEFT OF THE CURSOR
0000 ;                  0005
0000 ;                  0006 OFFSET     EQU     0
0000 ;                  0007
0000 ;                  0008
0000 ;                  0009                    ..REMOVE BEGINNING OF LINE ERASE FUNCTION
0000 ;                  0010            ORG OFFSET+0A29CH
A29C 30A6;              0011            BR 0A2A6H
A29E ;                  0012
A29E ;                  0013
A29E ;                  0014                    ..CHANGE LEFT BRACKET CALL
A29E ;                  0015            ORG OFFSET+0A31DH
A31D A389;              0016            DC 0A389H
A31F ;                  0017
A31F ;                  0018                    ..REMOVE RIGHT BRACKET
A31F ;                  0019            ORG OFFSET+0A34DH
A34D 3052;              0020            BR 0A352H
A34F ;                  0021
A34F ;                  0022
A34F ;                  0023                    ..CHANGE ERASE CHARACTER
A34F ;                  0024            ORG OFFSET+0A37EH
A37E D4A448A385;        0025            DC 0D4A4H, 48A3H, 85H
A383 3090;              0026            DC 3090H
A385 08200800;          0027            DC 0820H, 0800H         ..ERASE CHARACTER
A389 200800C4;          0028            DC 2008H, 00C4H         ..LEFT BRACKET SUBSTITUE
A38D ;                  0029
A38D ;                  0030                    ..REMOVE RIGHT BRACKET
A38D ;                  0031            ORG OFFSET+0A39EH
A39E 30A3;              0032            DC 30A3H
A3A0 ;                  0033
A3A0 ;                  0034            ORG OFFSET+0A285H
A285 A2EB;              0035            DC 0A2EBH
A287 ;                  0036
A287 ;                  0037            ORG OFFSET+0A2EBH
A2EB 0D0A2200;          0038            DC 0D0AH, 2200H
.A2EF ;                 0039
A2EF ;                  0040
A2EF ;                  0041
A2EF ;                  0042            END
0000
```

AB-004

Using the UART on the CDP18S602 CPU Board

In order to get all the I/O on the 602 board it was necessary to leave out the handshaking logic for the CDP1854 to communicate at high baud rates with other UARTs or Terminals. Specifically, there is no delayed clear to send output to tell the other sender when to send the next character. This function can however, be accomplished by using a software full duplex routine. First, initialize and clear both UARTs. This is done on the CDP1854 with the proper 2 level select, and OUT3 and 1D hex data, followed by an INP2 to read and clear the UART.

When transmitting a character, the sender does a 2 level select, then an OUT2 with the data and waits in a loop for its data available line to come true signalling receipt of an echo, this loop consists of doing a status input (INP3) a shift right and loop back to the INP3 until the DF register = 1. Finally another INP2 is done to clear the data available flag and be ready for the next character.

The receiver is selected and waits for its data available flag to come signalling a character was sent to it. The same type of status loop specified above is used (INP3, SHR, loop till DF = 1). Then an INP2 is done to get the data, remember to store it somewhere. Finally an OUT2 is done with any data as the echo.

This technique has been used with a 602 and 641 talking to each other at 19.2K baud. No problems have been experienced with programs in BASIC, PLM, and assembly language.

If you really want to get fancy on the echo, send back the just received data then the sender can check this with his originally transmitted byte for accuracy.

The following is a list of subroutines employed when using the UART on the CDP18S602 CPU board.

```
!M
0000 ;       0001                    ..THIS LISTING CONTAINS THREE SUBROUTINES WHICH
0000 ;       0002                    ..CAN BE USED AS SOFTWARE FULL DUPLEX WITH THE
0000 ;       0003                    ..CDP18S602 MICROBOARD AND ANY UART SUCH AS THE
0000 ;       0004                    ..CDP18S641 MICROBOARD.
0000 ;       0005
0000 ;       0006
0000 ;       0007          ..CONSTANTS
0000 ;       0008
0000 ;       0009 DATA     EQU     2
0000 ;       0010 STATUS   EQU     3
0000 ;       0011 UARTSEL  EQU     2
0000 ;       0012 URTWORD  EQU     1DH
0000 ;       0013 BDSEL    EQU     1
0000 ;       0014
0000 ;       0015
0000 ;       0016          ..REGISTERS
0000 ;       0017
0000 ;       0018 STK      EQU     2
0000 ;       0019 PC       EQU     3
0000 ;       0020 WORD     EQU     0FH
0000 ;       0021
0000 ;       0022
0000 ;       0023 ..*****************************************************************
0000 ;       0024 ..                                                               *
0000 ;       0025 ..                 ROUTINE TO CLEAR THE UART                     *
0000 ;       0026 ..                                                               *
0000 ;       0027 ..*****************************************************************
0000 ;       0028
0000 E3;     0029 CLEAR    SEX PC                    ..TO DO THE OUT IMMEDIATES
0001 6102;   0030          OUT BDSEL; DC UARTSEL     ..2 LEVEL SELECT THE UART BOARD
0003 631D;   0031          OUT STATUS; DC URTWORD    ..SET THE UART FOR 8 DATA BITS,
0005 ;       0032                                    ..2 STOP BITS, AND PARITY INHIBITED
0005 E2;     0033          SEX STK                   ..FOR THE INPUT
0006 6A;     0034          INP DATA                  ..CLEAR ANY DATA. REMEMBER THE DATA
0007 ;       0035                                    ..WILL GO ON THE STACK SO BE CAREFUL
0007 D5;     0036          EXIT
```

AB-004

```
0008 ;          0037
0008 ;          0038 ..*************************************************************************
0008 ;          0039 ..                                                                         *
0008 ;          0040 ..                 ROUTINE TO SEND, ASSUME WORD TO BE SENT IS IN THE       *
0008 ;          0041 ..                 HIGH HALF OF REGISTER F                                 *
0008 ;          0042 ..                                                                         *
0008 ;          0043 ..*************************************************************************
0008 ;          0044
0008 E3;        0045 SENDER   SEX PC                    ..FOR THE OUT IMMEDIATES
0009 6102;      0046          OUT BDSEL; DC UARTSEL     ..AS ABOVE
000B ;          0047
000B E2;        0048          SEX STK                   ..WE PUT THE DESIRED WORD TO BE SENT ON
000C ;          0049                                    ..THE STACK
000C 9F52;      0050          WORD.1->@STK
000E 62;        0051          OUT DATA                  ..SEND THE WORD
000F 22;        0052          DEC STK                   ..REPOSITION THE STACK POINTER
0010 ;          0053
0010 6B;        0054 LOOPS    INP STATUS                ..GET THE STATUS WORD
0011 F63B10;    0055          /2; IF NDF GOTO LOOPS     ..WAIT FOR THE 0 BIT TO BECOME A 1
0014 ;          0056                                    ..SIGNALLING DATA IS AVAILABLE
0014 ;          0057
0014 6A;        0058          INP DATA                  ..CLEAR THE DATA AVAILABLE FLAG, AGAIN
0015 ;          0059                                    ..REMEMBER THE DATA GOES ON THE STACK
0015 ;          0060
0015 D5;        0061          EXIT
0016 ;          0062
0016 ;          0063 ..*************************************************************************
0016 ;          0064 ..                                                                         *
0016 ;          0065 ..                 ROUTINE TO RECEIVE                                      *
0016 ;          0066 ..                                                                         *
0016 ;          0067 ..*************************************************************************
0016 ;          0068
0016 E3;        0069 RECVR    SEX PC                    ..AS ABOVE
0017 6102;      0070          OUT BDSEL; DC UARTSEL
0019 ;          0071
0019 E2;        0072          SEX STK
001A 6B;        0073 LOOPR    INP STATUS                ..WAIT FOR THE DATA AVAILABLE FLAG
001B F63B1A;    0074          /2; IF NDF GOTO LOOPR
001E ;          0075
001E 6A;        0076          INP DATA                  ..THIS GETS THE DATA WE WANT AND
001F ;          0077                                    ..PUTS IT ON THE STACK FOR LATER USE
001F ;          0078
001F 62;        0079          OUT DATA                  ..THIS SENDS BACK THE SAME DATA WE
0020 ;          0080                                    ..JUST RECEIVED, THE SENDER COULD DO
0020 ;          0081                                    ..A CHECK TO MAKE SURE THE TRANSMISSION
0020 ;          0082                                    ..WAS GOOD   THIS WAS NOT INCLUDED ABOVE.
0020 ;          0083
0020 22;        0084          DEC STK                   ..REPOSITION STACK POINTER
0021 ;          0085
0021 D5;        0086          EXIT
0022 ;          0087
0022 ;          0088
0000
```

AB-005
It's Easy to Talk to the VIS Microboard

The VIS Interpreter, CDP18S835, is an interpretive language developed specifically to support the CDP1869 and CDP1870/CDP1876, Video Interface System (VIS). The interpretive commands allow the user to control the VIS to provide displays of text, graphics, and motion on a cathode-ray tube in black and white or color. The interpreter is useful on any system containing the VIS chip set and is particularly supportive of the CDP18S661, RCA Microboard, Video-audio-keyboard Interface.

The interpreter has 109 instruction codes to handle just about every possible situation of putting characters, patterns or graphs on a monitor, to handle the audio output and to bring in character font information. If you can find more to do, the interpreter is open ended, allowing the user to add interpretive commands for his own special purposes. By use of the supplied source, routines that are not required for the particular application may be deleted saving memory space. The source routines may also be adapted into the user's own program and are documented to provide a guide to the programming of the VIS. The interpreter as delivered is a 3-kilobyte program and requires a minimum of 64 bytes of RAM.

The following is the object code of a program which uses the interpreter to load an ASCII character set into character memory, puts RCA in red, white and blue on a green background screen and ends with a cursor in the upper left corner ready for a character input.

Sample Program Using the VIS Interpreter CDP18S835

```
..SAMPLE PROGRAM OF THE OBJECT CODE TO DISPLAY A RED WHITE
..AND BLUE "RCA", LOAD A CHARACTER SET AND EXIT WITH A CURSOR
..IN THE UPPER LEFT READY FOR A CHARACTER INPUT

                ORG 0C00H          ..START AFTER THE INTERPRETER

        OPCODE                     ..THE MACRO OF THE OPCODE EQUATES WILL BE
                                   ..INSERTED HERE

                ..FILL CHARACTER MEMEORY

        DC OFFH                    ..START OF PROGRAM
        DC SETIO,80H,DISOFF        ..SET 2 LEVEL I/O & TURN OFF DISPLAY
        DC LOADAC,0,COLFOR         ..SET BACKROUND AND COLOR CONTROL
        DC SETFUL                  ..FULL SCREEN RESOLUTION (40 X 24)
        DC LDPMP,0F800H            ..POINT PAGE MEM POINTER AT F800 HEX ADDRESS
        DC LDMMP,CHARAC            ..POINT MAIN MEM POINTER AT CHARACTER PATTERN
        DC LDCMP,0                 ..POINT CHARACTER MEM POINTER AT 1ST LOCATION
        DC LOADVX,0,0              ..CONSTANT NEEDED FOR WRITE CHARACTER COMMAND

LOAD    DC WRTCHR,0,0              ..WRITE THE 8 ROWS OF THE CHARACTER PATTERN
                                   ..INTO THE CHARACTER MEMORY
   DO I=1,8
        DC MMPINC                  ..INCREMENT TO THE NEXT ROW
   ENDD
        DC CMPINC                  ..INCREMENT CHARACTER MEME POINTER TO NEXT
                                   ..LOCATION

        DC CMPAC,ACCLTK,81H        ..GET NEXT CHARACTER UNTIL WE DO 128 OF THEM
        DC LOAD

        DC LOADAC,20H              ..CLEAR THE SCREEN BY PUTTING THE ASCII CODE
    DO I=1,24                      ..FOR A SPACE IN EVERY PAGE MEM LOCATION
        DC FLROW1
    ENDD
```

AB-005

```
                ..DISPLAY A RED WHITE AND BLUE "RCA" ON A GREEN BACKROUND

        DC LDCMP,52H,COLORK,41H ..MAKE THE "R" RED
        DC LDCMP,41H,COLORK,81H ..MAKE THE "A" BLUE
        DC LOADAC,1,COLFOR      ..MAKE THE BACKROUND GREEN

        DC INIT,ROWINC,8        ..INITIALIZE AND GO DOWN 8 ROWS
        DC LDMMP,RCA            ..POINT AT THE PATTERN
        DC MOVEMU,240           ..PUT THE FIRST 6 ROWS INTO PAGE MEM
        DC MOVEMU,80            ..PUT IN THE LAST 2 ROWS

        DC INIT
        DC LOADAC,7FH,DISAWC    ..PUT THE CURSOR INTO THE PAGE MEM

        DC DISON                ..TURN IT ON & SEE WHAT HAPPENS

STOP    DC MEMGO,STOP           ..I'M DONE, NOW IT'S YOUR TURN


                THIS IS THE PATTERN TO DISPLAY

RCA     DC '    RRRRR    CCCC      AAA    '
        DC '    RRRRRR  CCCCCC    AAAA    '
        DC '    RR  RR  CC  CC   AA AA    '
        DC '    RR  RR  CC       AA AA    '
        DC '    RRRRR   CC       AAA AA   '
        DC '    RR RR   CC  CC  AAA  AA   '
        DC '    RR  RR  CCCCCC  AAA  AA   '
        DC '    RR   RR  CCCC   AAA  AA   '

CHARAC  CHARS                   ..THE MACRO OF THE CHARACTER SET IS INSERTED
                                ..HERE
        END
```

AB-006

Low-Power 8-Bit Combination A/D/A

The RCA COSMAC A/D-D/A converter Microboards, CDP18S644 and CDP18S654 series which contain combinations of an analog-to-digital conversion system having 8-bit resolution and/or two digital-to-analog conversion systems also with 8-bit resolution. These boards use the system +5V supply, no additional supplies are needed. They are primarily CMOS. As a result, the current requirements have been greatly minimized. The CDP18S644, 647 and 648 are bipolar versions linkable for either unipolar or bipolar operation. The CDP18S654, 657, and 658 are unipolar versions, capable of unipolar operation only. Both versions provide two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations. They are designed for use in a Microboard computer system and are plug-in compatible with the COSMAC Development Systems for hardware and software development.

Programming this board is very similar to the 12-bit boards. The following is a program which uses the CDP18S644 board in a test set application.

Features:

- Low power
- High noise immunity
- Operating temperature range -40°C to +85°C
- Operable from a single 5V supply
- Assignable I/O address
- Analog input section with:
  - — Multiplexed inputs—16 single ended or 8 differential
  - — Sample and hold circuitry
  - — A/D with 8-bit resolution
  - — Scanned or fixed channel mode
  - — Straight binary or offset binary* output code
  - — Unipolar or Bipolar* input voltage
- Analog output section with:
  - — Two independent D/A channels with 8-bit resolution
  - — Straight binary or offset binary* input code
  - — Unipolar or bipolar* output voltage

*available only on CDP18S644 board

Sample Program for the CDP18S644 A/D/A Microboard

```
!M
0000 ;                0001          ..THIS PROGRAM SHOWS THE USE OF THE CDP18S644 COMBINATION
0000 ;                0002          ..A/D/A MICROBOARD IN A SYSTEM WITH A CDP18S601 BOARD
0000 ;                0003          ..THIS IS PART OF A SYSTEM WHICH SETS UP CONDITIONS
0000 ;                0004          ..FOR A TRANSISTOR TEST SET, AND READS THE DATA
0000 ;                0005
0000 ;                0006                                ..CONSTANTS
0000 ;                0007
0000 ;                0008 BDSEL    EQU 1
0000 ;                0009 A2D2A    EQU 30H
0000 ;                0010 PIO      EQU 8
0000 ;                0011 DATA     EQU 3
0000 ;                0012 D2A1     EQU 4
0000 ;                0013 D2A2     EQU 3
0000 ;                0014 PIOBITS  EQU 2
0000 ;                0015 A2DSET   EQU 6
0000 ;                0016 A2DSTART EQU 5
0000 ;                0017
0000 ;                0018                                ..REGISTERS
0000 ;                0019
0000 ;                0020 CTR EQU 0
0000 ;                0021 STK EQU 2
0000 ;                0022
0000 ;                0023                                ..MAIN PROGRAM
0000 7100;            0024          DIS; DC 0                     ..DISABLE THE INTERRUPTS
0002 ;                0025
0002 F8FFA2;          0026          0FFH->STK.0
0005 F847B2;          0027          47H->STK.1                    ..SET STACK AREA
0008 ;                0028
```

AB-006

```
0008 ;                0029
0008 ;                0030                              ..SET UP THE VCE VOLTAGE
0008 ;                0031
0008 E0;              0032 START    SEX CTR                     ..SELECT THE A/D/A BOARD AND
0009 6130;            0033          OUT BDSEL; DC A2D2A         ..OUTPUT THE VCE VALUE TO
000B E2;              0034          SEX STK                     ..CHANNEL 2 OF THE D/A
000C 63;              0035          OUT D2A2
000D ;                0036
000D ;                0037                              ..SET UP THE IC MULTIPLIER
000D ;                0038
000D 64;              0039          OUT D2A1                    ..OUTPUT THE IC MULTIPLIER VALUE
000E ;                0040                              ..TO CHANNEL 1 OF THE D/A
000E ;                0041
000E ;                0042                              ..SET UP THE RANGE FOR IB AND IC
000E ;                0043
000E E0;              0044 ICIBRNG  SEX CTR
000F 6108;            0045          OUT BDSEL; DC PIO           ..SELECT THE PROGRAMMABLE I/O AND
0011 E2;              0046          SEX STK                     ..OUTPUT THE BIT PATTERN TO SET UP
0012 62;              0047          OUT PIOBITS                 ..THE IC AND IB RANGES
0013 2222;            0048          DEC STK; DEC STK
0015 ;                0049
0015 ;                0050                              ..WAIT FOR THE BOARDS TO SETTLE
0015 ;                0051
0015 F880FF013A17;    0052          80H; -1; IF >0 GOTO $-2
001B ;                0053
001B ;                0054                              ..READ THE A/D
001B ;                0055
001B E0;              0056 READAD   SEX CTR
001C 6130;            0057          OUT BDSEL; DC A2D2A         ..SELECT THE A/D/A BOARD AND SET THE
001E 6600;            0058          OUT A2DSET; DC 00H          ..A/D FOR FIXED CHANNEL AND
0020 6900;            0059          OUT A2DSTART; DC 00H        ..CHANNEL 0, SINGLE ENDED, AND START
0022 ;                0060                              ..CONVERSION
0022 ;                0061
0022 E2;              0062          SEX STK
0023 3C23;            0063          BN1 $                       ..WAIT FOR CONVERSION TO COMPLETE
0025 6B;              0064          INP DATA                    ..GET THE DATA
0026 FFFB;            0065          -0FBH                       ..SEE IF IT IS ABOVE 2.5 VOLTS
0028 3331;            0066          IF PZ GOTO INCIB            ..IF SO WE MUST INCREMENT TH IB
002A 12;              0067          INC STK                     ..GET RID OF THE IC RANGE
002B F0FA0373;        0068          @.AND.3->@-                 ..BITS BEFORE SENDING
002F ;                0069
002F 3008;            0070          GOTO START                  ..GO BACK FOR NEXT ONE
0031 ;                0071
0031 ;                0072                              ..INCREMENT THE IB RANGE
0031 ;                0073
0031 12;              0074 INCIB    INC STK
0032 F0FA03FB03;      0075          @.AND.03H.XOR.03H           ..IF WE WERE AT THE TOP IB RANGE
0037 323F;            0076          IF =0 GOTO OUTRNG           ..GO TO OUT OF RANGE ROUTINE
0039 ;                0077
0039 F0FC0152;        0078          @+1->@STK                   ..OTHERWISE INCREMENT THE IB RANGE
003D 300E;            0079          GOTO ICIBRNG                ..GO TRY AGAIN
003F ;                0080
003F ;                0081                              ..OUT OF IB RANGE
003F ;                0082
003F 22;              0083 OUTRNG   DEC STK
0040 F8FF52;          0084          OFFH->@STK          ..PUT FF HEX AS AN ERROR MESSAGE
0043 3045;            0085          GOTO XMITDATA       ..AND GO SEND IT
0045 ;                0086
0045 ;                0087 XMITDATA                     ..HERE THERE WOULD BE A ROUTINE TO
0045 ;                0088                              ..SEND THE MESSAGE BACK
0045 ;                0089
0045 ;                0090
0045 ;                0091          END
0000
```

AB-007
Using RAM Microboards in the Micromonitor

When using the RAM Microboards in the Micromonitor (CDP18S030) external memory socket, care must be taken to insure that Pin 3 is not connected. On the Micromonitor Pin 3 is TPB and on the RAM cards it is RUNU. Under certain conditions putting TPB on the RUNU connection will cause the memory board to be deselected. Here is a set-up list for each memory board (these are in addition to those shown in the MB's):

620	Link 2, pin A to pin B must be open (supplied open or closed depending on date of manufacture)
621 and 623	Link 2A, pin 4 to pin 13 must be cut open (supplied connected)
622	These boards do not have a link and the metal run from pin 3 must be cut. Suggest cutting the run on the bottom (solder side) of the board. About ¼ inch up from pin "C" there is a metal run which goes parallel to the length of the board for about 1½ inches between 2 plated through holes. This run can be cut to open pin 3. To reinstall, put a jumper between the two plated through holes. One of the holes comes up under U18, thus the jumper must be put on the solder side of the board. Use wire with insulation. This is on the agenda to have a link added.
625	Link 30, pin 4 to pin 5 must be open (supplied connected).

AB-008

Expanding the Capability of the Control and Display Module

Charlie Smith, FTS in Dallas suggested a circuit for modifying the Microboard Control and Display Module to Display 24 bits of data.

Most Microboard applications require data and status display. This application brief describes a modification to the CDP18S640 Microboard control and display module that allows displaying register data (16 bits) or memory data (8 bits) under programmed output control. No additional IC's are required and normal function of the -640 STEP mode is preserved.

1. To convert the MC14495P from direct to clocked display mode it is necessary to isolate pin 7 of U14 thru U19 from ground. This can be done by cutting the printed circuit between pin 7 and pin 8 of each IC. Care should be taken to prevent cutting adjacent conductors.
2. To generate the proper control signal to enable programmed output, isolate pin 8 and pin 9 of U37 (CD4001BE).
3. To preserve the address and data display during debug using the STEP Mode, add a wire from U37-4 to U37-9.
4. To enable programmed output, add a wire from U20-6 (OUT2) to U37-8.
5. Now add a wire between U37-10 and pin 7 of U14 thru U19. (See Fig. 1), to provide a clock to MC14495P.

Function

In STEP mode, switch S4 grounds U37-6 and each operation of RUN-U or RUN-P grounds U37-5 making U37-4 high. The high applied to U37-9 forces U37-10 to an unconditional low. This makes the MC14495 IC's transparent to address and data. In the non-STEP mode U37-4 is unconditionally low and U37-10 is the inverse of OUT 2 which latches address and data into the MC14495's.

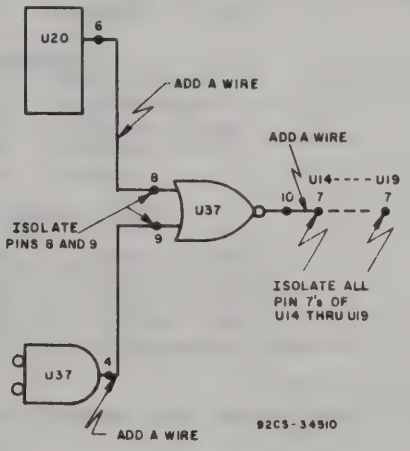

Fig. 1 - Programmed Register and Data Output for CDP18S640 Microboard Control and Display Module.

AB-009

Editor and Assembler Memory Map

Below is a memory map of the Assembler and editor for the CDP18S008 (CDS IV). A few people have asked about this and it is good general information to have.

ASM8 Version 1.0

0	2DFF	PROGRAM
2E00	34FF	BUFFERS
3500	3FFF	MACRO NAME LISTS
4000	6FFF	MACRO DEFINITION
7000	73FF	MACRO STACK
7400	7FFB	PROGRAM STACK
8000	8FFF	UTILITIES
9000	BFFF	CDOS
C000	FFFF	SYMBOL TABLE

XREF

0	16FF	PROGRAM
2000	6FFF	DATA BUFFER
7000	7FFF	STACK AREA
8000	BFFF	UTILITIES AND CDOS
C000	FFFF	SYMBOL TABLE

EDITOR Version 6.1

0	16FF	PROGRAM
1700	171F	WORK AREA
1720	BOTTOM OF STACK	BUFFER AREA
	7FFF	TOP OF STACK
8000	BFFF	UTILITIES AND CDOS

Editor Recovery

The question of recovering to the editor after accidentally depressing the RESET button on the CDP18S008 has come up a number of times. To date, there is no way known to recover since many of the registers are reinitialized on Reset. One way to lessen the chance of depressing RESET when going for the FSE key is to put a spring under the red RESET keytop. If you use this method, be EXTREMELY careful in removing the keytop, the stem underneath is breakable and replacing it is a major job.

AB-010

Memory Scan Program

The following is a program for CDOS based systems which will scan the entire 64-K byte memory area and report the areas which contain good RAM. This source code can be assembled using ASM8.

Memory Scan Program

```
          ..REGISTER DEFINITIONS
TO        EQU     0       ..TEMPORARY REGISTER
SP        EQU     2       ..STACK POINTER
PC        EQU     3       ..PROGRAM POINTER
CR        EQU     4       ..CALL REGISTER
RR        EQU     5       ..RETURN REGISTER
ARG       EQU     6       ..ARGUMENT POINTER
T1        EQU     7       ..TEMPORARY REGISTER
T2        EQU     8       ..TEMPORARY REGISTER
LIST      EQU     10      ..POINTER TO RANGES
PNT       EQU     11      ..POINTER

          ..CDOS CONSTANTS
UCALL     EQU     0B453H  ..SUBROUTINE FOR CALLING CDOS FUNCTIONS
CDENT     EQU     1EH     ..RETURN TO CDOS

          ..UTILITY ADDRESSES
TYPE      EQU     81A4H   ..RF.1->TTY
TYPE2     EQU     81AEH   ..HEX-PAIR(RF.1)->TTY
OSTRNG    EQU     83F0H   ..STRING AT @R6 -> TTY
GOUT21    EQU     83F9H   ..RETURN TO UT21
CRLF      EQU     0D0AH   ..CR/LF

                  ..PROGRAM START
          DIS; DC 0
          A.1(START)->PC.1;A.0(START)->PC.0
          A.1(STACK)->SP.1;A.0(STACK)->SP.0
          A.1(CROUT)->CR.1;A.0(CROUT)->CR.0
          A.1(RROUT)->RR.1;A.0(RROUT)->RR.0
          A.1(RANGES)->LIST.1;A.0(RANGES)->LIST.0
          SEP PC

                ..SET UP STANDARD CALL AND RETURN
          ..CALL
          SEP PC
```

AB-010

```
CROUT     ARG.1->@-"SP
          ARG.0->@-
          PC.1->ARG.1
          PC.0->ARG.0
          @ARG!->PC.1
          @ARG!->PC.0
          BR CROUT-1

          ..RETURN
          SEP PC
RROUT     ARG.1->PC.1
          ARG.0->PC.0
          SEX SP
          INC SP
          @!->ARG.0
          @->ARG.1
          BR RROUT-1

                    ..RAM AREA
          ORG ($-1)/4*4+4
RANGES    ..LIST OF GOOD AREAS
          DO [I]=1,50,1
          DC 0,0,0,0
          ENDD

          ..STACK FOR SCRT
          DO [I]=1,15,1
          DC 0,0
          ENDD
STACK     DC 0

ENDOFLIST DC 0FFH

                    ..TEST MEMORY AFTER "BEGIN" HAS BEEN TESTED
AFTER     CALL FINDBAD2,0000H
          LBDF EOMGOOD
          DEC PNT}CALL SETADDR}INC PNT

AFTER2    CALL FINDGOOD2,0000H
          LBDF RESULTS
          CALL SETADDR
          LBR AFTER

EOMGOOD   DEC PNT
          CALL SETADDR


                    ..PRINT RESULTS
RESULTS   A.1(ENDOFLIST)->PNT.1
          A.0(ENDOFLIST)->PNT.0
          LIST.0->@PNT

          ..GIVE RANGES
          A.1(RANGES)->LIST.1}A.0(RANGES)->LIST.0

GIVER     CALL OSTRNG,CRLF,'RAM AT ',0
          @LIST!->RF.1}CALL TYPE2
          @LIST!->RF.1}CALL TYPE2
          CALL OSTRNG,' - ',0
```

AB-010

```
          @LIST!->RF.1;CALL TYPE2
          @LIST!->RF.1;CALL TYPE2
          LIST.0.XOR.@"PNT;LBNZ GIVER

          CALL OSTRNG,CRLF,CRLF
          DC '                                          ENOUGH',CRLF
          DC '     PROGRAM                              MEMORY',CRLF
          DC CRLF,0

          CALL TEST,'UTILITY',0,8C00H,8C1FH,80H
          CALL TEST,'CDOS',0,9000H,0BFFH,80H
          CALL TEST,'ASM8 AND PL/M',0,0000H,7FFFH,9000H,0FFFFH,80H
          CALL TEST,'OTHER CDOS PROGRAMS',0,0000H,2FFFH,9000H,0BFFFH,80H

          LBNF GOUT21
          CALL UCALL,CDENT

                    ..RAM SEARCH ROUTINES (COPY 2)
FINDBAD2  ..DF=1 IFF WE DON'T FIND A BAD BYTE BEFORE END ADDRESS
          @PNT->@SP                         ..SAVE WHAT'S THERE
          5AH->@PNT
          @PNT.XOR.5AH;LBNZ FBERR2
          0A5H->@PNT
          @PNT.XOR.0A5H;LBNZ FBERR2
          @SP->@PNT                         ..RESTORE
          INC PNT
          PNT.1.XOR.@"ARG;LBNZ FINDBAD2
          INC ARG;PNT.0.XOR.@;DEC ARG;LBNZ FINDBAD2
          -0;LSKP
FBERR2    +0;INC ARG;INC ARG;EXIT

FINDGOOD2 @PNT->@SP
          5AH->@PNT
          @PNT.XOR.5AH;LBNZ FGERR2
          0A5H->@PNT
          @PNT.XOR.0A5H;LBNZ FGERR2
          @SP->@PNT
          INC ARG;INC ARG;+0;EXIT
FGERR2    @SP->@PNT;INC PNT
          PNT.1.XOR.@"ARG;LBNZ FINDGOOD2
          INC ARG;PNT.0.XOR.@;DEC ARG;LBNZ FINDGOOD2
          -0
          INC ARG;INC ARG;EXIT

                    ..CHECK FIRST HALF OF MEMORY
START

BEGIN     0->PNT.1,PNT.0

BEGIN2    CALL SETADDR
          CALL FINDBAD,BEGIN
          LBDF AFTER
          DEC PNT;CALL SETADDR;INC PNT
          CALL FINDGOOD,BEGIN
          LBNF BEGIN2
          LBR AFTER2

                    ..SUBROUTINES
```

AB-010

```
SETADDR   PNT.1->@LIST;INC LIST
          PNT.0->@LIST;INC LIST
          EXIT

FINDBAD   ..DF=1 IFF WE DON'T FIND A BAD BYTE BEFORE END ADDRESS
          @PNT->@SP                       ..SAVE WHAT'S THERE
          5AH->@PNT
          @PNT.XOR.5AH;LBNZ FBERR
          0A5H->@PNT
          @PNT.XOR.0A5H;LBNZ FBERR
          @SP->@PNT                       ..RESTORE
          INC PNT
          PNT.1.XOR.@"ARG;LBNZ FINDBAD
          INC ARG;PNT.0.XOR.@;DEC ARG;LBNZ FINDBAD
          -0;LSKP
FBERR     +0;INC ARG;INC ARG;EXIT

FINDGOOD  @PNT->@SP
          5AH->@PNT
          @PNT.XOR.5AH;LBNZ FGERR
          0A5H->@PNT
          @PNT.XOR.0A5H;LBNZ FGERR
          @SP->@PNT
          INC ARG;INC ARG;+0;EXIT
FGERR     @SP->@PNT;INC PNT
          PNT.1.XOR.@"ARG;LBNZ FINDGOOD
          INC ARG;PNT.0.XOR.@;DEC ARG;LBNZ FINDGOOD
          -0
          INC ARG;INC ARG;EXIT
                    ..RANGE TEST SUBROUTINES
LIMITS    ..CHECK LIMITS IN T1 AND T2

          A.1(RANGES)->LIST.1;A.0(RANGES)->LIST.0

LIMITS2   INC LIST
          T1.1-@"LIST                     ..CHECK LOWER BOUNDRY
          DEC LIST
          T1.1-"@
          INC LIST;INC LIST
          LBNF LIMITS3                    ..BRANCH IF T1<@LIST

          INC LIST
          T2.0-+@
          DEC LIST
          T2.1-+"@
          LBNF LIMITS3
          -0;EXIT

LIMITS3   INC LIST;INC LIST
          LIST.0.XOR.@"PNT;LBNZ LIMITS2
          +0;EXIT

TEST      ..TEST A GROUP OF MEMORY CHUNKS AND ISSUE REPORT
          0->T0.0
TEST2     @ARG!->RF.1;LBZ TABIT
          INC T0
          CALL TYPE;LBR TEST2

          ..MOVE OVER TO COLUMN
```

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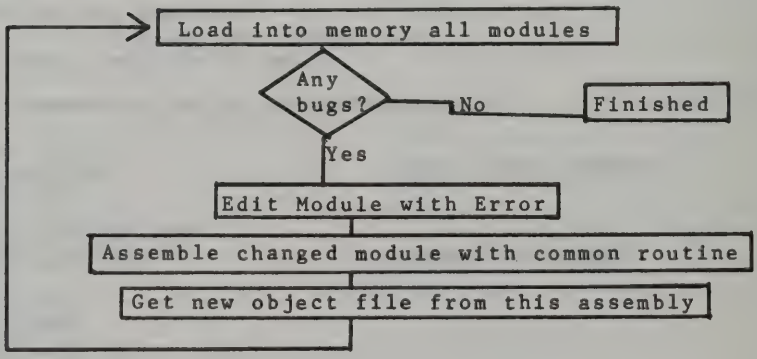
```
TABIT     T0.0.XOR.41;LBZ TEST3
          INC T0;CALL OSTRNG,' ',0
          LBR TABIT

TEST3     @ARG!->T1.1
           .XOR.80H;LBZ TESTGOOD
          @ARG!->T1.0
          @ARG!->T2.1
          @ARG!->T2.0
          CALL LIMITS
          LBDF TEST3

TEST4     ..RUN OUT TO END OF CALL SEQUENCE
          @ARG!.XOR.80H;LBZ TEST5
          INC ARG;INC ARG;INC ARG;LBR TEST4

TEST5
          ..BAD
          CALL OSTRNG,'NO',CRLF,0
          +0;EXIT
TESTGOOD  CALL OSTRNG,'YES',CRLF,0
          -0;EXIT

          END 0000H
```

AB-011

Modular Software Development Techniques for the CDP1802

I. Using the 008 Development System, CDSIV, to develop an application in a modular manner with separate assemblies:
   1. Define application
   2. Decide on modules required for the task
   3. Define input and output for the modules
   4. Decide on approximate size of the modules
   5. Determine memory address for the program space and variable space
   6. Decide on the number of common equate values
   7. Decide on the number of common variables and their usage
   8. Design a common routine defining:
      a. Global equate values
      b. Global variables RAM locations
      c. Origin for modules in memory
      d. Execution address for modules in memory
   9. Design the main control module for the application
   10. Design each sub-module
   11. Code the common routine, the main control module and each sub-module.
   12. The assembly process is as follows:
      a. Assemble the common routine
      b. Using the build mode, assemble a module
      c. The resulting object code is the object code for the module
   13. The debugging procedure follows:



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14. Sample coding of example with system:
    a. common routine
    b. Main control module — size = 100H
       Relative Start Address = 5H
    c. 2 sub modules
       #1 — Size = 300H
       Relative Start Address = 1DH
       #2 — Size = 400H
       Relative Start Address = 7H

```
..    Common Routine
..
..    Common Equate Values
CEV1        EQU   1
CEV2        EQU   2
CEV3        EQU   3
..    Common Variables
                  ORG   F000H                 ..Ram area at F000
CV1               DS    1
CVZ               DS    10
CV3               DS    5
..    Rom or Program Area
                  ORG   3000H
  MAINORG         DS    100H                  ..Origin of main routine
MINORIORG         DS    300H                  ..Origin of minor area 1
MINOR2ORG         DS    400H                  ..Origin of minor area 2
  RELMAIN         EQU   0CH                   ..Relative start address of Main
RELMINOR    1     EQU   10H                   ..Relative start address of
                                                  Minor 1
ELMINOR     2     EQU   7H                    ..Relative start address of
                                                  Minor 2
STARTMAIN         EQU   MAINORG+RELMAIN       ..Absolute start address of Main
STARTMINOR 1      EQU   MINORIORG+RELMINORI   ..Absolute start address of
                                                  Minor 1
STARTMINOR 2      EQO   MINORZORG+RELMINORZ   ..Absolute start address of
                                                  Minor 2
..
..    Code for Main Process
..
      ORG         MAINORG
      DS          5
      A.1 (STARTMAIN) R3.1
      A.0 (STARTMAIN) R2.0
      SEP   R3
      CALL  STARTMINOR1
      CALL  STARTMINOR2
      LBR   STARTMAIN
      END
..    CODE for MINDR1 Process
..
      ORG   MINORIORG
      DS    10H
      CALL  STARTMINDR2
      EXIT
      END
..    CODE for MINOR2 Process
..
      ORG   MINOR2ORG
      DS    7H
      EXIT
      END
```

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15. CDOS Commands to reassemble one changed module:
    Assume common routines file name is common
    Assume module's name to reassemble is
    >MINOR2
    >ASM8 COMMON
    >ASM8 MINOR2;B
    The object file contains only code for the assembled file in the correct memory address and with the external references resolved.
16. Sample listings of similar applications described in this section.

```
FILE: COMMON LST      DISK: SIMPLE LINKER 1

'M
0000 ;     0001 ;
0000 ;     0002 ;COMMON ROUTINE
0000 ;     0003 ;
0000 ;     0004 CEV1     EQU     1
0000 ;     0005 CEV2     EQU     2
0000 ;     0006 CEV3     EQU     3
0000 ;     0007 ;COMMON VARIABLES
0000 ;     0008          ORG     0F000H    ;RAM AREA AT F000
F000 ;     0009 CV1      DS      1
F001 ;     0010 CV2      DS      10
F00B ;     0011 CV3      DS      5
F010 ;     0012 ;ROM OR PROGRAM AREA
F010 ;     0013          ORG     3000H
3000 ;     0014 MAINORG  DS      100H      ;ORIGIN OF MAIN ROUTINE
3100 ;     0015 MINOR1ORG DS     300H      ;ORIGIN OF MINOR AREA 1
3400 ;     0016 MINOR2ORG DS     400H      ;ORIGIN OF MINOR AREA 2
3800 ;     0017 RELMAIN  EQU     0CH       ;RELATIVE START ADDRESS OF MAI
3800 ;     0018 RELMINOR1 EQU    10H       ;RELATIVE START ADR OF MINOR1
3800 ;     0019 RELMINOR2 EQU    7H        ;RELATIVE START ADR OF MINOR2
3800 ;     0020 STARTMAIN EQU    MAINORG+RELMAIN ;ABS START ADR OF MAIN
3800 ;     0021 STARTMIN1 EQU    MINOR1ORG+RELMINOR1 ;ABS START ADR OF MINOR1
3800 ;     0022 STARTMIN2 EQU    MINOR2ORG+RELMINOR2 ;ABS START ADR OF MINOR2
3800 ;     0023          END
0000

FILE: COMMON.XRF      DISK: SIMPLE LINKER 1

C R O S S   R E F E R E N C E   L I S T I N G

SYMBOL          ADDR    DEF     REFERENCES

CEV1            0001    0004
CEV2            0002    0005
CEV3            0003    0006
CV1             F000    0009
CV2             F001    0010
CV3             F00B    0011
MAINORG         3000    0014    0020
MINOR1ORG       3100    0015    0021
MINOR2ORG       3400    0016    0022
RELMAIN         000C    0017    0020
RELMINOR1       0010    0018    0021
RELMINOR2       0007    0019    0022
STARTMAIN       300C    0020
STARTMIN1       3110    0021
STARTMIN2       3407    0022
```

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```
FILE: MAIN.LST          DISK: SIMPLE LINKER 1

!M
0000 ;                  0001 ..
0000 ;                  0002 ..CODE FOR MAIN PROCESS
0000 ;                  0003 ..
0000 ;                  0004            ORG     MAINORG
3000 ;                  0005            DS      5
3005 F830B3;            0006            A.1(STARTMAIN)->R3.1
3008 F800A3;            0007            A.0(STARTMAIN)->R3.0
300B D3;                0008            SEP     R3
300C F8F0B8;            0009            A.1(CV1)->R8.1
300F F800A8;            0010            A.0(CV1)->R8.0
3012 D43110;            0011            CALL    STARTMIN1
3015 D43407;            0012            CALL    STARTMIN2
3018 C0300C;            0013            LBR     STARTMAIN
301B ;                  0014            END
0000


FILE: M1.L              DISK: PLM APPLICATION 1

!M
0000 ;                  0001 ..
0000 ;                  0002 ..CODE FOR MINOR1 PROCESS
0000 ;                  0003 ..
0000 ;                  0004            ORG     MINOR1ORG
3100 ;                  0005            DS      10H
3110 F800B8;            0006            A.1(CEV1)->R8.1
3113 F801A8;            0007            A.0(CEV1)->R8.0
3116 D43407;            0008            CALL    STARTMIN2
3119 D5;                0009            EXIT
311A ;                  0010            END
0000

FILE: M2.L              DISK: PLM APPLICATION 1

!M
0000 ;                  0001 ..
0000 ;                  0002 ..CODE FOR MINOR2 PROCESS
0000 ;                  0003 ..
0000 ;                  0004            ORG     MINOR2ORG
3400 ;                  0005            DS      7H
3407 D5;                0006            EXIT
3408 ;                  0007            END
0000
```

AB-011

II. Combining PLM applications with a generalized library Situation:

Resident is some debugged library which is originated at 6000H. A sample library follows:

```
FILE: PLMAPP.S6          DISK: PLM APPLICATION II

DO;
$A ORG 6000H
ROUT1: PROCEDURE (X,Y);
DECLARE (X,Y) ADDRESS;
        X=Y;
        X=Y;
        X=Y;
END ROUT1;
ROUT2: PROCEDURE (X2,Y2);
DECLARE (X2,Y2) ADDRESS;
        X2=Y2;
        X2=Y2;
        X2=Y2;
END ROUT2;
ROUT3: PROCEDURE (X3,Y3);
DECLARE (X3,Y3) ADDRESS;
        X3=Y3;
        X3=Y3;
        X3=Y3;
END ROUT3;
        $A LBR 60D0H
        $A ORG 0F000H
END;
EOF
```

After this library has been compiled, ascertain the starting address of the procedures ROUT1, ROUT2 and ROUT3.

Assume the users PLM program calls some of the library routines. Then their program would look as follows:

```
FILE: PLMMIA.N6          DISK: PLM APPLICATION II

DO;
DECLARE A BYTE;
DECLARE A1 BYTE;
DECLARE A2 BYTE;
        $A LBR 6000H
        $A ORG 6000H
ROUT1: PROCEDURE (X,Y);
DECLARE (X,Y) ADDRESS;
END ROUT1;
        $A LBR 6040H
        $A ORG 6040H
ROUT2: PROCEDURE (X2,Y2);
DECLARE (X2,Y2) ADDRESS;
END ROUT2;
        $A LBR 6080H
        $A ORG 6080H
```

```
ROUT3: PROCEDURE (X3,Y3);
DECLARE (X3,Y3) ADDRESS;
END ROUT3;
        $A LBR 60D0H
        $A ORG 60D0H
USER$PROCEDURE: PROCEDURE (A10,A11);
DECLARE (A10,A11) ADDRESS;
        A10=A11;
END USER$PROCEDURE;
/*   MAIN LOOP */
        DO WHILE A1 = A1;
        END;
END;
EOF
```

Once both programs are compiled the debugging step begins. Using the CDOS loader, first load in the user PLM object file. Then load in the library codes and begin debugging.

III. Linking Basic and Assembly Language Programs

Basic 1, 2 and 3 have two commands which allow the user to enter assembly language programs: CALL and USR in Basic 2 and 3 and GOSUB @ and USR in Basic 1

Basic 1 GOSUB @ EXPR1 [,EXPR2] [,EXPR3]
Basic 2 and 3 CALL EXPR1 [,EXPR2] [,EXPR3]

This statement provides the link between Basic and machine language programming. It serves as a machine language subroutine call. It transfers execution to a machine language subroutine, the address of which is determined by $expr_1$. The machine language routine should be written with the following rules in mind.

1. The program counter upon entry into the subroutine is R3.
2. Transfer is made back to Basic by means of a D5 (SEP R5) instruction.
3. Basic allows the machine language routines free use of R8, RA, RC, RD, and RE (if standard utility programs are used they require RC, RD and RE). If any other registers are to be used, they should be saved first on the stack and restored before returning to Basic.
4. Use of W and EF4 should be avoided. These signals are used for terminal I/O channels.
5. SCRT conventions have been established by Basic and no further initialization is required by the machine language subroutines to make use of SCRT. Basic 1 also preserves D and Clobbers RE.
6. The stack is available for use (pointed to by R2) so long as it returns as it was left.

For Basic 2 and 3 any of the expression ($expr_1$, $expr_2$, $expr_3$) may be expressed in either integer or floating point. Basic 2 and 3 will automatically convert them to integer. The value of $expr_2$, if used, is then passed to the machine language subroutine as a 16-bit binary integer number in R8. A second piece of data may also be passed to the machine language subroutine in register RA. The value will be that of $expr_3$.

USR ($expr_1$,)
USR ($expr_1$, $expr_2$,)
USR ($expr_1$, $expr_2$, $expr_3$)

This function acts like the CALL statement described in the previous section but with the difference that USR is a function to be used as part of an expression. When USR is encountered, a subroutine call is made to the machine language routine stored at $expr_1$. Data may be passed to the subroutine in exactly the same way as the CALL or GOSUB @ statement. With the USR function, when a D5 is encountered in the machine language routine, Basic 2 and 3 will return a 32-bit binary integer number as a value for the USR function. This 32-bit number will be constructed from R8 and RA. R8 provides the low-order 16 bits and RA provides the high-order 16 bits. In Basic 1, a 16-bit integer number is returned with the high 8 bits in RA 1 and the low 8 in D. An example follows:

PR 2*USR(@3C1E,#2F)+A/D

Example of using Basic 3 with the CDP18S661 VIS board. We assume the VIS board has the standard ASCII character set in character memory.

This is the basic program:

```
10 REM CLEAR THE SCREEN
20 CALL (@9080)
30 REM PUT THE ASCII VALUE OF THE
40 REM KEY WHICH IS DEPRESSED INTO
50 REM VARIABLE A AND DISPLAY THE
   CHARACTER
```

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```
 60 A = USR (@9100)
 70 REM DISPLAY THE CHARACTER "C" AT
 80 REM LOCATION F906 HEX
 90 CALL (@90C0, @F906, #43)
100 END
```

Another technique which may be used to link machine language routines with any of the three versions of Basic involve using Entry and Exit routines. In this approach, the USR or Basic call always transfers Control to the Entry routine address regardless of which routine is to be executed. The Entry routine saves all registers to the stack that are required by the machine language routine and yet must be maintained for Basic.

```
9045 ;          0146 ..*****************************************************
9045 ;          0147                    ..CLEAR SCREEN AND HOME CURSOR
9045 ;          0148 ..*****************************************************
9045 ;          0149
9045 ;          0150          ORG PGRM+80H
9080 ;          0151
9080 ;          0152 CLRSCN   VISON
9080 E3;        0152            SEX CTR
9081 6180;      0152            OUT BDSEL; DC VISBD
9083 E2;        0152            SEX STK
9084 ;          0153
9084 ;          0154          LAR HOME,PPTR         ..INITIALIZE THE PAGE POINTER
9084 F800A8;    0154            A.0(HOME)->PPTR.0
9087 F8F2B8;    0154            A.1(HOME)->PPTR.1
908A ;          0155
908A 348A;      0156 CLRSCN1  IF EF1 GOTO $         ..WAIT FOR NON-DISPLAY
908C F8205818;  0157          20H->@PPTR; INC PPTR..LOAD UP WITH SPACES
9090 98;        0158          PPTR.1
9091 3A8A;      0159          IF >0 GOTO CLRSCN1
9093 ;          0160
9093 ;          0161          LAR HOME,PPTR         ..HOME THE CURSOR
9093 F800A8;    0161            A.0(HOME)->PPTR.0
9096 F8F2B8;    0161            A.1(HOME)->PPTR.1
9099 ;          0162
9099 ;          0163          BASICON
9099 E3;        0163            SEX CTR
909A 6101;      0163            OUT BDSEL; DC BASICBD
909C E2D5;      0163            SEX STK; EXIT
909E ;          0164
909E ;          0165
909E ;          0166 ..*****************************************************
909E ;          0167             ..THIS TAKES A CALL FROM BASIC AND DISPLAYS
909E ;          0168             ..THE CHARACTER WHOSE ASCII VALUE IS EXPR #3
909E ;          0169             ..INTO THE LOCATION OF EXPRESSION #2
909E ;          0170 ..*****************************************************
909E ;          0171
909E ;          0172          ORG PGRM+0C0H
90C0 ;          0173
90C0 ;          0174          VISON
90C0 E3;        0174            SEX CTR
90C1 6180;      0174            OUT BDSEL; DC VISBD
90C3 E2;        0174            SEX STK
90C4 ;          0175
90C4 8A         0176          CHARPTR.0           ..GET THE CHARACTER, WAIT FOR
90C5 3AC5       0177          IF EF1 GOTO $       ..NON-DISPLAY
90C7 52         0178          ->@PPTR             ..AND SHOVE IT IN
90C8 ;          0179
```

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```
90C8 ;          0180          BASICON
90C8 E3;        0180            SEX CTR
90C9 6101;      0180            OUT BDSEL; DC BASICBD
90CB E2D5;      0180            SEX STK; EXIT
90CD ;          0181
90D1 ;          0193 ..*****************************************************
90D1 ;          0194        ..ROUTINE TO INPUT A CHARACTER FROM THE KEYBOARD
90D1 ;          0195        ..AND DISPLAY IT
90D1 ;          0196 ..*****************************************************
90D1 ;          0197
90D1 ;          0198     ORG PGRM+100H
9100 ;          0199
9100 ;          0200     VISON
9100 E3;        0200       SEX CTR
9101 6180;      0200       OUT BDSEL; DC VISBD
9103 E2;        0200       SEX STK
9104 ;          0201
9104 3D04;      0202     IF NEF2 GOTO $   ..WAIT FOR A KEY DEPRESSION
9106 ;          0203
9106 6B;        0204     INP CHARIN       ..GET THE CHARACTER
9107 ;          0205
9107 F980;      0206      OR.80H          ..MAKE THE PAGE COLOR BIT A "1"
9109 ;          0207
9109 3409;      0208     IF EF1 GOTO $    ..WAIT FOR NON-DISPLAY
910B 58;        0209     ->@PPTR          ..DISPLAY IT AT THE ADDRESS GIVEN
910C ;          0210                      ..IN THE BASIC "USR" INSTRUCTION
910C ;          0211
910C FA7F;      0212      AND.7FH         ..STRIP OFF THE PAGE COLOR BIT
910E A8;        0213     ->PPTR.0         ..PUT THE NUMBER INTO REG 8 FOR BASIC
910F ;          0214
910F ;          0215     LAR 0,RA         ..BASIC WANTS THIS
910F F800AA;    0215       A.0(0)->RA.0
9112 F800BA;    0215       A.1(0)->RA.1
9115 B8;        0216     ->PPTR.1
9116 ;          0217
9116 ;          0218     BASICON
9116 E3;        0218       SEX CTR
9117 6101;      0218       OUT BDSEL; DC BASICBD
9119 E2D5;      0218       SEX STK; EXIT
911B ;          0219
911B ;          0220
```

It then accepts the second expression as a number indicating the routine to be executed. This number is used to select the proper address from a table and transfer control to the routine. The Exit routine restores the register and returns control to Basic.

One advantage of this approach is that the Basic program only requires one fixed address, that of the Entry routine. Thus, the machine language routines may be relocated without affecting the Basic program. Only the table of addresses within the Entry routine must be updated. The approach also allows for usage of more registers by the machine language routines than those normally allowed. The only disadvantage is that the second expression of the Basic call is dedicated to containing the number of the routines to be executed and may not be used to past parameters.

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An example of the Entry and Exit follows:

```
Entry:          GHI    REG                 Store any register on
                STXD                        stack which is used by
                GLO REG                     Basic but are required
                STXD                        by the machine language
                                             Routine.

                GHI R6                      Store return address on
                STXD                        stack
                GLO R6
                STXD
                GLO R8
                SHL                         Add number of machine lan-
                ADI A.0(Address Table)      guage routine to the
                PLO R6                      address of table to find
                LDI  0                      routine address and put
                ADCI A,1 (Address Table)    result in R6.
                PHI R6                      Execute a return.
                SEP R5

                                            Machine Language Branches
                                              to Exit when done.

Exit:           INC   R2
                LDA   R2                    Restore Register
                PLD   REG
                LDA   RZ
                PHI   REG
                    .
                    .
                    .
                    .
                LDN   REG
                PHEREG
                SEP   RS                    Return to Basic

Address
 Table          A(Machine Lang. Routine 0)
                A(Machine Lang. Routine 1)
```

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Conserving Paper

When copying to the line printer or using the PRINT program, there are two form feeds done on initialization. This can easily be changed by modifying CDOS either in RAM temporarily or permanently on disk. To change RAM, load CDOS then reset to run the utility and use the !M command to change memory locations starting at 930E to CO9314 for 1 form feed or CO931A for no form feeds. To change the diskette permanently use the DISK program. The bytes to be changed are on Track 1, sector 15, locations 67 through 6C on the supplied CDOS 3.0 diskette. Use the modify in ASCII routine to change the data to CO9314 for 1 form feed or CO931A for none.

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Change to CDP18S480 PROM Programmer Board

If a short pulse occurs on the programming line on the CDP18U42 when the program power switch is turned on, the first memory location gets programmed with whatever happens to be on the data bus. To eliminate this problem, add a jumper on the 4 pole double throw switch on the board. The jumper goes on switch #2 on the solder side of the board. With the edge connector down and the solder side towards you, the switch is in the upper left. Solder the jumper between the third pin from the left on the middle row to the third pin from the left on the bottom row. This will not adversely affect other proms.

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Note on Utility Programs

When using the utility programs UT4 (CDP18S020 Evaluation kit) and UT60 (CDP18S691 Prototyping kit) please note that Register D, low byte, is clobbered by the TYPE Routines. This is not mentioned in the tables of the manuals, but it is in the included source listings of the utility programs.

Application Note Abstracts

ICAN-6416 ..... 8 pages
An Introduction to Microprocessors and the RCA COSMAC COS/MOS Microprocessor
This Note is an introduction to the fundamentals of microprocessors and to the specific capabilities of the RCA COSMAC microprocessor.

ICAN-6842 ..... 6 pages
16-Bit Operations in the CDP1802 Microprocessor
Although the CDP1802 microprocessor is an 8-bit machine, it contains mostly 16-bit registers. Its sixteen 16-bit registers are all general-purpose types, giving the CDP1802 a great deal of flexibility and the flavor of a 16-bit microprocessor in many respects. This Note describes various software routines and a few interface circuits that can be used to manipulate full 16-bit values in the CDP1802.

ICAN-6847 ..... 4 pages
Programming 2732 PROM's with the CDP18S480 PROM Programmer
The CDP18S480 PROM Programmer was designed to program a variety of industry-standard PROM's, including the Intel 2704, 2708, 2758, and 2716's and equivalent products from other suppliers. With a simple hardware addition to the PROM Programmer, and without any software changes, the CDP18S480 can also be used to program Intel 2732 PROM's. This Note describes the technique used for 2732 programming.

ICAN-6889 ..... 4 pages
Using Slower Memories with the VIS Display System
The VIS (Video Interface System) Display System (CDP1869 and CDP1870), a minimal-device-count approach to color-character generation, is essentially a CRT controller designed to interface to the CDP1800 series of microprocessors (CDP1802, CDP1804). The scheme described in this Note, while requiring a few more parts, very nearly doubles the memory access-time requirement of the system, and permits the use of memories approximately half as fast as those normally required with the VIS System.

ICAN-6918 ..... 4 pages
A Methodology for Programming COSMAC 1802 Applications Using Higher-Level Languages
This Note defines a method of optimizing the time-critical portions of programs written in higher-level languages for COSMAC 1802 applications by recoding those portions in assembly language.

ICAN-6925 ..... 8 pages
Understanding and Using the CDP18U42 EPROM
This Note describes the design and programming characteristics of the RCA CDP18U42 nonvolatile ultraviolet-erasable/programmable read-only memory.

ICAN-6928 ..... 6 pages
Interfacing PLM Code to CDOS System Functions
This Application Note defines a method for interfacing PLM programs to CDOS system functions without the need for assembly language; the interface is an array of PLM procedures (which can be included in a PLM library) and supportive macro definitions, all of which are described in detail and used in a sample program.

ICAN-6934 ..... 4 pages
Cassette Tape I/O For COSMAC Microprocessor Systems
This Note describes a circuit and the software needed to add a low-cost cassette-tape input and output to the COSMAC Evaluation Kit (CDP18S020, CDP18S024, and CDP18S025), the COSMAC Development System (CDP18S005 and CDP18S007), or the Microboard Prototyping Kit (CDP18S691).

ICAN-6943 ..... 28 pages
Designing Minimum/Nonvolatile Memory Systems with CMOS Static RAM's
This Note details the system considerations and circuit requirements for CDP1800-series RAM operation and data retention in CDP1802-based systems. Included are details relating to interfacing complexity as a function of memory-array size, power-distribution considerations, power-down/power-up control, and battery selections.

ICAN-6948 ..... 2 pages
Parallel Clocking of Sequential CMOS Devices
It is a well-established fact that process variations lead to different input MOS-transistor thresholds, and that these differences directly affect the clock input trigger voltage of sequential CMOS logic circuits. This Note describes the solution to this logic-error condition.

ICAN-6953 ..... 12 pages
An Introduction to the Video Interface System (VIS) Devices - CDP1869 and CDP1870
This Note describes a circuit and the software required to mate the RCA-CDP1869 and CDP1870 VIS (Video Interface System) chip set to the Evaluation Kit, CDP18S020. The capabilities of the VIS chip set are demonstrated by employing the set in the video portion of an intelligent terminal. Also included in the Note is the circuitry for a CPU controller which, combined with the video board, permits implementation of a stand-alone video output from serial ASCII input.

ICAN-6955 ..... 6 pages
Using the COSMAC Microboard Battery-Backup RAM, CDP-18S622
The RCA-CDP18S622, COSMAC Microboard 8-Kilobyte Battery-Backup RAM is a Microboard RAM card equipped with rechargeable batteries. This Note discusses the application of the board as a standard-power backup medium, a nonvolatile transport medium, and as an efficient means of aiding the testing of new or prototype boards.

ICAN-6970 ..... 12 pages
Understanding and Using The CDP1855 Multiply/Divide Unit
This Note tells how the CDP1855 Multiply/Divide Unit, MDU, can be an efficient hardware replacement for the software-only implementation of arithmetic and signal-processing algorithms.

ICAN-7029 ..... 6 pages
Low-Power Techniques for use with CMOS CDP1800-Based Systems
RCA CDP1800-series memory and microprocessor products employ static memory cells in all data-storage registers with the result that the products are fully functional from dc to their maximum rated frequencies. It is the static capability of the CDP1800-series products that gives them an advantage when low power consumption is imperative. This Note describes various techniques for reducing the power requirements of microcomputer systems since battery life is so important in most portable applications and in systems having a RAM battery back-up provision.

ICAN-7032 ..... 36 pages
CDP1800-Based Video Terminal Using the RCA Video Interface System, VIS
An important advantage of the VIS is its ability to operate independently of the CPU, and to provide all of the synchronization signals and refresh data for a standard NTSC (U.S.) or PAL (European) raster-scan display, while also supplying a clock input to the CPU. The result is a CPU free to handle other tasks, such as monitoring a keyboard, a primary requirement of the operating system used in the application discussed in this Note.

Technical Manuals

User Manual for the RCA-CDP1802 COSMAC Microprocessor—Describes the microprocessor architecture, provides easy-to-use programming instructions, and illustrates practical methods of adding external memory and control circuits. Gives examples of instructions and programming techniques.
MPM-201C (8-3/8" x 10-7/8", 120 pages)

Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors—Provides 31 subroutines designed to be operated on RCA COSMAC Microprocessors: 15 for 16-bit 2's-complement arithmetic, 14 for utility, and 2 for format conversion.
MPM-206A (8-3/8" x 10-7/8", 48 pages)

Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors—Describes 18 subroutines and gives detailed information on their application. Ten are 32-bit floating-point arithmetic subroutines, 6 are for utility, and 2 are for format conversion.
MPM-207 (8-3/8" x 10-7/8", 32 pages)

Instruction Manual for RCA COSMAC Microterminal—Explains the installation and application of a portable hand-held data terminal for microcomputer systems using the CDP1802 microprocessor. Describes available programs and operating modes and sequences.
MPM-212 (8-3/8" x 10-7/8", 28 pages)

Operator Manual for the RCA COSMAC Development System II CDP18S005—Guide for the user of RCA CDS II, a prototyping design aid for hardware and software systems based on the CDP1802 microprocessor. Describes the hardware modules and explains the functions available from software.
MPM-216A (8-3/8" x 10-7/8", 128 pages)

RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual—Describes the floppy-disk mass-memory storage unit for use with the CDS II CDP18S005 for rapid program development. Covers hardware interfacing, software for program loading, and Resident Editor, Assembler, and Utility programs.
MPM-217A (8-3/8" x 10-7/8", 112 pages)

Instruction Manual for the RCA COSMAC Micromonitor CDP18S030—Provides operation, installation, and application information on the COSMAC Micromonitor CDP18S030, which enables real-time in-circuit debugging of any CDP1802 microprocessor hardware and software system.
MPM-218B (8-3/8" x 10-7/8", 52 pages)

Operator's Manual for PROM Programmer CDP18S480—Describes use of hardware and software package CDP18S480 for facilitating user programming of RCA and other industry-standard PROM's. Used with COSMAC Development Systems CDP18S005 and CDP18S007 and with Microboard computer systems.
MPM-222A (8-3/8" x 10-7/8", 30 pages)

Instruction Guide for the COSMAC Macro Assembler (CMAC)—Describes use of Macro Assembler for use on COSMAC Development System CDS II CDP18S005 to extend Level II COSMAC Resident Assembler RAL II by providing macro and conditional assembly capability and other new logical features.
MPM-223A (8-3/8" x 10-7/8", 20 pages)

Instruction Manual for the RCA COSMAC Evaluation Kit CDP18S020 and the EK/Assembler-Editor Design Kit CDP18S024—Provides detailed information on the two kits, each comprising the key hardware and firmware elements for a CDP1802-based computer system. Covers kit components, configuration, operation, assembly, troubleshooting, software checkout, use of resident firmware, use of Assembler-Editor programs with CDP18S024, and use of COSMAC Tiny Basic.
MPM-224 (8-3/8" x 10-7/8", 312 pages)

Micromonitor Operating System (MOPS) CDP18S831 User's Guide—Describes the use of MOPS, a software package developed to enhance the capabilities of the RCA CDP18S030 Micromonitor. Included are MOPS installation and startup, specific commands available to the user, and examples of command set usage.
MPM-231A (8-3/8" x 10-7/8", 28 pages)

Operator Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007—Tells how to operate the new COSMAC DOS Development System CDS III, which includes a Central Processor containing 28 kilobytes of user-accessible RAM, a dual-drive floppy-disk system, and a disk-file management and operating system. It considerably facilitates program development. A companion to MPM-233.
MPM-232 (8-3/8" x 10-7/8", 128 pages)

Hardware Reference Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007—Describes the hardware structure of the COSMAC DOS Development System CDS III. Includes detailed descriptions of the hardware modules supplied with the system, the card nest and control panel, the power supply, and the floppy disk system. It provides information on memory addressing and expansion and on input and output interfacing. A companion to the MPM-232.
MPM-233 (8-3/8" x 10-7/8", 63 pages)

Use of BASIC1 Compiler/Interpreter CDP18S834 with RCA COSMAC DOS Development System (CDS III)—Describes BASIC1 language and gives detailed operation information on the compiler and interpreter. Covers BASIC1 elements, statement types, programming, loading and starting the interpreter, and loading and running the compiler.
MPM-234 (8-3/8" x 10-7/8", 31 pages)

Operator Manual for the RCA COSMAC Development System IV CDP18S008—Describes how to operate the COSMAC Development System IV featuring full-screen editing capability; an integral CRT display, keyboard, and central processor; 60 kilobytes of user-accessible RAM; CDOS disk-file management and operating system; Micromonitor for in-circuit real-time debugging; and a built-in PROM programmer. A powerful aid for the design of hardware and software based on RCA-1800 series of microprocessor products.
MPM-235A (8-3/8" x 10-7/8", 170 pages)

Hardware Reference Manual for the RCA COSMAC Development System IV CDP18S008—Describes the hardware structure of the COSMAC Development System IV CDP18S008. It includes a detailed description of the modules supplied with the System IV, the card nest and backplane structure, the keyboard and display systems, the power supplies, the system signals, memory organization, floppy disk system, input and output interfaces, and the cabling and interconnection details. This Manual is intended as a companion to the Operator Manual for the RCA COSMAC Development System IV CDP18S008, MPM-235.
MPM-236 (8-3/8" x 10-7/8", 72 pages)

User Manual for the RCA COSMAC PLM 1800 High-Level-Language Compiler—Describes the PLM 1800 High-Level Language and the Compiler implementation for it. The Manual gives the grammar of the PLM constructs in Backus-Naur Form followed by an informal description and examples. It describes the CDP18S839 Compiler, provided on diskette, and designed to accelerate program development on the RCA COSMAC CDOS Development System CDP18S007 and the COSMAC Development System IV CDP18S008.
MPM-239A (8-3/8" x 10-7/8", 36 pages)

Technical Manuals (cont'd)

User Manual for the RCA COSMAC Microboard Prototyping System CDP18S691 and Control and Display Module CDP-18S640—Describes the hardware and software for the COSMAC Microboard Prototyping System CDP18S691, a fully assembled development aid for designing microcomputer systems for custom applications. It includes a description of the Microboard Control and Display Module CDP18S640.
MPM-291 (8-3/8" x 10-7/8", 56 pages)

User Manual for the RCA COSMAC Microboard Prototyping System CDP18S692 and Control and Display Module CDP-18S640V1—Guide for both the CDP18S692 Microboard Prototyping system user and for those who plan to make use of the features of the CDP18S640V1 Control and Display Module in a custom design. The Manual includes a detailed description of the system components, how they tie in with each other, how to set up the system, how to use the UT61 utility program, and how to use the several additional utility routines. It also includes information on machine language programming of the system, memory addressing, memory expansion, and input/output interfacing.
MPM-292 (8-3/8" x 10-7/8", 60 pages)

(MCDS) CDP18S693 and CDP18S694—Intended for users of the Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694. It describes in detail the hardware structure and the software features and commands of the two systems.
MPM-293 (8-3/8" x 10-7/8", 108 pages)

VIS Interpreter CDP18S835 User Manual—Describes the interpretive language developed specifically to support the CDP1869 and CDP1870/CDP1876, Video Interface System (VIS). The interpretive commands allow the user to control the VIS to provide displays of text, graphics, and motion on a cathode-ray tube in black and white or color. The interpreter is useful on any system containing the VIS chip set and is particularly supportive of the CDP18S661, RCA Microboard Video-Audio-Keyboard Interface.
MPM-835 (8-3/8" x 10-7/8", 32 pages)

BASIC2 High-Level-Language Interpreter CDP18S840 User Manual—Describes the BASIC2 language and gives detailed operation information for the interpreter. The BASIC2 interpreter CDP18S840 is designed for use on RCA COSMAC Development Systems (CDS) equipped with a Floppy Disk Dual Drive Mechanism.
MPM-840A (8-3/8" x 10-7/8", 44 pages)

BASIC3 High-Level-Language Interpreter CDP18S841 User Manual—Describes the BASIC3 language and gives detailed operation information for the interpreter which is supplied in two versions. The first version is designed for use on an RCA COSMAC Microboard Computer Development System (MCDS) equipped with a Cassette Tape Drive Mechanism. The second version, a subset of the first, called Run-Time BASIC CDP18S842 is designed for use in custom-made systems comprised of RCA Microboard modules.
MPM-841A (8-3/8" x 10-7/8", 48 pages)

Catalogs and Brochures

COSMAC Microboard Computer Systems—Describes 31 Microboard modules along with the greatly expanded line of microprocessor-system supporting hardware and software available from RCA. This new booklet describes five Microboard computers, nine Microboard memories, seven digital I/O expansion modules, two video-audio-keyboard interface modules, and eight A/D and D/A converters. The booklet also covers a broad range of chassis and accessories, the new Microboard Computer Development Systems (MCDS), and the 1800 Development Systems. High-level languages described include the ASM8 COSMAC Macro Assembler, the PLM 1800 Compiler, BASIC1 Compiler/Interpreter, BASIC2 Interpreter, BASIC3 Interpreter, and the new Micro Concurrent PASCAL Compiler/Interpreter.
CMB-250B (8-3/8" x 10-7/8", 16 pages)

COSMAC Microprocessor Product Guide—Includes significant features, ratings, electrical characteristics, and functional and terminal diagrams for the RCA CDP1800 series of COSMAC microprocessors and associated memory and peripheral integrated circuits. Descriptive information is also provided on RCA general-purpose CMOS memories, COSMAC microprocessor development and support systems, and COSMAC Microboard computer modules.
MPG-180D (8-3/8" x 10-7/8", 40 pages)

Microsystems Product Guide and Price List—This catalog contains ordering information, prices, and descriptive text and data for the extensive line of RCA CMOS microsystems. This broad series of microprocessor-based products includes development, prototyping, and evaluation systems; Microboard computer, memory, and I/O expansion modules; software and hardware support systems; and accessory items.
MPL-200 (8-3/8" x 10-7/8", 24 pages)

CDP1802 Microprocessor Instruction Summary—Handy pocket guide to the CDP1802 microprocessor instruction summary. Contains CDP1802 flow chart, complete instruction summary, and hexadecimal-decimal conversion chart.
MPM-920B (3-3/8" x 4-7/8", 16 pages)

Mask Programmable ROMs—Sales Policy and Data Programming Instructions—Explains the RCA sales policy and describes the technical features and options for each ROM type. The custom ROM types currently available from RCA Solid State Division are listed together with a pin-out diagram, significant features, and descriptive information for each basic type. The main emphasis of the booklet, however, is on the programmable options available for each ROM type and the methods the customer uses to submit programming instructions to RCA. These items are described in detail.
RPP-610 (8-3/8" x 10-7/8", 8 pages)

DATABOOK

RCA LSI Products-Applications—Collection of current application notes on 1800-series products describes specific hardware and software interface schemes of memory or peripheral components with an 1800-series central processing unit (CPU) and provides tutorial information on basic concepts, general device architecture and characteristics, and features and advantages of the 1800-series family. This information serves as a useful design guide to the system designer in determining the required hardware and software for his microcomputer-based design.
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